V58XA System

Service Guide

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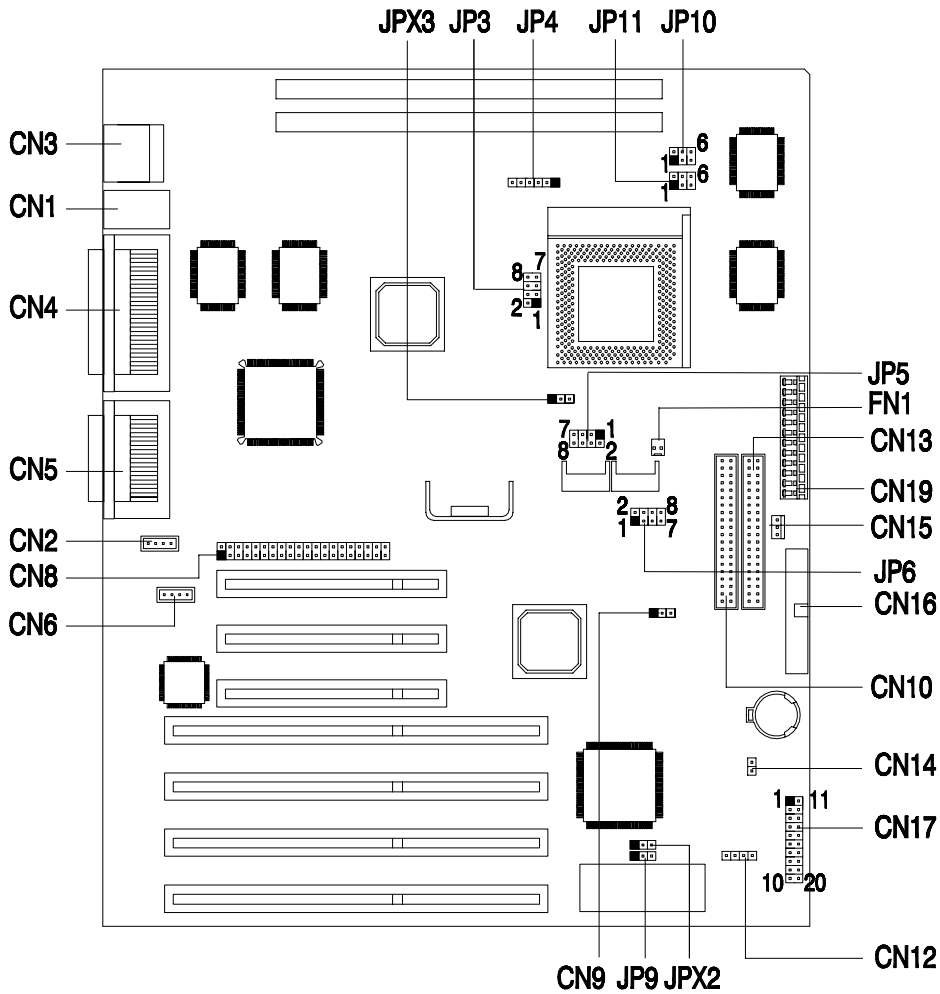
Appendix A: Schematics

C h a p t e r 1

Jumper Settings

1.1 System Board Layout



Note: The blackened pin of a jumper represents pin 1.

Figure 1 System Board Jumper and Connector Locations

1.2 System Board Jumper Settings

Table 1 System Board Jumper Settings

Jumper/Settings	Function
JPX2 1-2 2-3*	BIOS logo setting Without IBM logo shown on screen during POST With IBM logo shown on screen during POST
System board PCB number: 97114-1 JP4 1-2, 4-5 1-2, 5-6 2-3, 5-6 2-3, 4-5	Core/bus frequency rate P54C 6X86L P55C/6X86MX/K6 1.5 3.0 3.5 2.0 2.0 2.0 2.5 -- 2.5 3.0 -- 3.0
System board PCB number: 97114-2 JPX3, JP4 2-3, (1-2, 4-5) 2-3, (1-2, 5-6) 2-3, (2-3, 5-6) 2-3, (2-3, 4-5) 1-2, (1-2, 5-6) 1-2, (2-3, 5-6)	Core/bus frequency rate P54C 6X86L P55C/6X86MX/K6 1.5 3.0 3.5 2.0 2.0 2.0 2.5 -- 2.5 3.0 -- 3.0 -- -- 4.0 (not applicable to 55.38401.061) -- -- 4.5 (not applicable to 55.38401.061)
System board PCB number: 97114-1 JP3, JP5, JP6 Closed$_{\beta}$, Open$_{\alpha}$, 3-5 Closed$_{\beta}$, Open$_{\alpha}$, 2-4 Closed$_{\beta}$, Open$_{\alpha}$, 4-6 Closed$_{\beta}$, Open$_{\alpha}$, 7-8 Open$_{\alpha}$, Closed$_{\beta}$, 1-3 Open$_{\alpha}$, Closed$_{\beta}$, 3-5	Processor core voltage 2.1V (reserved) 2.8V 2.9V 3.2V 3.3V 3.52V
System board PCB number: 97114-2 JP3, JP5, JP6 Closed$_{\beta}$, Open$_{\alpha}$, 3-5 Closed$_{\beta}$, Open$_{\alpha}$, 2-4 Closed$_{\beta}$, Open$_{\alpha}$, 4-6 Closed$_{\beta}$, Open$_{\alpha}$, 7-8 Open$_{\alpha}$, Closed$_{\beta}$, 1-3 Open$_{\alpha}$, Closed$_{\beta}$, 3-5	Processor core voltage 2.2V (2.1V for 55.38401.061) 2.8V 2.9V 3.2V 3.3V 3.52V
JP9 1-2* 2-3	Password security Check password Bypass password

$_{\alpha}$: Disconnected, no jumper installed.

$_{\beta}$: Connections pins 1-2, 3-4, 5-6, 7-8.

* : Default setting.

Jumper/Settings	Function
JP10, JP11 (1-3, 2-4), (1-3, 2-4) (3-5, 4-6), (1-3, 2-4) (1-3, 2-4), (3-5, 4-6) (3-5, 4-6), (3-5, 4-6)	Host / PCI bus frequency 60 /30 MHz 66 /33 MHz 75 /30 MHz 83 /33 MHz

1.3 Processor Type Jumper Settings

Warning: *You must check out the exact processor type before setting the processor type jumpers. The wrong processor type jumper setting may damage CPU, especially the single/dual voltage setting.*

Table 2 Processor Type Jumper Settings

CPU	JP3	JPX3δ	JP4	JP5	JP6	JP10	JP11
Pentium							
P-166	Openα	2-3	2-3, 5-6	Closedβ	1-3	3-4, 5-6	1-3, 2-4
P-200	Openα	2-3	2-3, 4-5	Closedβ	1-3	3-4, 5-6	1-3, 2-4
Pentium MMX							
P-166	Closedβ	2-3	2-3, 5-6	Openα	2-4	3-5, 4-6	1-3, 2-4
P-200	Closedβ	2-3	2-3, 4-5	Openα	2-4	3-5, 4-6	1-3, 2-4
P-233	Closedβ	2-3	1-2, 4-5	Openα	2-4	3-5, 4-6	1-3, 2-4
Cyrix/IBM 6x86L							
PR166+	Closedβ	2-3	1-2, 5-6	Openα	2-4	3-5, 4-6	1-3, 2-4
PR200+	Closedβ	2-3	1-2, 5-6	Openα	2-4	1-3, 2-4	3-5, 4-6
Cyrix/IBM 6x86MX							
PR166+	Closedβ	2-3	1-2, 5-6	Openα	4-6	3-5, 4-6	1-3, 2-4
AMD K6							
PR166	Closedβ	2-3	2-3, 5-6	Openα	4-6	3-5, 4-6	1-3, 2-4
PR200	Closedβ	2-3	2-3, 4-5	Openα	4-6	3-5, 4-6	1-3, 2-4
PR233	Closedβ	2-3	1-2, 4-5	Openα	7-8	3-5, 4-6	1-3, 2-4
AMD K6 (for PCB number: 97114-2)							
PR266	Closedβ	1-2	1-2, 5-6	Openα	3-5	3-5, 4-6	1-3, 2-4
PR300	Closedβ	1-2	2-3, 5-6	Openα	3-5	3-5, 4-6	1-3, 2-4

δ : JPX3 is an optional jumper, the system board may come without it.

α : Disconnected, no jumper installed.

β : Connections pins 1-2, 3-4, 5-6, 7-8.

1.4 Connector and Functions

Table 3 System Board Connector Functions

Connector	Function	Connect to…
CN1	Lower: PS/2 keyboard connector Upper: PS/2 mouse connector	Keyboard Mouse
CN2	Modem/voice-in connector	Modem card
CN3	Universal serial bus (USB) connectors	USB devices
CN4	Upper: Printer port Lower: Serial port Video port	Printer Serial device Monitor
CN5	Upper: MIDI/game port Lower: Line-out, line-in, mic-in ports	Joystick Speaker, microphone
CN6	CD audio input connector	CD-ROM drive
CN8	ATI media connector (AMC)	Reserved
CN9	Modem ring-in wake-up connector	Modem card
CN10	Secondary IDE channel	CD-ROM drive
CN12	Hard disk LED connector Connect the red wire to pin-1, white wire to pin-2, then leave pin-3, -4 as non-connected; or connect the red wire to pin-4, white wire to pin-3, then leave pin-1,-2 as non-connected.	Hard disk drive
CN13	Primary IDE channel	Hard disk drive
CN14	Power/suspend switch connector This connector has no directional concern.	Power/suspend switch
CN15	Standby power connector	Power supply
CN16	Diskette connector	Diskette drive
CN17	Power LED connector. Connect the green wire to pin-12, white wire to pin-14.	Power LED
CN19	System board power connector	Power supply
FN1	Processor fan connector	CPU heat sink

1.5 DIMM Configurations

Table 4 DIMM Configurations

DIMM1	DIMM2	Total Memory
8 MB		8 MB
16 MB		16 MB
32 MB		32 MB
	8 MB	8 MB
	16 MB	16 MB
	32 MB	32 MB
8 MB	8 MB	16 MB
8 MB	16 MB	24 MB
8 MB	32 MB	40 MB
16 MB	8 MB	24 MB
16 MB	16 MB	32 MB
16 MB	32 MB	48 MB
32 MB	8 MB	40 MB
32 MB	16 MB	48 MB
32 MB	32 MB	64 MB

C h a p t e r 2

Major Chipsets

2.1. M1531

The Aladdin-IV is the succeeding generation chipset of Aladdin-III from Acer Labs. It maintains the best system architecture (two-chip solution) to achieve the best system performance with the lowest system cost (TTL-free). The Aladdin-IV consists of two BGA chips to give the 586-class system a complete solution with most up-to-date features and architecture for multimedia/ multithreading OS and software applications. It utilizes the modern BGA package to improve the AC characterization, resolves system bottleneck and makes the system manufacturing easier.

The M1531 includes:

- Higher CPU bus frequency (up to 83.3 MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and Memory Cache L2 controller
- Internal MESI tag bits (8K x 2) to reduce cost and enhance performance
- High-performance FPM/EDO/SDRAM DRAM controller
- PCI 2.1 compliant bus interface
- Smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance
- Highly efficient PCI fair arbiter
- The most flexible 32/64-bit memory bus interface for the best DRAM upgrade ability and ECC/parity design to enhance the system reliability

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, while PCI-to-DRAM access can run concurrently with CPU-to-L2 access. The M1531 also supports the snoop ahead feature to achieve the PCI master full-bandwidth access (133 MB) and provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support the Microsoft's On Now technology OS.

The M1533 offers the best power management system solution. It integrates ACPI support, deep green function, two-channel dedicated Ultra-33 IDE master controller, two-port USB controller, SMBus controller, and PS2 keyboard/mouse controller.

The M1543 provides the best desktop system solution. It integrates ACPI support, green function, two-channel dedicated Ultra-33 IDE Master controller, two-port USB controller, SMBus controller, PS/2 keyboard/mouse controller and the Super I/O (Floppy Disk Controller, two serial port/one parallel port) support.

The Aladdin-IV gives a highly-integrated system solution and a most up-to-date architecture to provide the best cost/performance system solution for desktop and notebook vendors.

2.1.1 Features

- Supports all Intel/Cyrix/AMD/TI/IBM 586 processors. Host bus at 83.3, 75, 66, 60 and 50 MHz at 3.3V/2.5V

- Supports Linear Wrap mode for Cyrix M1 and M2
    - Write-Allocation feature for K6
    - Pseudo-Synchronous PCI bus access
      (CPU bus: 75 MHz - PCI bus: 30 MHz, CPU bus: 83.3 MHz - PCI bus: 33 MHz)

- Supports Pipelined-burst SRAM/Memory Cache
    - Direct mapped, 256 KB/512 KB/1 MB
    - Write-Back/Dynamic-Write-Back cache policy
    - Built-in 8K x 2 bit SRAM for MESI protocol to reduce cost and enhance performance
    - Cacheable memory up to 64 MB with 8-bit Tag SRAM
    - Cacheable memory up to 512 MB with 11-bit Tag SRAM
    - 3-1-1-1-1-1-1-1 for Pipelined-burst SRAM/Memory Cache at back-to-back burst read and write cycles
    - 3.3V/5V SRAMs for Tag address
    - CPU single-read cycle L2 allocation

- Supports FPM/EDO/SDRAM DRAMs
    - 8 RAS lines up to 1 GB support
    - 64-bit data path to memory
    - Symmetrical/Asymmetrical DRAMs
    - 3.3V or 5V DRAMs
    - Duplicated MA[1:0] driving pins for burst access
    - No buffer needed for RASJ and CASJ and MA[1:0]
    - CBR and RAS-only refresh for FPM
    - CBR and RAS-only refresh and Extended refresh and self refresh for EDO
    - CBR and Self refresh for SDRAM
    - 16 Qword deep merging buffer for 3-1-1-1-1-1-1-1 posted-write cycle to enhance high-speed CPU burst access
    - 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit, 5-2-2-2-2-2-2-2 for back-to-back EDO read page hit, 6-1-1-1-2-1-1-1 for back-to-back SDRAM read page hit, 2-2-2-2 for retired data for posted write on FPM and EDO page-hit, x-1-1-1 for retired data for posted write SDRAM page-hit
    - Enhanced DRAM page miss performance
    - Supports 64 Mbit (16M x 4, 8M x 8, 4M x 16) technology of DRAMs

- Supports Programmable-strength RAS/CAS/ MWEJ/MA buffers
- Supports Error Checking and Correction (ECC) and Parity for DRAM
- Supports the most flexible six 32-bit populated banks of DRAM for easy DRAM upgrade
- Supports SIMM and DIMM
- Synchronous/Pseudo Synchronous 25/30/33MHz 3.3V/5V tolerance PCI interface
- Concurrent PCI architecture
- PCI bus arbiter: five PCI masters and M1533/ M1543 (ISA Bridge) supported
- 6 DWords for CPU-to-PCI memory write posted buffers
- Converts back-to-back CPU to PCI memory write to PCI burst cycle
- 38/22 Dwords for PCI-to-DRAM Write-posted/ Read-prefetching buffers
- PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write-back)
- L1/L2 pipelined-snoop ahead for PCI-to-DRAM cycle
- Supports PCI mechanism #1 only
- Complies with PCI spec. 2.1 (N(32/16/8)+8 rule, passive release, fair arbitration)
- Enhanced performance for Memory-Read-Line, Memory-Read-Multiple and Memory-write- Invalidate PCI commands

- Enhanced Power Management
  - ACPI support
  - PCI bus CLKRUN function
  - Dynamic Clock Stop
  - Power-on Suspend
  - Suspend to Disk
  - Suspend to DRAM
  - Self refresh during Suspend

- 328-pin (27mm x 27mm) BGA package

2.1.2 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	PHLDAJ	AD3	AD6	AD8	AD12	PAR	TRDYJ	AD17	AD22	AD25	AD30	REQJ3	GNTJ2	GNTJ3	MPD2	MPD0	MD61	MD29	MD62
B	BEJ0	PHLDJ	AD2	AD5	AD7	AD11	CBEJ1	DEVSELJ	AD16	AD21	AD24	AD29	REQJ2	GNTJ1	MPD5	MPD1	MD63	MD27	MD60	MD28
C	BEJ3	BEJ2	BEJ1	AD4	CBEJ0	AD10	AD15	STOPJ	CBEJ2	AD20	CBEJ3	AD28	REQJ1	GNT0J	MPD4	MD30	MD25	MD58	MD26	MD59
D	BEJ6	BEJ5	BEJ4	AD0	AD1	AD9	AD14	LOCKJ	FRAMEJ	AD19	AD23	AD27	REQJ0	MPD7	MPD3	MD55	MD23	MD56	MD24	MD57
E	DCJ	HITMJ	EADSJ	BEJ7	RSTJ	PCIMRQJ	AD13	SERRJ	IRDYJ	AD18	PCLKIN	AD26	AD31	MPD6	MD31	MD20	MD53	MD21	MD54	MD22
F	BRDYJ	BOFFJ	SMIACTJ	HLOCKJ	ADSJ	VCC_B								VCC_C	VCC_C	MD50	MD18	MD51	MD19	MD52
G	HD63	CACHEJ	AHOLD	KENJ	NAJ	VCC_A			**M1531**						VCC_C	MD15	MD48	MD16	MD49	MD17
H	HD60	HD61	HD62	WRJ	MIOJ			GND	GND	GND	GND	GND	GND			MD45	MD13	MD46	MD14	MD47
J	HD55	HD56	HD57	HD58	HD59			GND	GND	GND	GND	GND	GND			MD10	MD43	MD11	MD44	MD12
K	HD51	HD52	HD53	HD54	HCLKIN			GND	GND	GND	GND	GND	GND			MD40	MD8	MD41	MD9	MD42
L	HD46	HD47	HD48	HD49	HD50			GND	GND	GND	GND	GND	GND			MD5	MD38	MD6	MD39	MD7
M	HD41	HD42	HD43	HD44	HD45			GND	GND	GND	GND	GND	GND			MD35	MD3	MD36	MD4	MD37
N	HD36	HD37	HD38	HD39	HD40			GND	GND	GND	GND	GND	GND		VDD5S	REQJ4	GNTJ4	MD1	MD34	MD2
P	HD31	HD32	HD33	HD34	HD35	VCC_A									VCC_C	32K	SUSPEND	MD32	MD0	MD33
R	HD26	HD27	HD28	HD29	HD30	VDD5	VCC_A							VCC_B	VCC_C	RASJ6	RASJ7	CASJ2	CASJ7	CASJ3
T	HD21	HD22	HD23	HD24	HD25	HD0	A12	A5	GWEJ	COEJ	CADVJ	TWEJ	MAA0	MAA1	TIO8	TIO9	TIO10	RASJ1	RASJ0	CASJ6
U	HD16	HD17	HD18	HD19	HD20	HD1	A13	A8	CCSJ	BWEJ	CADSJ	TIO0	TIO1	MAB0	MAB1	MA5	MWEJ	RASJ4	RASJ3	RASJ2
V	HD15	HD14	HD13	HD6	HD3	A17	A14	A10	A4	A29	A25	A24	A23	TIO2	MA2	MA4	MA8	CASJ5	CASJ1	RASJ5
W	HD12	HD11	HD10	HD5	HD2	A18	A15	A11	A7	A30	A31	A22	A21	TIO4	TIO6	MA3	MA7	MA10	CASJ0	CASJ4
Y	HD9	HD8	HD7	HD4	A20	A19	A16	A9	A6	A3	A28	A26	A27	TIO3	TIO5	TIO7	MA6	MA9	MA11	NC

TOP VIEW

Figure 2-1 M1531 Pin Diagram

2.1.3 Pin Descriptions

Table 2- 1 M1531 Signal Descriptions

Signal	Type	Description
Host Interface 3.3V/2.5V		
A[31:3]	I/O Group A	Host Address Bus Lines. A[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1531 drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	I Group A	Byte Enables. These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1531.
ADSJ	I Group A	Address Strobe. The CPU will start a new cycle by asserting ADSJ first. The M1531 will not precede to execute a cycle until it detects ADSJ active.
BRDYJ	O Group A	Burst Ready. The assertion of BRDYJ means the current transaction is complete. The CPU terminates the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	O Group A	Next Address. This signal is asserted by the M1531 to inform the CPU that pipelined cycles are ready for execution.
AHOLD	O Group A	CPU AHold Request Output. It connects to the input of CPU's AHOLD pin and is actively driven for inquiry cycles.
EADSJ	O Group A	External Address Strobe. This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1531 asserts this signal to proceed snooping.
BOFFJ	O Group A	CPU Back-Off. If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1531 asserts this signal to request CPU floating all its output buses.
HITMJ	I Group A	Primary Cache Hit and Modified. When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.
MIOJ	I Group A	Host Memory or I/O. This bus definition pin indicates the current bus cycle is either memory or input/ output.
DCJ	I Group A	Host Data or Code. This bus definition pin is used to distinguish data access cycles from code access cycles.
WRJ	I Group A	Host Write or Read. When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.
HLOCKJ	I Group A	Host Lock. When HLOCKJ is asserted by the CPU, the M1531 will recognize the CPU is locking the current cycles.
CACHEJ	I Group A	Host Cacheable. This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.
Host Interface 3.3V/2.5V		

Table 2- 1 M1531 Signal Descriptions

Signal	Type	Description
KENJ/INV	O Group A	Cache Enable Output. This signal is connected to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1531 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	I Group A	SMM Interrupt Active. This signal is asserted by the CPU to inform the M1531 that SMM mode is being entered.
HD[63:0]	I/O Group A	Host Data Bus Lines. These signals are connected to the CPU's data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.
MPD[7:0]	I/O Group C	DRAM Parity /ECC check bits. These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit.
RASJ[7] / SRASJ[0]	O Group C	Row Address Strobe 7, (FPM/EDO) of DRAM row 7. SDRAM Row Address Strobe (SDRAM) copy 0. It connects to SDRAM RASJ. This is a multifunction pin and determined by Index-5Ch bit0.
RASJ[6] / SCASJ[0]	O Group C	Row Address Strobe 6, (FPM/EDO) of DRAM row 6. SDRAM Column address strobe (SDRAM) copy 0. It connects to SDRAM CASJ. This is a multifunction pin and determined by Index-5Ch bit0.
RASJ[5:0]	O Group C	Row Address Strobes. These signals are used to drive the corresponding RASJs of FPM/EDO DRAMs. In SDRAM, they are used to drive the corresponding SDRAM CSJs.
CASJ[7:0] / DQM[7:0]	O Group C	Column Address Strobes or Synchronous DRAM Input/Output Data Mask. These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].
MA[11:2]	O Group C	DRAM Address Lines. These signals are the address lines[11:2] of all DRAMs. The M1531 supports DRAM types ranging from 256K to 64Mbits.
MAA[1:0]	O Group C	Memory Address copy A for [1:0]. These signals are the address lines[1:0] copy 0 of all DRAMs.
MAB[1:0]	O Group C	Memory Address copy B for [1:0]. These signals are the address lines[1:0] copy 1 of all DRAMs.
MWEJ[0]	O Group C	DRAM Write Enable. This is the DRAM write enable pin and behaves according to the early-write mechanism, i.e. , it activates before the CASJs do. For refresh cycles, it will remain deasserted.
MD[63:0]	I/O Group C	Memory Data. These pins are connected to DRAM's data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.
Host Interface 3.3V/2.5V		
CLKEN[0]/ REQJ[4]	I/O Group C	SDRAM Clock Enable Copy 0 or PCI Master Request. This signal is used as SDRAM clock enable copy 0 to do self refresh during suspend. It can also be used as bus request signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.

Table 2- 1 M1531 Signal Descriptions

Signal	Type	Description
CLKEN[1]/ GNTJ[4]	O Group C	SDRAM Clock Enable Copy 1 or PCI Master Grant. This signal is used as SDRAM clock enable copy 1 to do self refresh during suspend. It can also be used as grant signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.
Secondary Cache Interface 3.3V/2.5V Tolerance		
CADVJ	O Group A	Synchronous SRAM Advance. This signal will make PBSRAM/Memory Cache internal burst address counter advance.
CADSJ	O Group A	Synchronous SRAM Address Strobe. This signal connects to PBSRAM/ Memory Cache ADSCJ.
CCSJ	O Group A	Synchronous SRAM Chip Select. This signal connects to PBSRAM/Memory Cache CE1J to mask ADSPJ and enable ADSCJ sampling.
GWEJ	O Group A	Synchronous SRAM Global Write Enable. This signal will write all the byte lanes data into PBSRAM/Memory Cache.
COEJ	O Group A	Synchronous SRAM Output Enable. This signal will enable the data output driving of PBSRAM/Memory Cache.
BWEJ	O Group A	Synchronous SRAM Byte-Write Enable. This signal connects to byte write enable of PBSRAM/Memory Cache.
TIO[10]/ MWEJ[1]/ MKREFRQJ	I/O Group C	SRAM Tag[10] or another copy of MWEJ or DRAM Cache MKREFRQJ. This pin is used for multifunction. It can be SRAM tag address bit 10, or another copy of MWEJ connected to DRAM, or MKREFRQJ connected to DRAM Cache. Refer to Register Index-41h bit 6, bit3 and bit0 description.
TIO[9]/ SRASJ[1]	I/O Group C	SRAM Tag[9] or Synchronous DRAM (SDRAM) RAS copy 1. This pin is used for multifunction. It can be SRAM tag address bit 9, or another copy of SRASJ connected to SDRAM. Refer to Register Index-41h bit3 and bit0 description.
TIO[8]/ SCASJ[1]	I/O Group C	SRAM Tag[8] or Synchronous DRAM (SDRAM) CAS copy 1. This pin is used for multifunction. It can be SRAM tag address bit 8, or another copy of SCASJ connected to SDRAM. Refer to Register Index-41h bit3 and bit0 description.
TIO[7:0]	I/O Group B	SRAM Tag[7:0]. This pin contains the L2 tag address for 256-KB L2 caches. TIO[6:0] contain the L2 tag address and TIO7 contains the L2 cache valid bit for 512-KB caches. TIO[5:0] contain L2 tag address, TIO7 contains L2 cache valid bit and TIO6 contains the L2 cache dirty bit for 1-MB cache. Refer to index-41h cache configuration table.
TAGWEJ	O Group B	Tag Write Enable. This signal, when asserted, will write into the external tag new state and tag addresses.
PCI Interface 3.3V/2.5V Tolerance		
AD[31:0]	I/O Group B	PCI Address and Data Bus Lines. These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBEJ[3:0]	I/O Group B	PCI Bus Command and Byte Enables. Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.

Table 2- 1 M1531 Signal Descriptions

Signal	Type	Description
FRAMEJ	I/O Group B	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. It will be as an output driven by M1531 on behalf of CPU, or as an input during PCI master access.
DEVSELJ	I/O Group B	Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	I/O Group B	Initiator Ready. This signal indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	I/O Group B	Target Ready. This pin indicates the target is ready to complete the current data phase of transaction.
STOPJ	I/O Group B	Stop. This signal indicates the target is requesting the master to stop the current transaction.
LOCKJ	I/O Group B	Lock Resource Signal. This pin indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[3:0]	I Group B	Bus Request signals of PCI Masters. When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.
GNTJ[3:0]	O Group B	Grant signals to PCI Masters. When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.
PHLDJ	I Group B	PCI bus Hold Request. This active low signal is a request from M1533/M1543 for the PCI bus.
PHLDAJ	O Group B	PCI bus Hold Acknowledge. This active low signal grants PCI bus to M1533/M1543.
PAR	I/O Group B	Parity bit of PCI bus. It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ/ CLKRUNJ	I/O Group B	System Error or PCI Clock RUN. If the M1531 detects parity errors in DRAMs, it will assert SERRJ to notify the system. As CLKRUNJ, this signal will connect to M1533 CLKRUNJ to start, or maintain the PCI CLOCK. It is a multifunction pin and determined by Index-77h bit0.
Clock, Reset, and Suspend		
HCLKIN	I Group A	CPU bus Clock Input. This signal is used by all of the M1531 logic that is in the Host clock domain.
RSTJ	I Group B	System Reset. This pin, when asserted, resets the M1531 state machine, and sets the register bits to their default values.
Clock, Reset, and Suspend		
PCICLK	I Group B	PCI bus Clock Input. This signal is used by all of the M1531 logic that is in the PCI clock domain.
PCIMRQJ	O Group B	Total PCI Request. This signal is used to notify M1533/M1543 that there is PCI master requesting PCI bus.
SUSPENDJ	I Group C	Suspend. When actively sampled, the M1531 will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.

Table 2- 1 M1531 Signal Descriptions

Signal	Type	Description
OSC32KO	I Group C	The refresh reference clock of frequency 32 KHz during suspend mode. This signal should be pulled to a fixed value when the suspend feature is disabled.
Power Pins		
VCC_A	P	Vcc 3.3V or 2.5V Power for Group A. This power is used for CPU interface and L2 control signals. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VCC_B	P	Vcc 3.3V Power for Group B. This power is used for PCI interface and Tag signals. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VCC_C	P	Vcc 3.3V Power for Group C. This power is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VDD_5	P	Vcc 5.0V Power for Group A and Group B. This pin supplies the 5V input tolerance circuit and the core power for the internal circuit except the suspend circuit.
VDD_5S	P	Vcc 5.0V Power for Group C. This pin supplies the 5V input tolerance circuit and the core power for the internal suspend circuit.
Vss or Gnd	P	Ground

2.1.4 Numerical Pin List

Pin No.	Pin Name	Pin Type
A1	--	-
A2	PHLDAJ	O
A3	AD3	I/O
A4	AD6	I/O
A5	AD8	I/O
A6	AD12	I/O
A7	PAR	I/O
A8	TRDYJ	I/O
A9	AD17	I/O
A10	AD22	I/O
A11	AD25	I/O
A12	AD30	I/O
A13	REQJ3	I
A14	GNTJ2	O
A15	GNTJ3	O
A16	MPD2	I/O
A17	MPD0	I/O
A18	MD61	I/O
A19	MD29	I/O
A20	MD62	I/O
B1	BEJ0	I
B2	PHLDJ	I
B3	AD2	I/O
B4	AD5	I/O
B5	AD7	I/O
B6	AD11	I/O
B7	CBEJ1	I/O
B8	DEVSELJ	I/O
B9	AD16	I/O
B10	AD21	I/O
B11	AD24	I/O
B12	AD29	I/O
B13	REQJ2	I
B14	GNTJ1	O
B15	MPD5	I/O
B16	MPD1	I/O
B17	MD63	I/O
B18	MD27	I/O

B19	MD60	I/O
B20	MD28	I/O
C1	BEJ3	I
C2	BEJ2	I
C3	BEJ1	I
C4	AD4	I/O
C5	CBEJ0	I/O
C6	AD10	I/O
C7	AD15	I/O
C8	STOPJ	I/O
C9	CBEJ2	I/O
C10	AD20	I/O
C11	CBEJ3	I/O
C12	AD28	I/O
C13	REQJ1	I
C14	GNTJ0	O
C15	MPD4	I/O
C16	MD30	I/O
C17	MD25	I/O
C18	MD58	I/O
C19	MD26	I/O
C20	MD59	I/O
D1	BEJ6	I
D2	BEJ5	I
D3	BEJ4	I
D4	AD0	I/O
D5	AD1	I/O
D6	AD9	I/O
D7	AD14	I/O
D8	LOCKJ	I/O
D9	FRAMEJ	I/O
D10	AD19	I/O
D11	AD23	I/O
D12	AD27	I/O
D13	REQJ0	I
D14	MPD7	I/O
D15	MPD3	I/O
D16	MD55	I/O
D17	MD23	I/O
D18	MD56	I/O
D19	MD24	I/O

D20	MD57	I/O
E1	DCJ	I
E2	HITMJ	I
E3	EADSJ	O
E4	BEJ7	I
E5	RSTJ	I
E6	PCIMRQJ	O
E7	AD13	I/O
E8	SERRJ	I/O
E9	IRDYJ	I/O
E10	AD18	I/O
E11	PCLKIN	I
E12	AD26	I/O
E13	AD31	I/O
E14	MPD6	I/O
E15	MD31	I/O
E16	MD20	I/O
E17	MD53	I/O
E18	MD21	I/O
E19	MD54	I/O
E20	MD22	I/O
F1	BRDYJ	O
F2	BOFFJ	O
F3	SMIACTJ	I
F4	HLOCKJ	I
F5	ADSJ	I
F6	VCC_B	P
F14	VCC_C	P
F15	VCC_C	P
F16	MD50	I/O
F17	MD18	I/O
F18	MD51	I/O
F19	MD19	I/O
F20	MD52	I/O
G1	HD63	I/O
G2	CACHEJ	I
G3	AHOLD	O
G4	KENJ	O
G5	NAJ	O
G6	VCC_A	P
G15	VCC_C	P

G16	MD15	I/O
G17	MD48	I/O
G18	MD16	I/O
G19	MD49	I/O
G20	MD17	I/O
H1	HD60	I/O
H2	HD61	I/O
H3	HD62	I/O
H4	WRJ	I
H5	MIOJ	I
H8	GND	P
H9	GND	P
H10	GND	P
H11	GND	P
H12	GND	P
H13	GND	P
H16	MD45	I/O
H17	MD13	I/O
H18	MD46	I/O
H19	MD14	I/O
H20	MD47	I/O
J1	HD55	I/O
J2	HD56	I/O
J3	HD57	I/O
J4	HD58	I/O
J5	HD59	I/O
J8	GND	P
J9	GND	P
J10	GND	P
J11	GND	P
J12	GND	P
J13	GND	P
J16	MD10	I/O
J17	MD43	I/O
J18	MD11	I/O
J19	MD44	I/O
J20	MD12	I/O
K1	HD51	I/O
K2	HD52	I/O
K3	HD53	I/O
K4	HD54	I/O

K5	HCLKIN	I
K8	GND	P
K9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13	GND	P
K16	MD40	I/O
K17	MD8	I/O
K18	MD41	I/O
K19	MD9	I/O
K20	MD42	I/O
L1	HD46	I/O
L2	HD47	I/O
L3	HD48	I/O
L4	HD49	I/O
L5	HD50	I/O
L8	GND	P
L9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13	GND	P
L16	MD5	I/O
L17	MD38	I/O
L18	MD6	I/O
L19	MD39	I/O
L20	MD7	I/O
M1	HD41	I/O
M2	HD42	I/O
M3	HD43	I/O
M4	HD44	I/O
M5	HD45	I/O
M8	GND	P
M9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13	GND	P
M16	MD35	I/O
M17	MD3	I/O

M18	MD36	I/O
M19	MD4	I/O
M20	MD37	I/O
N1	HD36	I/O
N2	HD37	I/O
N3	HD38	I/O
N4	HD39	I/O
N5	HD40	I/O
N8	GND	P
N9	GND	P
N10	GND	P
N11	GND	P
N12	GND	P
N13	GND	P
N15	VDD5S	P
N16	REQJ4	I/O
N17	GNTJ4	O
N18	MD1	I/O
N19	MD34	I/O
N20	MD2	I/O
P1	HD31	I/O
P2	HD32	I/O
P3	HD33	I/O
P4	HD34	I/O
P5	HD35	I/O
P6	VCC_A	P
P15	VCC_C	P
P16	32K	I
P17	SUSPENDJ	I
P18	MD32	I/O
P19	MD0	I/O
P20	MD33	I/O
R1	HD26	I/O
R2	HD27	I/O
R3	HD28	I/O
R4	HD29	I/O
R5	HD30	I/O
R6	VDD5	P
R7	VCC_A	P
R14	VCC_B	P
R15	VCC_C	P

R16	RASJ6	O
R17	RASJ7	O
R18	CASJ2	O
R19	CASJ7	O
R20	CASJ3	O
T1	HD21	I/O
T2	HD22	I/O
T3	HD23	I/O
T4	HD24	I/O
T5	HD25	I/O
T6	HD0	I/O
T7	A12	I/O
T8	A5	I/O
T9	GWEJ	O
T10	COEJ	O
T11	CADVJ	O
T12	TWEJ	O
T13	MAA0	O
T14	MAA1	O
T15	TIO8	I/O
T16	TIO9	I/O
T17	TIO10	I/O
T18	RASJ1	O
T19	RASJ0	O
T20	CASJ6	O
U1	HD16	I/O
U2	HD17	I/O
U3	HD18	I/O
U4	HD19	I/O
U5	HD20	I/O
U6	HD1	I/O
U7	A13	I/O
U8	A8	I/O
U9	CCSJ	O
U10	BWEJ	O
U11	CADSJ	O
U12	TIO0	I/O
U13	TIO1	I/O
U14	MAB0	O
U15	MAB1	O
U16	MA5	O

U17	MWEJ	I/O
U18	RASJ4	O
U19	RASJ3	O
U20	RASJ2	O
V1	HD15	I/O
V2	HD14	I/O
V3	HD13	I/O
V4	HD6	I/O
V5	HD3	I/O
V6	A17	I/O
V7	A14	I/O
V8	A10	I/O
V9	A4	I/O
V10	A29	I/O
V11	A25	I/O
V12	A24	I/O
V13 7	A23	I/O
V14	TIO2	I/O
V15	MA2	O
V16	MA4	O
V17	MA8	O
V18	CASJ5	O
V19	CASJ1	O
V20	RASJ5	O
W1	HD12	I/O
W2	HD11	I/O
W3	HD10	I/O
W4	HD5	I/O
W5	HD2	I/O
W6	A18	I/O
W7	A15	I/O
W8	A11	I/O
W9	A7	I/O
W1 0	A30	I/O
W1 1	A31	I/O
W1 2	A22	I/O
W1 3	A21	I/O

W14	TIO4	I/O
W15	TIO6	I/O
W16	MA3	O
W17	MA7	O
W18	MA10	O
W19	CASJ0	O
W20	CASJ4	O
Y1	HD9	I/O
Y2	HD8	I/O
Y3	HD7	I/O
Y4	HD4	I/O
Y5	A20	I/O
Y6	A19	I/O
Y7	A16	I/O
Y8	A9	I/O
Y9	A6	I/O
Y10	A3	I/O
Y11	A28	I/O
Y12	A26	I/O
Y13	A27	I/O
Y14	TIO3	I/O
Y15	TIO5	I/O
Y16	TIO7	I/O
Y17	MA6	O
Y18	MA9	O
Y19	MA11	O
Y20	--	--

2.2. M1533

The M1533 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. This chip has Integrated System Peripherals (ISP) (2 x 82C59 and serial interrupt, 1 x 82C54), advanced features (Type F and Distributed DMA) in the DMA controller (2 x 82C54), PS/2 keyboard/mouse controller, two-channel dedicated IDE master controller with Ultra-33 specification, System Management Bus (SMB), and two OpenHCI 1.0a USB ports. The ACPI (Advanced Configuration and Power Interface) and PCI 2.1 (Delayed Transaction & Passive Release) specification have also been implemented. Furthermore, this chip supports the Advanced Programmable Interrupt Controller (APIC) interface for Multiple-Processors system.

The M1533 also supports the deep flexible green function for the best green system. It can connect to the ALi Pentium North Bridge (M1521/M1531/M1541) and ALi Pentium Pro North Bridge (M1615) to provide the best system solution. One eight-byte bidirectional line buffer is provided for ISA/DMA master memory read/writes; one 32-bit wide posted write buffer is provided for PCI memory write & I/O write (for audio) cycles to the ISA bus, to provide a PCI to ISA IRQ routing table, and level-to-edge trigger transfer.

The chip provides two extra IRQ lines and one programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts. The on-chip IDE controller supports two separate IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. The Ultra 33 specification (that supports the 33 MB/second transfer rate) has been implemented at this IDE controller. The ATA bus pins and the buffer (read ahead and posted write) are all dedicated for separate channel to improve the performance of IDE master.

The M1533 supports Super Green function for Intel and Intel compatible CPUs. It implements SMI or SCI (System Controller Interrupt) to meet the ACPI specification. It also meets the requirement for OnNow design initiative. It also features powerful power management for power saving including On, Standby, Sleeping, SoftOff, and Mechanical Off states. To control the CPU power consumption, it provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control. In addition, the M1533 offers the most flexible system clock design. It can be programmed to stop the CPU Clock, PCI Clock, the Clock cell, or to reduce the Clock frequency. The PBSRAM (Pipelined-burst SRAM) doze mode is also supported.

The M1533 is includes a PS/2 keyboard/mouse controller, SMBus, two OpenHCI 1.0a USB ports, and the dedicated GPIO (General Purpose Input/Output) pins. These components enable the chip to implement the best green and cost/performance system.

2.2.1 Features

- Provides a bridge between the PCI bus and ISA bus for both Pentium and Pentium Pro systems

- PCI interface
    - PCI master and slave interface
    - PCI master and slave initiated termination
    - PCI spec. 2.1 compliant (Delayed Transaction support)

- Buffers control
    - 8-byte bidirectional line buffers for DMA/ISA memory read/write cycles to PCI bus
    - 32-bit posted write buffer for PCI memory write and I/O data write (for sound card) to ISA bus
- Provides steerable PCI interrupts for PCI device plug-and-play
    - Up to eight PCI interrupt routing
    - Level-to-edge trigger transfer
- Enhanced DMA controller
    - Provides 7 programmable channels: 4 for 8-bit data size, 3 for 16-bit data size
    - 32-bit addressability
    - Provides compatible DMA transfers
    - Provides Type F transfers
- Interrupt controller
    - Provides 14 interrupt channels
    - Independent programmable level/edge triggered channels
- Counter/Timers
    - 8254 compatible timers for System Timer, Refresh Request, Speaker Output Use
- Distributed DMA supported
    - 7 DMA Channels can be arbitrarily programmed as distributed channel
- Serialized IRQ supported
    - Quiet/Continuous mode
    - Programmable (default 21) IRQ/DATA frames
    - Programmable START frame pulse width
- Plug-and-Play port supported
    - One programmable chip select
    - Two steerable interrupt request lines
- Built-in keyboard controller
    - Built-in PS/2/AT keyboard and PS/2 mouse controller
- Supports up to 256-KB ROM size decoding

- Supports positive/subtractive decode for ISA device

- PMU features
    - Full-support for ACPI and OS directed power management
    - CPU SMM Legacy mode and SMI feature supported
    - Supports programmable STPCLKJ: throttle/CKONSTP/CKOFFSTP control
    - Supports I/O trap for I/O restart feature
    - PMU operation states :
        - On
        - Standby
        - Sleeping (Power-On Suspend)
        - Suspend (Suspend to DRAM)
        - Suspend to HDD
        - Soft Off
        - Mechanical Off
    - APM state detection and control logic supported
    - Global and local device power control logic
    - Ten Programmable Timers: Standby / LB / LLB / APMA / APMB / Global_Display / Primary_IDE / Secondary_IDE / SIO&Audio / Programmable IO Region
    - Provides system activity and display activity monitorings, including:
        - Video
        - Audio
        - Hard disk
        - Floppy
        - Serial ports
        - Parallel port
        - Keyboard
        - Six programmable I/O groups
        - Three programmable memory spaces
    - Provides hot plugging events detection

  - CRT connector
  - AC power
  - Docking insert
  - Eject
  - Setup button
  - Hot key press
- Multiple external wakeup events of Standby mode
  - Power button
  - Cover open
  - Modem ring
  - RTC alarm
  - EXTSW
  - DRQ2
- Suspend wakeup detected
  - Hot key
  - Modem ring
  - RTC alarm
  - Cover open
  - Docking insert
  - Power button
  - USB events
  - IRQ
  - EJECT
  - ACPWR
  - GPIO[19:16] event
- Two-level battery warning monitor
- Thermal alarm supported

- Clock generator control logic supported
  - CPUCLK stop control
  - PCICLK stop control
  - PLL stop control
  - Down frequency control
- L2 cache power down and PCI CLKRUN control logic supported
- 21 general purpose input signals, 24 general purpose output signals, 20 general purpose input/output signals
- 16 external expandable general purpose inputs, 16 external expandable general purpose outputs
- LCD control
- All registers readable/restorable for proper resume from Suspend state

- Built-in PCI IDE controller
  - Supports Ultra 33 Synchronous DMA Mode transfers up to Mode 2 Timing (33 MB/sec)
  - Supports PIO Modes up to Mode 5 timings, and Multiword DMA Mode 0, 1 ,2 with independent timing of up to 4 drives
  - Integrated 10 x 32-bit read ahead & posted write buffers for each channel (total: 20 Dwords)
  - Dedicated pins of ATA interface for each channel
  - Supports tri-state IDE signals for swap bay

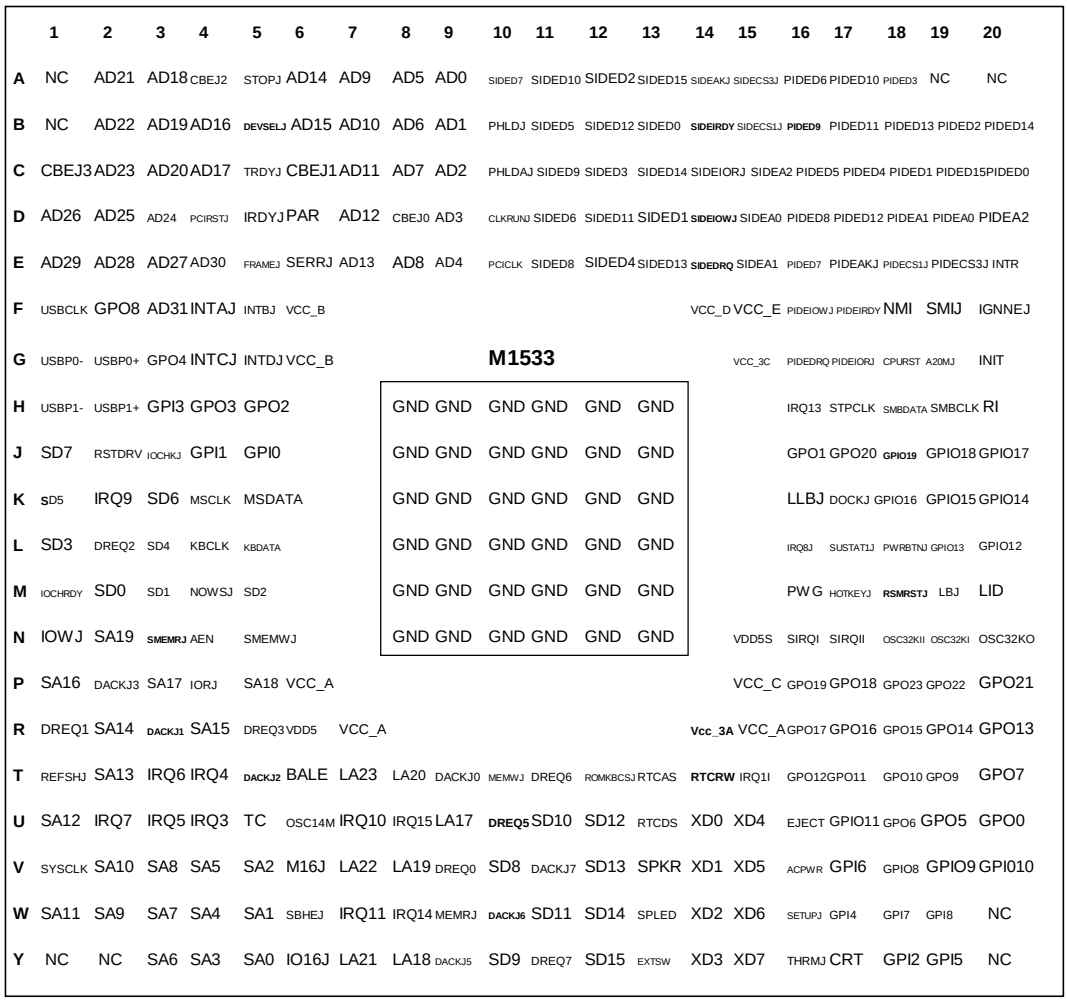
- USB interface
  - One root hub with two USB ports based on OpenHCI 1.0a specification
  - Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) serial transfer
  - Supports Legacy keyboard and mouse software with USB-based keyboard and mouse

- SMBus interface
  - System Management Bus interface which meets the v1.0 specification

- External APIC interface supported

- 328-pin (27mm x 27mm) BGA package

2.2.2 Pin Diagram



TOP VIEW

Figure 2-2 M1533 Pin Diagram

2.2.3 Pin Descriptions

Pin Name	Type	Description
Clock & Reset Unit :		
PWG	I-Group C Schmitt	Power-Good Input. This signal comes from the power supply to indicate that power is available and stable. The de-assertion of this input will enable the leakage control circuit between Soft-off (Suspend to Disk) resume circuit and no power circuit.
PCICLK	I-Group B	PCI Clock for Internal PCI Interface. This is an input PCI clock, it should always be running at ON, STANDBY, SLEEP (Power-On Suspend) state. When CLKRUNJ is active, this clock should always keep on running. Internal PCI state machine and ISA state machine will use this clock.
OSC14M	I-Group A	14.318Mhz Clock Input. This input clock will be used for Power Management timer, M8254 timer, SM bus base frequency and ISA state machine.
OSC32KI	I-Group C	32 Khz Oscillator Input1. This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The M1533 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a crystal is not used, an external 32 Khz clock input should connect to this pin.
OSC32KII	I-Group C	32 Khz Oscillator Input2. This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The M1533 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, this pin should be floated.
CLK32KO	O-Group C 2.4/2.4 mA	32 KHz Clock Output for DRAM Refresh. At ON, STANDBY, SLEEP (Power On Suspend), SUSPEND (Suspend to DRAM) states, the output will send to Memory controller, to support DRAM refresh clock. At Soft off and Suspend to Disk states, the output will drive low to avoid leakage current.
USBCLK	I-Group B	48 MHz USB Clock Input. This clock will send to USB state machine to generate USB signals.
PCI Bus Interface Unit :		
PCIRSTJ	O-Group B 12/16 mA	PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.
AD[31:0]	I/O Group B 12/16 mA	Address and Data Multiplexed Bus. During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBEJ[3:0]	I/O Group B 12/16 mA	Bus Command and Byte enable. During address phase, CBEJ[3:0] define the Bus Command. During data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	I/O Group B 12/16 mA	Cycle Frame. Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.
TRDYJ	I/O Group B 12/16 mA	Target Ready. Target Ready indicates the target's ability to complete the current data phase of the transaction.
IRDYJ	I/O Group B 12/16 mA	Initiator Ready. Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.

STOPJ	I/O Group B 12/16 mA	Cycle stop request. Cycle Stop indicates the target is requesting the master to stop the current transaction.
DEVSELJ	I/O Group B 12/16 mA	Device Select. This signal indicates that the target device has decoded the address as its own cycle. This pin is an output pin when M1533 acts as a PCI slave has decoded address as its own cycle including subtractive decoding.
SERRJ	I-Group B	System Error. This signal may be pulsed active by any agent that detects a system error condition. When SERRJ is sampling low, M1533 will assert NMI to generate non-maskable interrupt to CPU.
PAR	I/O Group B 12/16 mA	Parity Signal. PAR is an Even Parity and is calculated on AD[31:0] and CBEJ[3:0]. When M1533 acts as a PCI master, it drives PAR one PCI clock after address phase for read/write transaction and one PCI clock after data phase for write transaction. When the M1533 acts as a target, it drives PAR one PCI clock after data phase for PCI master read transaction.
PHLDAJ	I-Group B	PCI Bus Ownership Acknowledge. When PCI bus arbiter asserts this pin, M1533 has owned the PCI bus.
PHOLDJ	O-Group B 4/4 mA	PCI Bus Ownership Request. M1533 requests the ownership of the PCI bus from the PCI bus arbiter on the North Bridge. M1533 will assert this signal on behalf of the ISA Master, DMA Device, IDE Master, and the USB Master.
INTAJ_MI	I-Group B	PCI INTA. PCI interrupt input A or PCI interrupt polling input. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTAJ when 4 PCI Interrupts are supported, or connects to the 74F181 encoded output to support the 8 PCI Interrupts polling mode.
INTBJS0	I/O Group B Schmitt 4/4 mA	PCI INTB. PCI interrupt input B or polling select_0 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTBJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 0 to support the 8 PCI Interrupts polling mode.
INTCJS1	I/O Group B Schmitt 4/4 mA	PCI INTC. PCI interrupt input C or polling select_1 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTCJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 1 to support the 8 PCI Interrupts polling mode.
INTDJS2	I/O Group B Schmitt 4/4 mA	PCI INTD. PCI interrupt input D or polling select_2 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTDJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 2 to support the 8 PCI Interrupts polling mode.
CPU interface :		
INIT	O-Group E 2.4/2.4 mA	CPU Initialize Interrupt. CPU cold & warm reset. When CPU is Pentium Pro, this signal is low active. Otherwise, this signal is high active. When power on, KBC RC, port 92 RC, shutdown all will trigger INIT active.
CPURST	O-Group E 2.4/2.4 mA	CPU Cold Reset. When power turn on, this reset signal will be asserted, and then will become de-asserted until 4 ms after PWG becomes high.
IGNNEJ	O-Group E 2.4/2.4 mA	Ignore Error. This pin is used as the ignore numeric coprocessor error.
INTR	O-Group E 2.4/2.4 mA	Interrupt Request to CPU. This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt.

NMI	O-Group E 2.4/2.4 mA	Non-maskable Interrupt to CPU. This is generated by the ISA Parity error (IOCHKJ assertion), PCI Parity error or DRAM Parity error (SERRJ assertion), and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt.
A20MJ	O-Group E 2.4/2.4 mA	CPU A20 Mask. This is the CPU Address line 20 mask signal.
FERRJ/ IRQ13	I-Group E	Floating Point Error. FERRJ input to generate IRQ13. When Coprocessor interface is disabled through configuration register Index-43h bit 6 setting, the function of this pin is IRQ13.
ISA Bus Interface Unit :		
IRQ[15:14], IRQ[11:9], IRQ[7:3]	I/O Group A Schmitt 9.6/9.6 mA	Interrupt Request. The Interrupt Request lines are directly from the ISA Bus, from the PCI Interrupt Routing, or from the steerable Interrupt pins. The M1533 will also drive the interrupt pins if the source is not from the ISA bus to support the APIC interface.
RSTDRV	O-Group A 12/16 mA	ISA Bus reset. This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.
SD[15:8]	I/O Group A 12/12 mA	ISA High Byte Slot Data Bus. These pins should connect to the ISA High Byte Slot Data Bus.
XD[7:0]	I/O Group A 12/12 mA	XD Data Bus. When the SD[7:0] pins are defined as the GPIO[7:0] pins, these pins can be used to drive SD[7:0] if TTL LS245 is used as a buffer. M1533 signal XDIR will control this buffer.
SD[7:0]/ GPIO[7:0]	I/O Group A 12/12 mA	ISA Low Byte Slot Data Bus or General Purpose I/O. When external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL, these pins are used as the GPIO pins for green control. Otherwise, these pins are SD[7:0]. No external LS245 is required.
SA[19:17]	O-Group A 12/12 mA	ISA Slot Address Bus A19-A17. These pins should connect to the ISA System Address Bus.
SA[16:0]	I/O Group A 12/12 mA	ISA Slot Address Bus A16-A0. These pins should connect to the ISA System Address Bus.
SBHEJ	I/O Group A 12/12 mA	ISA Byte High Enable. This pin should connect to the ISA System Byte High Enable pin.
LA[23:17]	I/O Group A 12/12 mA	ISA Latched Address Bus. They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.
ISA Bus Interface Unit :		
IO16J	I -Group A	ISA 16 Bit I/O Device Indicator. This is an input and will be driven by the device if the ISA I/O cycle is a 16-bit access.
M16J	I/O Group A 12/20 mA	ISA 16 Bit Memory Device Indicator. This pin will be driven by the device or by the M1533 if the ISA Memory cycle is a 16-bit access.

MEMRJ	I/O Group A 12/12 mA	ISA Memory Read. This signal is an output when the M1533 is the ISA Bus master, or an input during ISA master cycle.
MEMWJ	I/O Group A 12/12 mA	ISA Memory Write. This signal is an output when the M1533 is the ISA Bus master, or an input during ISA master cycle.
AEN	O-Group A 12/12 mA	ISA I/O Address Enable. This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.
IOCHRDY	I/O Group A 12/20 mA	ISA System Ready. This signal is an output during ISA master cycle, or an input when the M1533 is the ISA Bus master.
NOWSJ	I-Group A	ISA Zero Wait-State for Input. This input signal will terminate the CPU to ISA command instantly.
IOCHKJ	I-Group A	ISA Parity Error. M1533 will generate NMI to CPU when this signal is asserted.
SYSCLK	O-Group A 12/12 mA	ISA System Clock. This output is generated by the PCI clock and is used as the ISA system clock.
BALE	O-Group A 12/12 mA	Bus Address Latch Enable. BALE will be asserted throughout DMA, ISA master , and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.
IORJ	I/O Group A 12/16 mA	ISA I/O Read. This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
IOWJ	I/O Group A 12/12 mA	ISA I/O write. This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
SMEMRJ	O-Group A 12/12 mA	ISA System Memory Read. This signal indicates that the memory read command is below 1M Byte address.
SMEMWJ	O-Group A 12/12 mA	ISA System Memory Write. This signal indicates that the memory write command is below 1M Byte address.
DREQ[7:5], DREQ[3:0]	I-Group A Schmitt	DMA Request Signals. These are inputs from the DMA Device or ISA Master Request. The M1533 will combine the DMA request, ISA Master request, IDE Bus Master request, and USB Master request to generate the PHOLDJ to the PCI Arbiter.
DACKJ[7:5], DACKJ[3:0]	O-Group A 9.6/9.6 mA	DMA Acknowledge Signals. After the M1533 has got the PCI Bus grant (PHLDAJ), the internal arbiter will assert the DMA acknowledge signal to the DMA Device Request.
TC	O-Group A 12/12 mA	DMA End of Process. This signal will be asserted after the DMA Device has ended the transaction.
REFSHJ	I/O Group A 12/20 mA	ISA Refresh Cycle. This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
Miscellaneous Logic :		
SPKR	O-Group A 4/4 mA	Speaker Output. This pin is used to control the Speaker Output and should connect to the Speaker.

RTCAS	O-Group A 4/4 mA	RTC Address Strobe. This pin is used as the RTC Address Strobe and should connect to the RTC.
RTCRW	O-Group A 4/4 mA	RTC Write strobe. This pin is used as the RTC Read/Write Command and should connect to the RTC. The M1533 will drive the RTC command through dedicated pin instead of the 74F32 decode to save the system cost.
RTCDS	O-Group A 4/4 mA	RTC Data Strobe. This pin is used as the RTC Data Strobe and should connect to the RTC.
SPLED	O-Group A 4/4 mA	Speed LED Output. This pin is used to control the Speed LED Output and should connect to LED.
ROMKBCSJ	O-Group A 4/4 mA	ROM/Keyboard Chip Select. This pin is the ROM chip select and is the Keyboard chip select also when internal KBC is disabled.
SERIRQ/ GPI[2]	B/I Group A 12/16 mA	Serial Interrupt Request or General Purpose Input. This pin is used to support the serial interrupt protocol or as a General Purpose Input.
SIRQI	I-Group A Schmitt	Steerable IRQ Input1. This is a steerable Interrupt input, M1533 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
SIRQII	I-Group A Schmitt	Steerable IRQ Input2. This is a steerable Interrupt input, M1533 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
IRQ8J	I-Group C Schmitt	RTC Interrupt Input. This is the RTC Interrupt input. This pin belongs to the Power Group C, and it can support the RTC Alarm function during Soft-off or Suspend state.
XDIR/ GPO[12]	O-Group A 4/4 mA	XD Bus Direction Control or General Purpose Output. When external XD bus is designed on motherboard, this pin is X-bus direction control. Otherwise, this pin is a general purpose output.
KBINH/ IRQ1I	I/O Group A Schmitt 12/24 mA	Keyboard Inhibit or Interrupt One Input. This pin will be the Keyboard Inhibit input when internal KBC is enabled. Otherwise, it will be the IRQ1 input.
IRQ1O/ GPO[13]	O-Group A 4/4 mA	IRQ1 Output or General Purpose Output. When both external APIC and internal KBC are enabled, this pin is IRQ1 output. Otherwise, it is a general purpose output.
KBCLK/ GPI[9]	I/O Group A Schmitt 12/24 mA	Keyboard Clock or General Purpose Input. This pin is the Keyboard interface Clock when internal KBC is enabled. Otherwise, it is a general purpose input.
KBDATA/ GPI[10]	I/O Group A Schmitt 12/24 mA	Keyboard data or General Purpose Input. KB interface DATA output when internal KBC is enabled. Otherwise, this pin is a general purpose input.
MSCLK/ GPI[11]	I/O Group A Schmitt 12/24 mA	Mouse Clock or General Purpose Input. Mouse clock output when internal PS2 Keyboard is enabled. Otherwise, this pin is a general purpose input.

MSDATA/ IRQ12I	I/O Group A Schmitt 12/24 mA	Mouse Data or Interrupt Line 12 Input. Mouse data output when internal PS2 Keyboard is enabled. Otherwise, this pin is the IRQ12 input.
IRQ12O/ GPO[14]	O-Group A 4/4 mA	Interrupt Line 12 Output or General Purpose Output. When both external APIC and internal KBC are enabled, this pin is IRQ12 output. Otherwise, this pin is a general purpose output.
IRQ0/ GPO[15]	O-Group A 4/4 mA	Interrupt Line 0 Output or General Purpose Output. This pin is the Interrupt request 0 output when external APIC mode is enabled. Otherwise this pin is a general purpose output.
APICREQJ/ GPI[8]	I -Group A	APIC Request Input or General Input. This pin connects to the APIC Chip Request Line when external APIC mode is enabled. Otherwise, this pin is a general purpose input.
APICCSJ/ GPO[16]	O-Group A 4/4 mA	APIC Chip Select or General Purpose Output. This pin connects to the APIC Chip Select Line when external APIC mode is enabled. Otherwise, this pin is a general purpose output.
APICGNTJ/ GPO[17]	O-Group A 4/4 mA	APIC Grant Output or General Purpose Output. This pin connects to the APIC Chip Grant Line when external APIC mode is enabled. Otherwise, this pin is a general purpose output.
BIOSA17/ GPO[19]	O-Group A 4/4 mA	ROM Address 17 or General Purpose Output. This pin is the ROM A17 control when 2M ROM is used, or it is a general purpose output.
BIOSA16/ GPO[18]	O-Group A 4/4 mA	ROM Address 17 or General Purpose Output. This pin is the ROM A16 control when 2M ROM is used, or it is a general purpose output.
PCSJ/ GPO[0]	O-Group A 4/4 mA	Programmable Chip Select or General Purpose Output. This pin can be selected as a Programmable Chip Select, or as a general purpose output.
IDE interface :		
PIDE_DRQ	I-Group D	Primary IDE DMA Request for IDE Master. This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer.
SIDE_DRQ	I-Group D	Secondary IDE DMA Request for IDE Master. This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer.
PIDE_AKJ	O-Group D 9.6/9.6 mA	Primary IDE DACKJ for IDE Master. This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer.
SIDE_AKJ	O-Group D 9.6/9.6 mA	Secondary IDE DACKJ for IDE Master. This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer.
PIDE_RDY	I-Group D	Primary IDE Ready. This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
SIDE_RDY	I-Group D	Secondary IDE Ready. This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
PIDEIORJ	O-Group D 12/12 mA	Primary IDE IORJ Command. This is the IORJ command output pin to notify the Primary IDE device to assert the Read Data.
SIDEIORJ	O-Group D 12/12 mA	Secondary IDE IORJ Command. This is the IORJ command output pin to notify the Secondary IDE device to assert the Read Data.

PIDEIOWJ	O-Group D 12/12 mA	Primary IDE IOWJ Command. This is the IOWJ command output pin to notify the Primary IDE device that the available Write Data is already asserted by M1533.
SIDEIOWJ	O-Group D 12/12 mA	Secondary IDE IOWJ Command. This is the IOWJ command output pin to notify the Secondary IDE device that the available Write Data is already asserted by M1533.
PIDECS1J	O-Group D 9.6/9.6 mA	IDE Chip Select 1 for Secondary Channel 0. This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.
PIDECS3J	O-Group D 9.6/9.6 mA	IDE Chip Select 3 for Secondary Channel 1. This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
SIDECS1J	O-Group D 9.6/9.6 mA	IDE Chip Select 1 for Primary Channel 0. This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3J	O-Group D 9.6/9.6 mA	IDE Chip Select 3 for Primary Channel 1. This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
PIDE_A[2:0]	O-Group D 9.6/9.6 mA	Primary IDE ATA Address Bus. These are the Address pins connected to Primary Channel.
SIDE_A[2:0]	O-Group D 9.6/9.6 mA	Secondary IDE ATA Address Bus. These are the Address pins connected to Secondary Channel.
PIDE_D[15:0]	I/O Group D 9.6/9.6 mA	Primary IDE ATA Data Bus. These are the Data pins connected to Primary Channel.
SIDE_D[15:0]	I/O Group D 9.6/9.6 mA	Secondary IDE ATA Data Bus. These are the Data pins connected to Secondary Channel.
Power Management Unit :		
RSM_RSTJ	I-Group C Schmitt	Resume Circuit Initial Reset Input. This input is used to initialize the resume circuit.
SMIJ	O-Group E 4/4 mA	SMM Interrupt Output. This output should be connected to CPU SMM Interrupt input.
STPCLKJ	O-Group E 4/4 mA	Stop CPU Internal Clock Output. This output is used to stop the CPU internal clock and should be connected to CPU STPCLKJ input.
SLEEPJ/ GPO[20]	O-Group E 4/4 mA	Pentium PRO Sleep State or General Purpose Output. This output will force Pentium PRO CPU to enter Sleep State, or as a general purpose output.
ZZ/ GPO[1]	O-Group E 4/4 mA	PBSRAM Power Saving Mode or General Purpose Output. This output is used to control L2 cache entering power saving mode, or as a general purpose output.
CLKRUNJ	I/O - Group B 12/16 mA	PCI Clock Stop Message Control. This pin is used to support PCI Clock Run function.
CPU_STPJ/ GPO[2]	O-Group B 4/4 mA	Clock Cell CPU Clock Stop or General Purpose Output. This output is used to stop the CPU Clock of the clock generator, or as a general purpose output.
PCI_STPJ/ GPO[3]	O-Group B 4/4 mA	Clock Cell PCI Clock Stop or General Purpose Output. This output is used to stop the PCI Clock of the clock generator, or as a general purpose output.

SUSTAT1J	O-Group C 4/4 mA	Suspend Status for North Bridge. This output is used to notice the north bridge to control DRAM suspend refresh circuit.
SLOWDWN/ GPO[4]	O-Group B 4/4 mA	Slow Down the Clock Generator Output or General Purpose Output. This output is used to control the Clock Generator to slow down the clock output, or as a general purpose output.
AMSTATJ/ GPO[8]	O-Group B 4/4 mA	APM State Control. It is asserted when HALT or STPGNT cycle is detected.
PWRBTNJ	I-Group C Schmitt	Power Button Input. This input is used to support the ACPI Power Button function.
PCIREQJ/ GPI[3]	I-Group B	PCI Bus Request Event Input or General Purpose Input. This input comes from the North Bridge or external circuit to notice M1533 there is PCI request pending. This pin can also be programmed as a general purpose input.
POSSTA/ GPI[4]	I -Group A	Force M1533 into Suspend Mode or General Purpose Input. This input can be used to force M1533 entering suspend mode, or as a general purpose input.
SQWO/ GPO[9]	O-Group A 4/4 mA	Square Wave Output or General Purpose Output. This output can be used to output Square Wave with 1Hz or 2Hz, or as a general purpose output.
OFF_PWR0/ GPO[21]	O-Group C 4/4 mA	Remove Clock Generator Power Control or General Purpose Output. This output can be used to remove the Clock Generator Power, or as a general purpose output.
OFF_PWR1/ GPO[22]	O-Group C 4/4 mA	Remove All Circuit Power Except Internal Suspend Circuit and External DRAM or General Purpose Output.
OFF_PWR2/ GPO[23]	O-Group C 4/4 mA	Remove All Circuit Power Except Internal Suspend Circuit or General Purpose Output.
RI	I -Group C Schmitt	Ring-in or General Purpose Input. This input connects to Modem Ring-in input to support ACPI Ring-in function, or as a general purpose input.
LBJ	I -Group C Schmitt	First Battery Low Indication Input or General Purpose Input. This input can be used as the first stage battery low level indication, or as a general purpose input signal.
LLBJ	I -Group C Schmitt	Last Battery Low Indication Input or General Purpose Input. This input can be used as the last battery low level indication, or as a general purpose input signal.
EXTSW	I -Group A Schmitt	External Switch Event or General Purpose Input. EXTSW is a triggered input to the M1533 showing that an external device is requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
THRMJ	I -Group A Schmitt	Thermal Event Input or General Purpose Input. THRMJ is a triggered input to the M1533 showing that the external thermal detected circuits are requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
ACPWR	I - Group A Schmitt	Detect AC Adapter Plug-in or General Purpose Input. This is a triggered input showing that the AC adapter is plugged in or plugged out event. This triggered event can be used as a system management (or control) interrupt source. This signal also can be used optionally as a general purpose input signal.
CRT	I -Group A Schmitt	Detect CRT Connector Plug-in or General Purpose Input. This signal represents whether the external CRT connector is plugged in/ plugged out, or used as a general purpose input.
SETUPJ	I -Group A	Setup Switch Input or General Purpose Input. This signal can be used as a setup switch triggered input for generating the power management interrupt event, or as a general purpose input signal.

EJECT	I -Group A	External Eject SMIJ Trigger or General Purpose Input. This triggered input is used as an eject (undocking) event indicator, or as a general purpose input signal.
LID	I -Group C	Cover Switch Input or General Purpose Input. This signal is used to indicate if the system's lid is open or closed, or as a general purpose input.
HOTKEYJ	I -Group C Schmitt	Hot Key Press Event Input or General Purpose Input. This input signal is used to indicate a hot key press event occurred or not, or as a general purpose input.
DOCKJ	I-Group C	Docking Insert Event Input or General Purpose Input. This triggered input is used as a docking event indicator, or as a general purpose input signal.
VCSJ/ GPI[5]	I-Group A	VGA Activity Event Input or General Purpose Input. The VGA chip should set this signal to active low when an VGA memory access occurred. This active signal is used by the M1533 to reload the VGA monitor timer or to generate a system management event. This signal also can be used as a general purpose input.
FPVEE/ GPI[6]	I-Group A	LCD Back Light VEE Input or General Purpose Input. This signal is used by the M1533 to generate DISPLAY and a programmable CCFT signals. This signal also can be used as a general purpose input.
CCFT/ GPO[5]	O-Group A 4/4 mA	Back Light Control or General Purpose Output. This signal can be programmed to be a periodical wave controlled by the FPVEE signal or kept to static low level. This signal also can be used as a general purpose output.
DISPLAY/ GPO[6]	O-Group A 4/4 mA	LCD Display On/Off Control or General Purpose Output. This signal can be programmed to be a response controlled by the FPVEE signal, or it can also be used as general purpose output.
CONTRAST/ GPO[7]	O-Group A 4/4 mA	LCD Contrast Control or General Purpose Output. It is a 1KHz signal with programmable duty cycle and can be used to control LCD contrast. It can also be a general purpose output.
GPIORBJ/ GPO[10]	O-Group A 4/4 mA	Input Event Latching into External Buffers Command or General Purpose Output. This signal can be used as an external buffer(s) latching command for extended general inputs, or as a normal general purpose output signal.
GPIOWB/ GPO[11]	O-Group A 4/4 mA	Output Control Signal Latching into External Buffers Command or General Purpose Output. This signal can be used as an external buffer(s) latching command for extended general outputs, or as a normal general purpose output signal.
GPIO[19:16]	I/O Group C Schmitt 4/4 mA	General Purpose I/O Pins for Resume from Suspend Mode. These signals can be programmed as the inputs or outputs for the resume triggered events from the suspend mode.
GPIO[15:12]/ BATSEL[3:0]	I/O Group C Schmitt 4/4 mA	General Purpose I/O Pins or SM Bus Battery Select. These signals can be used as the general purpose I/O pins, or as the external SMB battery select control signals.
GPIO[11:8]	I/O Group A Schmitt 4/4 mA	General Purpose I/O Pins for Wake-up from Stand-by Mode. These signals can be programmed as the inputs or outputs for the wake-up triggered events from the standby mode.
USB interface :		
USBP0+ USBP0-	I/O Group B	Universal Serial Bus Port 0. These are the serial data pair for USB Port 0.

USBP1+ USBP1-	I/O Group B	Universal Serial Bus Port 1. These are the serial data pair for USB Port 1.
OVCRJ[1:0]/ GPI[1:0]	I -Group B	Over Current Detect Inputs or General Purpose Inputs. These two pins are used to monitor the USB Power Over Current, or as two general purpose inputs.
SM Bus signal :		
SMBEVENTJ/ GPI[7]	I-Group A Schmitt	SM Bus Resume Event or General Purpose Input. This signal can be used as the SM Bus resume event indicator, or as a general purpose input.
SMBCLK	I/O-Group C Schmitt 9.6/9.6 mA	SM Bus Clock. SM Bus clock signal should be combined with SM Bus data to carry information between the devices connected to the SM Bus.
SMBDATA	I/O-Group C Schmitt 9.6/9.6 mA	SM Bus Data Line. SM Bus data signal should be combined with SM Bus clock to carry information between the devices connected to the SM Bus.
Power Pins :		
VCC_A	P	Vcc 3.3V or 5V for Power Group A. This power is used for ISA interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power connects to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_3A	P	Vcc 3.3V for Power Group A. This power is used for ISA interface. If Vcc_A is selected as 3.3V, this power pin connects with Vcc_A to 3.3V power plane. If Vcc_A is selected as 5V, this power pin should connect to 3.3V power plane to save power consumption.
VCC_B	P	Vcc 3.3V for Power Group B. This power is used for PCI interface. It must be connected to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VCC_C	P	Vcc 3.3V or 5V for Power Group C. This power is used for resume/ suspend control interface signals during normal operation and suspend periods. If this power is connected to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power is connected to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_3C	P	Vcc 3.3V for Power Group C. This power is used for Resume/Suspend Control interface. If Vcc_C is selected as 3.3V, this power pin connects with Vcc_C to 3.3V power plane. If Vcc_C is selected as 5V, this power pin should connect to 3.3V power plane to save power consumption.
VCC_D	P	Vcc 3.3V or 5V for Power Group D. This power is used for IDE interface. If this power is connected to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power is connected to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_E	P	Vcc 3.3V or 2.5V for Power Group E. This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_5	P	Vcc 5.0V for core Power. It supplies the core power for the internal circuit except the suspend circuit.
VDD_5S	P	Vcc 5.0V for Suspend/Resume Core Power. It supplies the core power for the internal suspend/resume circuit.
Vss or Gnd	P	Ground.

2.2.4 Numerical Pin List

Pin No.	Pin Name	Pin Type
A1	--	--
A2	AD21	I/O
A3	AD18	I/O
A4	CBEJ2	I/O
A5	STOPJ	I/O
A6	AD14	I/O
A7	AD9	I/O
A8	AD5	I/O
A9	AD0	I/O
A10	SIDED7	I/O
A11	SIDED10	I/O
A12	SIDED2	I/O
A13	SIDED15	I/O
A14	SIDEAKJ	O
A15	SIDECS3J	O
A16	PIDED6	I/O
A17	PIDED10	I/O
A18	PIDED3	I/O
A19	--	-
A20	--	-
B1	--	-
B2	AD22	I/O
B3	AD19	I/O
B4	AD16	I/O
B5	DEVSELJ	I/O
B6	AD15	I/O
B7	AD10	I/O
B8	AD6	I/O
B9	AD1	I/O
B10	PHOLDJ	O
B11	SIDED5	I/O
B12	SIDED12	I/O
B13	SIDED0	I/O
B14	SIDERDY	I
B15	SIDECS1J	O
B16	PIDED9	I/O
B17	PIDED11	I/O

Pin No.	Pin Name	Pin Type
B18	PIDED13	I/O
B19	PIDED2	I/O
B20	PIDED14	I/O
C1	CBEJ3	I/O
C2	AD23	I/O
C3	AD20	I/O
C4	AD17	I/O
C5	TRDYJ	I/O
C6	CBEJ1	I/O
C7	AD11	I/O
C8	AD7	I/O
C9	AD2	I/O
C10	PHLDAJ	I
C11	SIDED9	I/O
C12	SIDED3	I/O
C13	SIDED14	I/O
C14	SIDEIORJ	O
C15	SIDEA2	O
C16	PIDED5	I/O
C17	PIDED4	I/O
C18	PIDED1	I/O
C19	PIDED15	I/O
C20	PIDED0	I/O
D1	AD26	I/O
D2	AD25	I/O
D3	AD24	I/O
D4	PCIRSTJ	O
D5	IRDYJ	I/O
D6	PAR	I/O
D7	AD12	I/O
D8	CBEJ0	I/O
D9	AD3	I/O
D10	CLKRUNJ	I/O
D11	SIDED6	I/O
D12	SIDED11	I/O
D13	SIDED1	I/O
D14	SIDEIOWJ	O
D15	SIDEA0	O
D16	PIDED8	I/O

Pin No.	Pin Name	Pin Type
D17	PIDED12	I/O
D18	PIDEA1	O
D19	PIDEA0	O
D20	PIDEA2	O
E1	AD29	I/O
E2	AD28	I/O
E3	AD27	I/O
E4	AD30	I/O
E5	FRAMEJ	I/O
E6	SERRJ	I
E7	AD13	I/O
E8	AD8	I/O
E9	AD4	I/O
E10	PCICLK	I
Pin no.	Pin name	Type
E11	SIDED8	I/O
E12	SIDED4	I/O
E13	SIDED13	I/O
E14	SIDEDRQ	I
E15	SIDEA1	O
E16	PIDED7	I/O
E17	PIDEAKJ	O
E18	PIDECS1J	O
E19	PIDECS3J	O
E20	INTR	O
F1	USBCLK	I
F2	GPO8	O
F3	AD31	I/O
F4	INTAJ	I
F5	INTBJ	I/O
F6	VCC	P
F14	VCC	P
F15	VCC	P
F16	PIDEIOWJ	O
F17	PIDERDY	I
F18	NMI	O
F19	SMIJ	O
F20	IGNNEJ	O
G1	USBP0-	I/O

Pin No.	Pin Name	Pin Type
G2	USBP0+	I/O
G3	GPO4	O
G4	INTCJ	I/O
G5	INTDJ	I/O
G6	VCC	P
G15	VCC	P
G16	PIDEDRQ	I
G17	PIDEIORJ	O
G18	CPURST	O
G19	A20MJ	O
G20	INIT	O
H1	USBP1-	I/O
H2	USBP1+	I/O
H3	GPI3	I
H4	GPO3	O
H5	GPO2	O
H8	GND	P
H9	GND	P
H10	GND	P
H11	GND	P
H12	GND	P
H13	GND	P
H16	IRQ13	I/O
H17	STPCLK	O
H18	SMBDATA	I/O
H19	SMBCLK	I/O
H20	RI	I
J1	SD7	I/O
J2	RSTDRV	O
J3	IOCHKJ	I/O
J4	GPI1	I
J5	GPI0	I
J8	GND	P
J9	GND	P
J10	GND	P
J11	GND	P
J12	GND	P
J13	GND	P
J16	GPO1	O

Pin No.	Pin Name	Pin Type
J17	GPO20	O
J18	GPIO19	I/O
J19	GPIO18	I/O
J20	GPIO17	I/O
K1	SD5	I/O
K2	IRQ9	I/O
K3	SD6	I/O
K4	MSCLK	O
K5	MSDATA	I/O
K8	GND	P
K9	GND	P
K10	GND	P
K11	GND	P
K12	GND	P
K13	GND	P
K16	LLBJ	I
K17	DOCKJ	I
K18	GPIO16	I/O
K19	GPIO15	I/O
K20	GPIO14	I/O
L1	SD3	I/O
L2	DREQ2	I
L3	SD4	I/O
L4	KBCLK	I/O
L5	KBDATA	I/O
L8	GND	P
L9	GND	P
L10	GND	P
L11	GND	P
L12	GND	P
L13	GND	P
L16	IRQ8J	I
L17	SUSTAT1J	O
L18	PWRBTNJ	I
L19	GPIO13	I/O
L20	GPIO12	I/O
M1	IOCHRDY	I/O
M2	SD0	I/O
M3	SD1	I/O

Pin No.	Pin Name	Pin Type
M4	NOWSJ	I
M5	SD2	I/O
M8	GND	P
M9	GND	P
M10	GND	P
M11	GND	P
M12	GND	P
M13	GND	P
M16	PWG	I
M17	HOTKEYJ	I
M18	RSMRSTJ	I
M19	LBJ	I
M20	LID	I
N1	IOWJ	I/O
N2	SA19	O
N3	SMEMRJ	O
N4	AEN	O
N5	SMEMWJ	O
N8	GND	P
N9	GND	P
N10	GND	P
N11	GND	P
N12	GND	P
N13	GND	P
N15	VDD5S	P
N16	SIRQI	I
N17	SIRQII	I
N18	OSC32KII	I
N19	OSC32KI	I
N20	OSC32KO	O
P1	SA16	I/O
P2	DACKJ3	O
P3	SA17	O
P4	IORJ	I/O
P5	SA18	O
P6	VCC	P
P15	VCC	P
P16	GPO19	O
P17	GPO18	O

Pin No.	Pin Name	Pin Type
P18	GPO23	O
P19	GPO22	O
P20	GPO21	O
R1	DREQ1	I
R2	SA14	I/O
R3	DACKJ1	O
R4	SA15	I/O
R5	DREQ3	I
R6	VDD5	P
R7	VCC	P
R14	VCC	P
R15	VCC	P
R16	GPO17	O
R17	GPO16	O
R18	GPO15	O
R19	GPO14	O
R20	GPO13	O
T1	REFSHJ	I/O
T2	SA13	I/O
T3	IRQ6	I/O
T4	IRQ4	I/O
T5	DACKJ2	O
T6	BALE	O
T7	LA23	I/O
T8	LA20	I/O
T9	DACKJ0	O
T10	MEMWJ	I/O
T11	DREQ6	I
T12	ROMKBCSJ	O
T13	RTCAS	O
T14	RTCRW	O
T15	IRQ1I	I/O
T16	GPO12	O
T17	GPO11	O
T18	GPO10	O
T19	GPO9	O
T20	GPO7	O
U1	SA12	I/O
U2	IRQ7	I/O

Pin No.	Pin Name	Pin Type
U3	IRQ5	I/O
U4	IRQ3	I/O
U5	TC	O
U6	OSC14M	I
U7	IRQ10	I/O
U8	IRQ15	I/O
U9	LA17	I/O
U10	DREQ5	I
U11	SD10	I/O
U12	SD12	I/O
U13	RTCDS	O
U14	XD0	I/O
U15	XD4	I/O
U16	EJECT	I
U17	GPIO11	I/O
U18	GPO6	O
U19	GPO5	O
U20	GPO0	O
V1	SYSCLK	O
V2	SA10	I/O
V3	SA8	I/O
V4	SA5	I/O
V5	SA2	I/O
V6	M16J	I/O
V7	LA22	I/O
V8	LA19	I/O
V9	DREQ0	I
V10	SD8	I/O
V11	DACKJ7	O
V12	SD13	I/O
V13	SPKR	O
V14	XD1	I/O
V15	XD5	I/O
V16	ACPWR	I
V17	GPI6	I
V18	GPIO8	I/O
V19	GPIO9	I/O
V20	GPIO10	I/O
W1	SA11	I/O

Pin No.	Pin Name	Pin Type
W2	SA9	I/O
W3	SA7	I/O
W4	SA4	I/O
W5	SA1	I/O
W6	SBHEJ	I/O
W7	IRQ11	I/O
W8	IRQ14	I/O
W9	MEMRJ	I/O
W10	DACKJ6	O
W11	SD11	I/O
W12	SD14	I/O
W13	SPLED	O
W14	XD2	I/O
W15	XD6	I/O
W16	SETUPJ	I
W17	GPI4	I
W18	GPI7	I
W19	GPI8	I
W20	--	-
Y1	--	-
Y2	--	-
Y3	SA6	I/O
Y4	SA3	I/O
Y5	SA0	I/O
Y6	IO16J	I
Y7	LA21	I/O
Y8	LA18	I/O
Y9	DACKJ5	O
Y10	SD9	I/O
Y11	DREQ7	I
Y12	SD15	I/O
Y13	EXTSW	I
Y14	XD3	I/O
Y15	XD7	I/O
Y16	THRMJ	I
Y17	CRT	I
Y18	GPI2	I
Y19	GPI5	I
Y20	--	-

2.3. ATI 264GT

The *mach64* 3D RAGE™ (also known as the GT) is a 208-pin VLSI video graphics controller chip with built-in 3D coprocessor, GUI coprocessor, video scaler, color space converter, true-color palette DAC, and dual-clock synthesizer. This controller is 100% register-compatible with the IBM VGA display adapter.

The GT supports synchronous graphics memory chips SDRAM/SGRAM. When combined with the 64-bit memory interface and memory clocks up to 63 MHz, the available bandwidth can reach 800 MB/sec. This increase in memory bandwidth allows for greater display resolutions and uncompromising video playback capabilities. The GT also supports DRAM and EDO DRAM.

Both footprint and pinout of the GT are backward compatible with the ATI-264CT (CT) and ATI-264VT (VT).

2.3.1 Features

2.3.1.1 3D Accelerator

- Complete 3D primitives - Points, Lines, Triangles, Trapezoids, and Rectangles
- Full-screen or window double buffering for smooth animation
- Flat and Gouraud shading
- Dithering down from 24 bits per pixel (bpp) to 8 or 16 bpp 3D engine for smaller memory foot print
- Texture mapping
    - Hardware perspective correction
    - Sub-pixel accuracy
    - Mip-mapping
    - Bi-linear and tri-linear filtering
    - Texture maps up to 1024 x 1024
    - Non-square texture maps
    - Alpha in texture map
    - Video textures using YUV format
- 3D effects
    - Alpha blending and alpha interpolation
    - Fogging and fog interpolation

- Texture lighting modes

- 3D modes
    - ARGB32 (8:8:8:8)
    - ARGB16 (1:5:5:5)
    - RGB16 (5:6:5)
    - RGB8 (3:3:2)
    - Y8 grey scale
    - ARGB16 (4:4:4:4)
    - YUV444, YUV422

2.3.1.2 2D Accelerator

- Hardware acceleration - Rectangle Fill, Line Draw, BitBlt, Polygon Fill, Panning/Scrolling, Bit Masking, Monochrome Expansion, Scissoring, and full ROP support

- Hardware cursor up to 64 x 64 x 2

- Acceleration provided in 4/8/16/24/32-bpp modes. Packed pixel support (24 bpp) enables true color in 1-MB configuration

- Game acceleration for Microsoft's DirectDraw-Double Buffering, Virtual Sprites, Transparent Blit, Masked Blit, and Context Chaining

2.3.1.3 Video Accelerator

- Filtered horizontal and vertical scalers for TV-quality, full-screen video playback

- Integrated video line buffers support filtered video scaling

- Color interpolation during scaling for improved high resolution video quality

- YUV to RGB color space conversion with support for both packed and planar

- Graphics and video keying for effective overlay of video and graphics

- AMC supports I^2C interface for special applications (i.e., video tuner control)

- Supports ATI Media Channel (AMC) 1.0 for additional video expansion capabilities

- Support for 26-pin VESA compatible VGA Feature Connector (VFC) with a 1024 x 768 maximum resolution capability

2.3.1.4 General Features

- First graphics controller to integrate 3D, 2D, and Video accelerators with palette DAC and dual-clock synthesizer in a single chip
- 24-bit, true-color palette DAC
    - Supports pixel clock rates to 1280 x 1024 resolution at 75-Hz refresh
    - Gamma correction for true WYSIWYG color
    - Full 24-bit palette
- PCI Revision 2.0 bus for Plug-and-Play ease of use
- Bi-endian support for compliance on a variety of processor platforms
- 32-level command FIFO assures fast response to host command transfers for maximum CPU/host bus/controller efficiency and concurrent operation
- Software interface including:
    - Programmable flat- or paged-memory model with enhanced host access to a linear frame buffer
    - 32-bit wide read/writable memory mapped registers with optimized organization to reduce instruction overhead and raises performance
- DDCI and DDC2B Plug-and-Play monitor support
- Power management for full-VESA Display Power Management Signaling (DPMS) and EPA Energy Star compliance. Also, register support for controller power reduction and DAC power down
- Optional EEPROM for storing user-selectable configurations
- Single-chip solution in 208-pin PQFP package, 0.511m, mixed 3.3V/5.0V
- Supports Fast Page Mode DRAM and EDO DRAM at up to 63 MHz memory clock across a 64-bit memory interface
- 3D driver support
    - Microsoft Direct 3D including support for Reality Lab and OpenGL
    - Apple QuickDraw 3D and TinselTown 3D interface
    - ATI 3D RAGE DOS and Windows API
    - Intel 3DR
- Easy-to-use Windows utilities

2.3.2 Block Diagrams

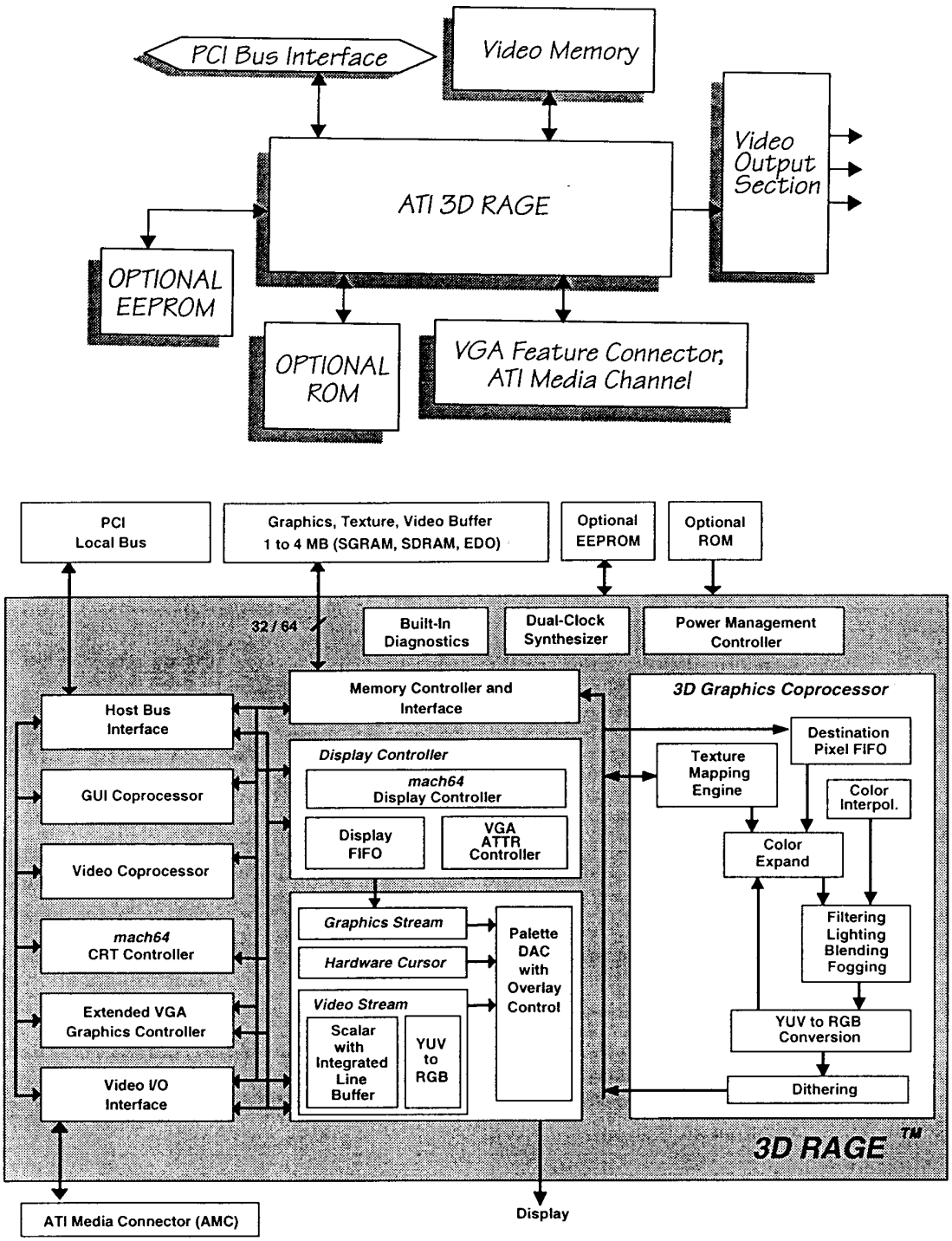


Figure 2-3 ATI 264GT Block Diagrams

2.3.3 Pin Diagram

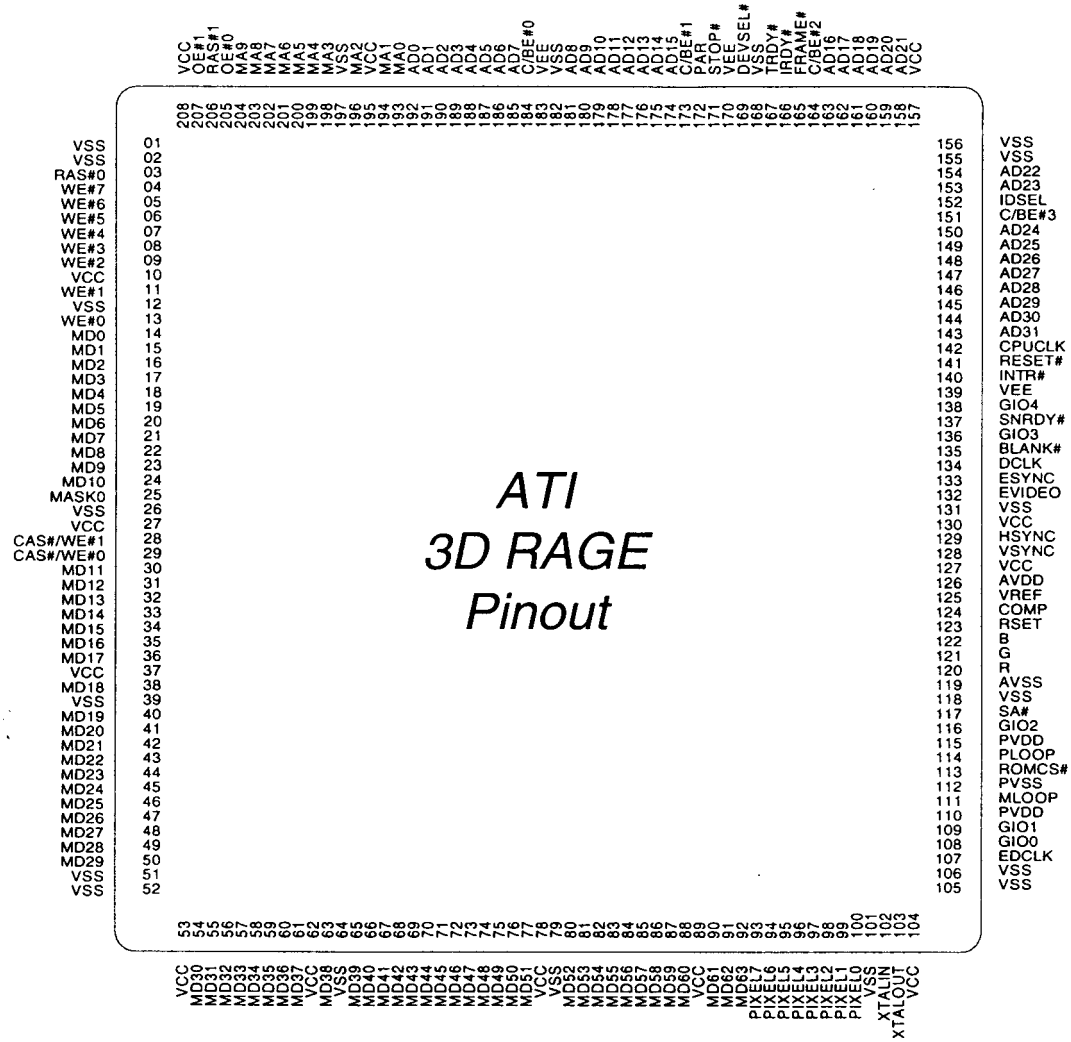


Figure 2-4 ATI 264GT Pin Diagram

2.3.4 Signal Descriptions

Table 2- 2 Signal Type Definitions

Signal Type	Definition
O	Output pin
1/0	Bidirectional pin
Pwr	Power pin
Gnd	Ground pin
A	Analog pins
#	Active-low signal

Table 2- 3 ATI 264GT Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface Implementation (for 5V PCI interface support)			
AD[31 :0]	143:150, 153:154, 158:163, 174:181, 185:192	I/O	Multiplexed-System Address or Data bits [31:0]
C/BE#[3:0]	151,164, 173,184	I	Multiplexed-Bus Command or Byte Enable bits 3:0. (BE# is active low)
CPUCLK	142	I	Bus Clock
DEVSEL#	169	O	Device Select indicates that the controller has decoded its address.
FRAME#	165	I	Frame is driven by the current bus master to indicate the beginning and duration of an access.
IDSEL	152	I	Initialization Device Select is used as a chip select during configuration read and write transactions.
INTR#	140	O	Interrupt Request-Level is triggered active low by default
IRDY#	166	I	Initiator Ready indicates that the bus master is able to complete the current data phase of the transaction
PAR	172	O	Parity. Even parity used
RESET#	141	I	Bus Reset
STOP#	171	O	Stop indicates the current target is requesting the master to stop the current transaction.
TRDY#	167	O	Target Ready indicates that the target agent is able to complete the current data phase of the transaction.
Signal	**Pin**	**Type**	**Description**
Memory Interface			
CAS#/WE#0	29	O	Write Strobe of the first and second MB of memory
CS#3/WE#1	28	O	Write Strobe of the third and fourth MB of memory
MA[9:0]	204:198, 196, 194:193	O	Memory Address bits 9:0

Table 2- 3 ATI 264GT Signal Descriptions

MD[31 :0]	55:54, 50:40, 38, 36:30, 24:14,	I/O	Memory Data bits 31:0 of the first and third MB of memory
MD[63:32]	92:90, 88:80, 77:65, 63, 61:56	I/O	Memory Data bits 63:32 of the second and fourth MB of memory.
OE#0	205	O	Output Enable of the first and second MB of memory
OE#1	207	O	Output Enable of the third and fourth MB of memory
RAS#0	3	O	Row Address Strobe of the first and second MB of memory
CS#2	206	O	Row Address Strobe of the third and fourth MB of memory
WE#[7:0]	4:9,11, 13	I/O	Column Address Strobe
SDRAM Memory 128KBx16x2, and x32x2			
CAS#/WE# [1 :0]	28,29	O	CAS[1:0]
MA[9:0]	204:198, 196,194, 193	O	MA[9:0]
MD[63:0]	92:90, 88:80, 77:65, 63, 61 :54, 50:40, 38, 36:30, 24:14	I/O	AD[63:0]
OE#1	205	O	WE# Command
OE#0	207	O	MCLK
RAS#[1:0]	3, 206	O	RAS[1:0]
WE#[7:0]	4:9,11, 13	O	DQM[7:0]
DAC and Monitor Interface			
R	120	A	Red analog pixel data output to monitor
G	121	A	Green analog pixel data output to monitor
B	122	A	Blue analog pixel data output to monitor
COMP	124	A	Compensation pin for the DAC
HSYNC	129	O	Horizontal sync
VSYNC	128	O	Vertical sync
RSET	123	A	Current setting resistor for the DAC
VREF	125	A	DAC reference voltage
Frequency Synthesizer Interface			
MLOOP	111	A	Memory Clock Loop filter
PLOOP	114	A	Pixel Clock Loop filter
XTALIN*	102	A	14.31818-MHz crystal or TTL oscillator connection
XTALOUT*	103	A	14.31818-MHz crystal connection

* For designs using external clock source (instead of a crystal): the input XTALIN is CMOS inverter with Cjn = 0.5pF, and XTALOUT is not connected.

Table 2- 3 ATI 264GT Signal Descriptions

Optional ATI Media Channel Interface			
BLANK#	135	0	Blank signal
DCLK	134	0	Pixel Clock output
EDCLK	107	I	Enable Pixel clock
ESYNC	133	I	Enable Sync
EVIDEO	132	I	Enable Pixel data
PIXEL[7:0]	93:100	0	Pixel data output
SA#	117	I/O	Serial I/O, Interrupt Request
137		I/O	Slave not ready
MASKO	25	I/O	Pixel mask
Optional EEPROM Interface			
Gl01	109	I/O	EEPROM clock
Gl02	116	I/O	EEPROM data I/O
Gl03	136	0	EEPROM chip select
MD [46:32]	72:65, 63, 61:56	I/O	EPROM address bus
MD [63:56]	92:90, 88:84	I/O	EPROM data bus
ROMCS#	113	O	ROM chip select
Optional EEPROM Interface (Monitor ID for DDC Support)			
GlO0	108	I/O	DDC serial data
Gl04	138	I/O	DDC serial clock
Power and Ground Pins			
AVDD	126	PWR	DAC analog power
AVSS	119	GND	DAC analog ground
PVDD	110, 115	PWR	PLL power
PVSS	112	GND	PLL ground
VCC	10,27, 37,53, 62,78, 127,130, 157,195, 208	PWR	3.3V power
Power and Ground Pins			
VEE	139,170, 183	PWR	5.0V power
VSS	1,2,12, 26,39, 51,52, 64,79, 101,105, 106,118, 131,155, 156,168, 182,197	GND	Ground

2.4. µPD481850 SGRAM

The mPD481850 is a synchronous graphics memory (SGRAM) organized as 131,072 words x 32 bits x 2 banks random access port.

This device can operate up to 100 MHz by using synchronous interface. Also, it has 8-column Block Write function to improve capability in graphics system.

This product is packaged in 100-pin plastic QFP (14 ´ 20 mm).

2.4.1 Features

- 131,072 words x 32 bits x 2 banks memory
- Synchronous interface (Fully synchronous DRAM with all input signals are latched at rising edge of clock)
    - Pulsed interface
    - Automatic precharge and controlled precharge commands
    - Ping-pong operation between the two internal memory banks
    - Up to 100 MHz operation frequency
- Possible to assert random column address in every cycle
- Dual internal banks controlled by A9 (Bank Address: BA)
- Byte control using DQM0 to DQM3 signals both in read and write cycle
- 8-column Block Write (BW) function
- Persistent write per bit (WPB) function
- Wrap sequence: Sequential
- Programmable burst length (1, 2, 4, 8 and full page)
- Programmable CAS# latency (2 and 3)
- Power Down operation and Clock Suspend operation
- Auto refresh (CBR refresh) or self refresh capability
- Single 3.3 V ± 0.3 V power supply

- LVTTL compatible inputs and outputs
- 100-pin Plastic QFP (14 ´ 20 mm)
- 1,024 refresh cycles/16 ms
- Burst termination by Precharge command
- Burst termination by Burst stop command (in case of full-page burst)

2.4.2 Block Diagram

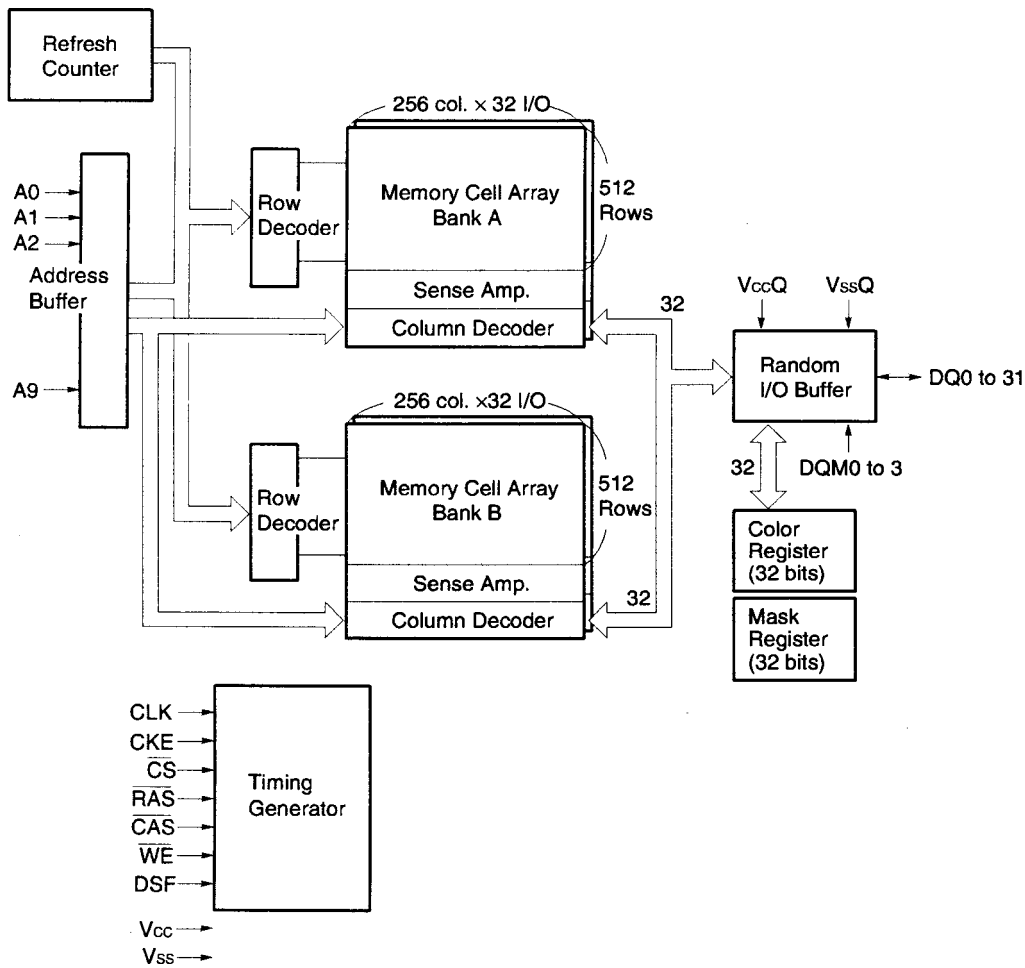


Figure 2- 1 µPD481850 Block Diagram

2.4.3 Pin Diagram

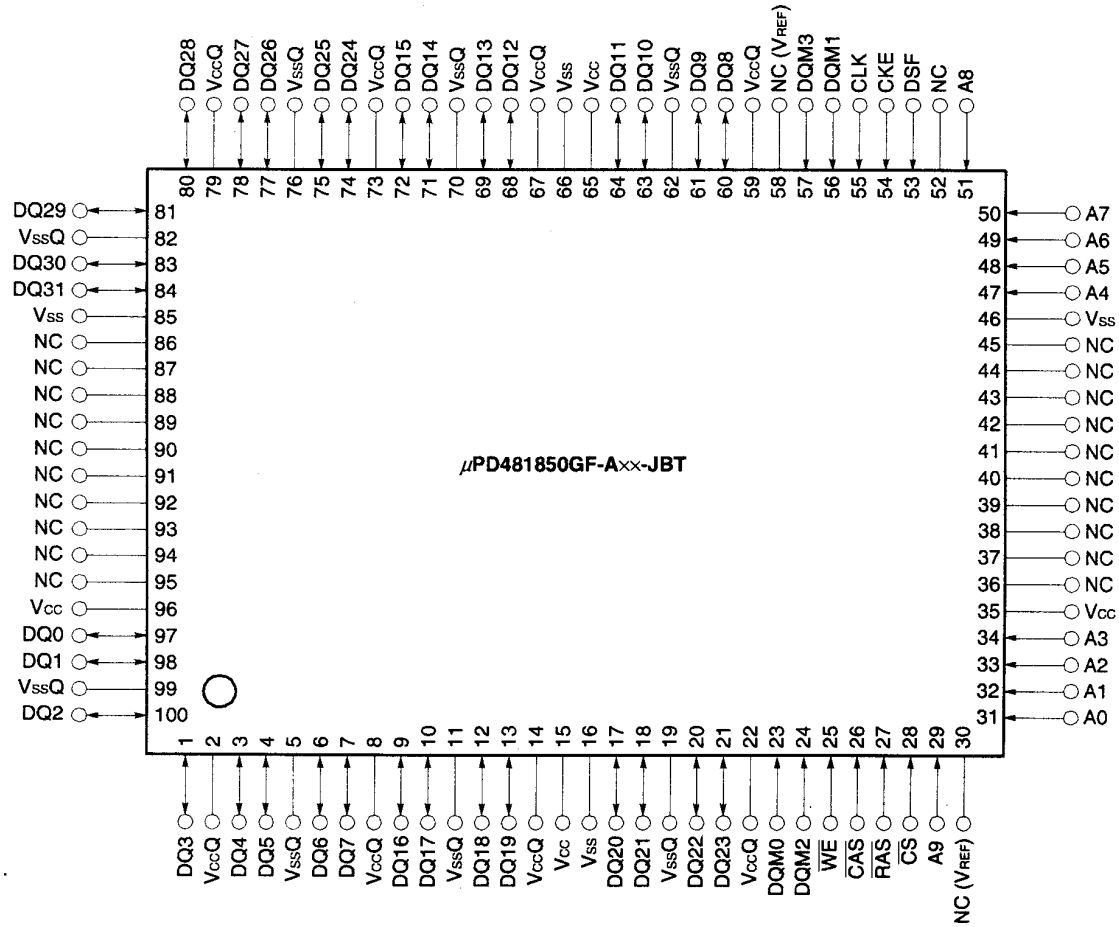


Figure 2- 2 μPD481850 Pin Diagram

2.4.4 Signal Descriptions

Table 2- 4 μPD481850 Signal Descriptions

Signal	Pin	Type	Pin Descriptions
CLK	55	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE	54	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the μPD481850 suspends operation. When the mPD481850 is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low. In Self refresh mode, low level on this pin is also used as part of the input command to specify Self refresh.
CS#	28	Input	CS# low starts the command input cycle. When CS# is high, commands are ignored but operations continue.
RAS#, CAS#, WE#	27, 62, 25	Input	RAS#, CAS# and WE# have the same symbols on conventional DRAM but different functions. For details, refer to the command table.
DSF	53	Input	DSF is part of the inputs of graphics command of the μPD481850. If DSF is inactive (Low level), mPD481850 operates as same as SDRAM.
A0 - A8	31-34, 47-50	Input	Row Address is determined by A0 - A8 at the CLK (clock) rising edge in the activate command cycle. Column Address is determined by A0 - A7 at the CLK rising edge in the read or write command cycle. A8 defines the precharge mode. When A8 is high in the precharge command cycle, both banks are precharged; when A8 is low, only the bank selected by A9 is precharged. When A8 high in read or write command cycle, the precharge start automatically after the burst access.
A9	29	Input	A9 is the bank address signal (BA). In command cycle, A9 low selects bank A and A9 high selects bank B.
DQM0 - DQM3	23, 56, 24, 57	Input	DQM controls I/O buffers. DQM0 corresponds to the lowest byte (DQ0 to DQ7), DQM1 corresponds to DQ8 to DQ15, DQM2 corresponds to DQ16 to DQ23. DQM3 corresponds to DQ24 to DQ31. In read mode, DQM controls the output buffers like a conventional OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the

Table 2- 4 µPD481850 Signal Descriptions

Signal	Pin	Type	Pin Descriptions
			read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ31	97, 98, 100, 1, 3, 4, 6, 7, 60, 61, 63, 64, 68, 69, 71, 72, 9, 10, 12, 13, 17, 18, 20, 21, 74, 75, 77, 78, 80, 80, 83, 84	Input/ Output	DQ pins have the same function as I/O pins on a conventional DRAM. These are normally 32-bit data bus and are used for inputting and outputting data. Function as the mask data input pins in the special register set command. Write operations can be performed after Active command with WPB (old mask data). Functions as the column selection data input pin in the block write cycle.
VCC VSS $V_{CC}Q$ $V_{SS}Q$	15, 35, 65, 97 16, 46, 66, 85 2, 8, 14, 22, 59, 73, 79 5, 11, 19, 62, 70, 76, 82, 99	(Power supply)	VCC and VSS are power supply pins for internal circuits. VCCQ and VSSQ are power supply pins for the output buffers.
N.C.	30, 36-45, 52, 58, 86-95		Non-connected

2.5. SMC 37C93xAPM

The SMC 37C93xAPM is an advanced high-performance multi-mode parallel port super I/O floppy disk controller.

2.5.1 Features

- Compatible with ISA Plug-and-Play standard (version 1.0a)
- 8042 keyboard controller
    - 2-K Proqram ROM
    - 256-byte Data RAM
    - Asynchronous access to two data registers and one status register
    - Supports interrupt and pollinq access
    - 8-bit timer counter
- Real time clock
    - MC146818 and DS1287 compatible
    - 256 bytes of battery-backed CMOS in two banks of 128 bytes
    - 128 bytes of CMOS RAM lockable in 4 x 32 byte blocks
    - 12 and 24-hour time format
    - Binary and BCD format
    - <1µa standby current (typ)
- Intelligent auto-power management
- 2.88-MB super I/O floppy disk controller
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - Three DMA options
    - Licensed CMOS 765B floppy disk controller
    - Advanced digital data separator
    - Software and register compatible with SMC's proprietary 82077AA compatible core
    - Sophisticated Power Control Circuitry (PCC) including multiple power-down modes for reduced power consumption
    - Game port select logic
    - Directly supports two floppy drives
    - 24-mA AT bus drivers

- Low-power CMOS design

- Licensed CMOS 765B floppy disk controller core
    - Supports vertical recording format
    - 16-byte data FIFO
    - 100% IBM compatibility
    - Detects all overrun and underrun conditions
    - 48-mA drivers and Schmitt Trigger inputs
    - DMA enable logic
    - Data rate and drive control registers
- Enhanced digital data separator
    - Low-cost implementation
    - No filter components required
    - 2-Mbps, 1-Mbps, 500-Kbps, 300-Kbps, 250-Kbps data rates
    - Programmable pre-compensation modes
- Serial ports
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - 2 high-speed NS16C550 Compatible UARTs with send/receive 16-byte FIFOs
    - Programmable baud rate generator
    - Modem control circuitry including 230-K and 460-K baud
    - IrDA, HP-SIR, ASK-IR support
- IDE interface
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - 6 DMA options
    - 2-channel/4-drive support
    - On-chip decode and select logic compatible with IBM PC/XT and PC/AT embedded hard disk drives
- Multi-mode parallel port with ChiProtect
    - Relocatable to 480 different addresses

2.5.2 Block Diagram

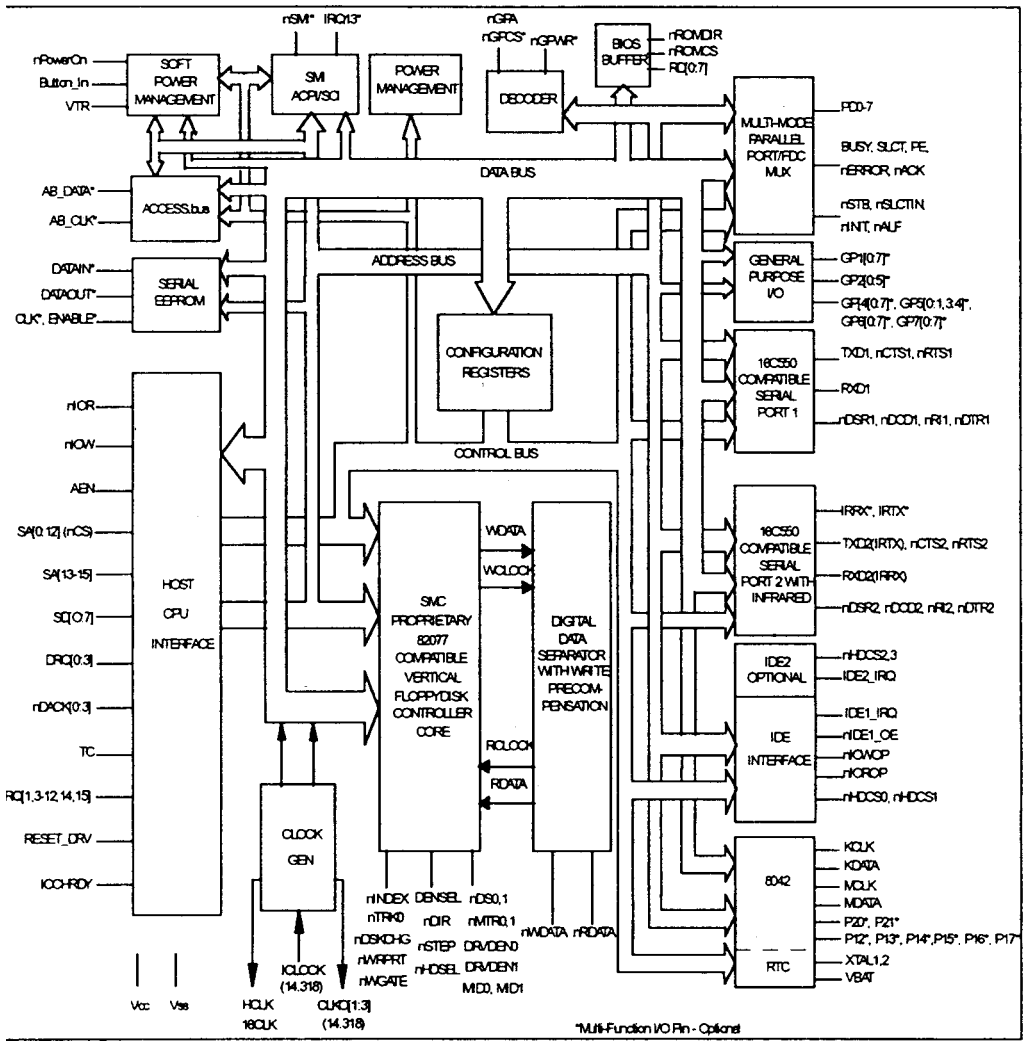


Figure 2-6 SMC 37C93xAPM Block Diagram

2.5.3 Pin Diagram

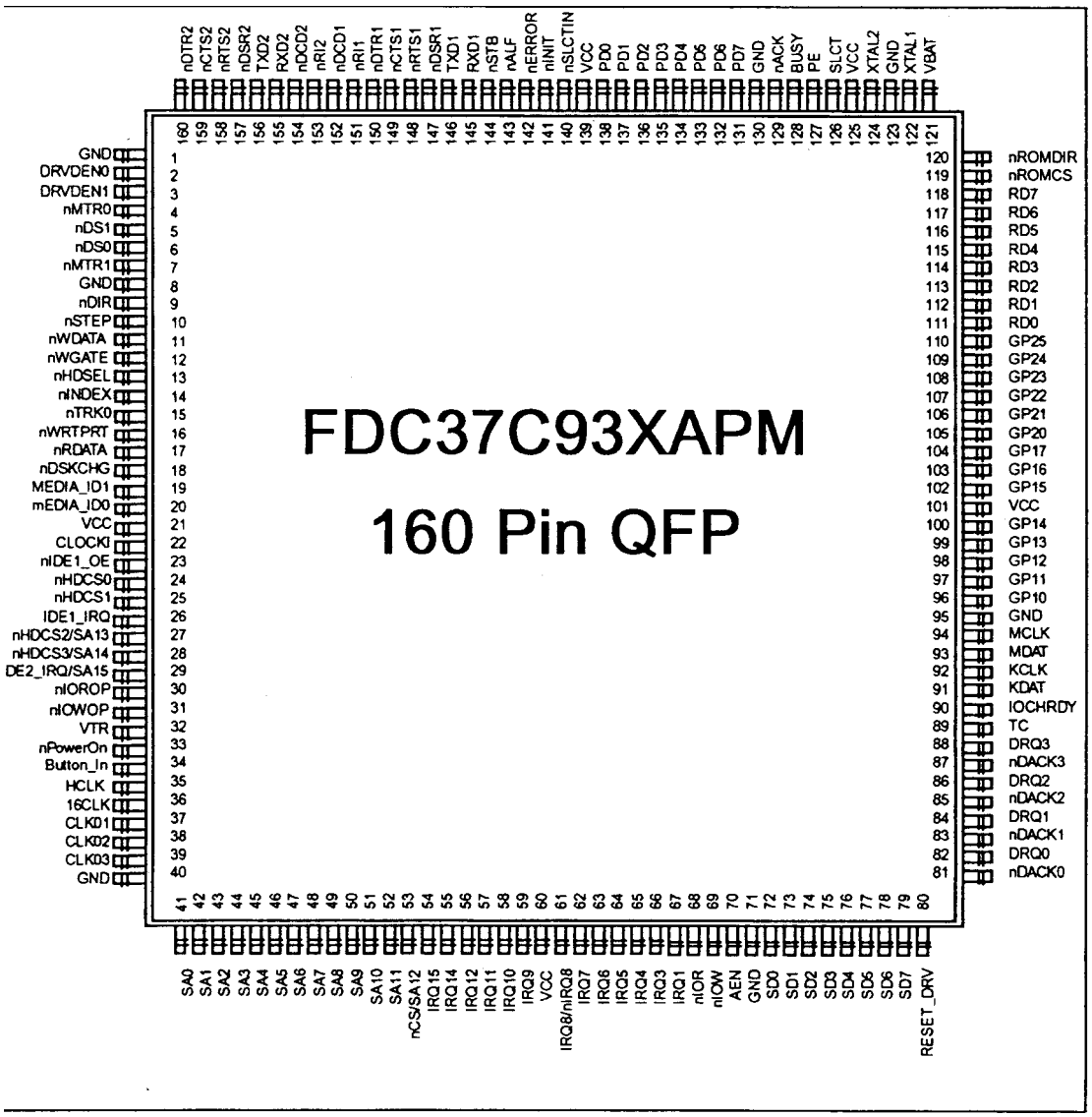


Figure 2-7 SMC 37C93xAPM Pin Diagram

2.5.4 Signal Descriptions

Table 2- 5 SMC 37C93xAPM Signal Descriptions

Signal	Pin	Type	Description
Host Processor Interface			
SD0 - SD7	72:79	I/O24	System Data Bus
SA0 - SA11	41:52	I	System Address Bus
CS#	53	I	Chip Select / SA12
AEN	70	I	Address Enable
IOCHRDY	90	OD24	I/O Channel Ready
RESET_DRV	80	IS	Reset Drive
IRQ[1, 3:12, 14, 15]	67:61, 59:54	OD24	Interrupt Requests
DRQ[0:3]	82,84,86,88	O24	DMA Request
DACK[0:3]#	81, 83, 85, 87	I	DMA Acknowledge
TC	89	I	Terminal Count
IOR#	68	I	I/O Read
IOW#	69	I	I/O Write
16CLK	36	O8SR	16MHz Out
CLOCKI	22	ICLK	14.318MHz Clock Input
CLOCK1	37	O8SR	14.318MHz Clock Output 1
CLOCK2	38	O8SR	14.318MHz Clock Output 2
CLOCK3	39	O8SR	14.318MHz Clock Output 3
Floppy Drive Interface			
RDATA#	17	IS	Read Disk Data
WGATE#	12	OD48	Write Gate
WDATA#	11	OD48	Write Data
HDSEL#	13	OD48	Head Select (1 = side 0)
DIR#	9	OD48	Direction Control (1 = out)
STEP#	10	OD48	Step Pulse
DSKCHG#	18	IS	Disk Change
DS[0:1]#	5,6	OD48	Drive Select 0, 1
MTR[0:1]#	7,4	OD48	Motor on Lines
WPROT#	16	IS	Write Protected
TR0#	15	IS	Track 00
INDEX#	14	IS	Index Pulse Input
DRVDEN[1:0]	3,2	OD48	Drive Density Select [1:0]
MID[1:0]	19,20	IS	Media ID Inputs
Serial Port Interface			
RXD1, RXD2	145, 155	I	Receive Data
TXD1, TXD2	146, 156	O4	Transmit Data
RTS1#, RTS2#	148, 158	O4	Request to Send
Serial Port Interface			
CTS1#, CTS2#	149, 159	I	Clear to Send

Table 2- 5 SMC 37C93xAPM Signal Descriptions

Signal	Pin	Type	Description
DTR1#, DTR2#	150, 160	O4	Data Terminal Ready
DSR1#, DSR2#	147, 157	I	Data Set Ready
DCD1#, DCD2#	152, 154	I	Data Carrier Select
RI1#, RI2#	151, 153	I	Ring Indicator
Parallel Port Interface			
PD0-PD7	138:131	I/OP24	Port Data
SLCTIN#	140	OD24/OP24	Printer Select
INIT#	141	OD24/OP24	Initiate Output
ALF#	143	OD24/OP24	Auto Line Feed
STB#	144	OD24/OP24	Strobe Signal
BUSY	128	I	Busy Signal
ACK#	129	I	Acknowledge Handshake
PE	127	I	Paper End
SLCT	126	I	Printer Selected
ERROR#	142	I	Error at Printer
IDE			
IDE1_OE#	23	O4	IDE1 Enable
HDCS0#	24	O24	IDE1 Chip Select0
HDCS1#	25	O24	IDE1 Chip Select1
IOROP#	30	O24	IOR Output
IOWOP#	31	O24	IOW Output
A[2:0]	32:34	O24	Address [2:0] Output
IDE1_IRQ	26	I	IDE Interrupt Request
HDCS2	27	O24	IDE2 Chip Select 2 / SA13
HDCS3	28	O24	IDE2 Chip Select 3 / SA14
IDE2_IRQ	29	I	IDE2 Interrupt Request / SA15
Real Time Clock			
XTAL1	122	ICLK	32-KHz Crystal Input
XTAL2	124	OCLK	32-KHz Crystal Output
Vbat	121		Battery Voltage
Keyboard / Mouse			
KDAT	91	I/OD16P	Keyboard Data
KCLK	92	I/OD16P	Keyboard Clock
MDAT	93	I/OD16P	Mouse Data
Keyboard / Mouse			
MCLK	94	I/OD16P	Mouse Clock
Soft Power Management Interface			
PowerOn#	33	I/O24	Power On

Table 2- 5 SMC 37C93xAPM Signal Descriptions

Signal	Pin	Type	Description
Button_In	34	I/O24	Button Input
General Purpose I/O			
GP10	96	I/O4	IRQ In
GP11	97	I/O4	IRQ In
GP12	98	I/O4	WD Timer Output / IRRX
GP13	99	I/O24	Power LED Output / IRTX
GP14	100	I/O4	GPI/O, General Purpose Read Strobe
GP15	102	I/O4	GPI/O, General Purpose Write Strobe
GP16	103	I/O4	GPI/O, Joystick Read Strobe / JOYCS
GP17	104	I/O4	GPI/O, Joystick Write Strobe
GP20	105	I/O4	GPI/O, IDE2 Output Enable
GP21	106	I/O4	GPI/O, Serial EEPROM Data In
GP22	107	I/O4	GPI/O, Serial EEPROM Data Out
GP23	108	I/O4	GPI/O, Serial EEPROM Clock
GP24	109	I/O4	GPI/O, Serial EEPROM Enable
GP25	110	I/O4	GPI/O, 8042 P21
BIOS Buffers			
RD[0:7]	111:118	I/O4	ROM Bus (I/O to the SD bus)
DOMCS#	119	I	ROM Chip Select (only used for ROM)
ROMOE#	120	I	ROM Output Enable (DIR) (only used for ROM)
Power			
VCC	21, 60, 101, 125, 139		+ 5V Supply Voltage
VTR	32		Trickle Voltage Input
GND↔	1, 8, 40, 71, 95, 123, 130		Ground

2.5.5 Multifunction Pins with GPI/O and Other Alternate Functions

Table 2- 6 Multifunction Pins with GPI/O and Other Alternate Functions

Pin No.	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Buffer Type	Default	Index Register	GPI/O
19	MEDIA_ID1	GPI/O			I/O8	Float	GP4	GP40
20	MEDIA_ID0	GPI/O			I/O8	Float	GP4	GP41
23	IDE1_OE#	GPI/O			I/O4	High	GP4	GP42
24	HDCS0#	GPI/O			I/O24	High	GP4	GP43
25	HDCS1#	GPI/O			I/O24	High	GP4	GP44
26	IDE1_IRQ	GPI/O			I/O8	Float	GP4	GP45
30	IOROP#	GPI/O	Power LED Output	WDT	I/O24	Float	GP4	GP46
31	IOWOP#	GPI/O	SMI#		I/O24	Float	GP4	GP47
33	PowerOn#	GPI/O			I/O24	Active low open collector output	GP5	GP51
34	Button_In	GPI/O			I/O24	Input	GP5	GP50
111	RD0	GPI/O	Power LED Output		I/O4	RD0 (1) (4)	GP6	GP60
112	RD1	GPI/O	WDT		I/O4	RD1 (1) (4)	GP6	GP61
113	RD2	GPI/O	8042-P12		I/O4	RD2 (1) (4)	GP6	GP62
114	RD3	GPI/O	8042-P13		I/O4	RD3 (1) (4)	GP6	GP63
115	RD4	GPI/O	8042-P14		I/O4	RD4 (1) (4)	GP6	GP64
116	RD5	GPI/O	8042-P15		I/O4	RD5 (1) (4)	GP6	GP65
117	RD6	GPI/O	8042-P16		I/O4	RD6 (1) (4)	GP6	GP66
118	RD7	GPI/O	8042-P17		I/O4	RD7 (1) (4)	GP6	GP67
119	ROMCS#	GPI/O			I/O8	ROMCS# (1)	GP5	GP53
120	ROMOE#	GPI/O			I/O8	ROMOE# (1)	GP5	GP54
153	R12#	GPI/O			I/O8	Input (2)	GP7	GP70
154	DCD2#	GPI/O			I/O8	Input (2)	GP7	GP71
155	RXD2	GPI/O			I/O8	Input (2)	GP7	GP72
156	TXD2	GPI/O			I/O8	Input (2) (4)	GP7	GP73
157	DSR2#	GPI/O			I/O8	Input (2)	GP7	GP74
158	RTS2#	GPI/O			I/O8	Input (2) (4)	GP7	GP75
159	CTS2#	GPI/O			I/O8	Input (2)	GP7	GP76
160	DTR2#	GPI/O			I/O8	Input (2) (4)	GP7	GP77

Table 2- 6 Multifunction Pins with GPI/O and Other Alternate Functions

Pin No.	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Buffer Type	Default	Index Register	GPI/O
27	HDCS2#	SA13			I/O24	Float		
28	HDCS3#	SA14			I/O24	Float		
29	IDE2_IRQ	SA15			I	Float		
53	CS/SA 12#				I	Input		
96	GPI/O	IRQ in			I/O4	Input	GP1	GP10
97	GPI/O	IRQ in	IRQ13		I/O4	Input	GP1	GP11
98	GPI/O	WDT Timer Output/IRRX			I/O4	Input	GP1	GP12
99	GPI/O	Power LED Output/IRTX			I/O24	Input	GP1	GP13
100	GPI/O	GP Address Decode			I/O4	Input	GP1	GP14
102	GPI/O	GP Write Strobe			I/O4	Input	GP1	GP15
103	GPI/O	Joy Read Strobe	JOYCS		I/O4	Input	GP1	GP16
104	GPI/O	Joy Write Strobe			I/O4	Input	GP1	GP17
105	GPI/O	IDE2 Output Enable	8042 P20		I/O4	Input	GP2	GP20
106	GPI/O	Serial EEPROM Data In	AB_DATA		I/O8/ OD8 (EN1)	Input	GP2	GP21
107	GPI/O	Serial EEPROM Data Out	AB_CLK		I/O8/ OD8 (EN1)	Input	GP2	GP22
108	GPI/O	Serial EEPROM Clock			I/O4	Input	GP2	GP23
109	GPI/O	Serial EEPROM Enable			I/O4	Input	GP2	GP24
110	GPI/O	8042 P21			I/O4	Input	GP2	GP25

Notes (1): At power-up, RD0-RD7, ROMCS# and ROMOE# function as the XD Bus. To use RD0-RD7 for functions other than the XD Bus, ROMCS# must stay high until the reprogramming of RD0-RD7 is done.

(2): These pins are input (high-z) until they are programmed for second serial port.

(3): This is the trickle voltage input pin for the FDC37C93XAPM.

(4): These pins cannot be programmed as open drain pins in their original function.

(5): No pins in their original function can be programmed as inverted input or inverted output.

2.5.6 Buffer Type Descriptions

Table 2- 7 SMC 37C935 Buffer Type Descriptions

Buffer Type	Description
I	Input TTL compatible
IS	Input with Schmitt Trigger
I/OD16P	Input/output, 19-mA sink, 90-uA pull-up
I/O24	Input/output pin. 24-mA sink; 12-mA source
O4	Output, 4-mA sink; 2.0-mA source
O8SR	Output, 8-mA sink; 4.0-mA source with Slew Rate Limiting
O24	Output, 24-mA sink; 12-mA source
OD24	Output, open drain; 24-mA sink
OD48	Output, open drain; 48-mA sink
OD24P	Output, open drain; 24-mA sink, 4-mA source pull up
OP24	Output; 24-mA sink, 12-mA source
OCLK	Clock output
ICLK	Clock input

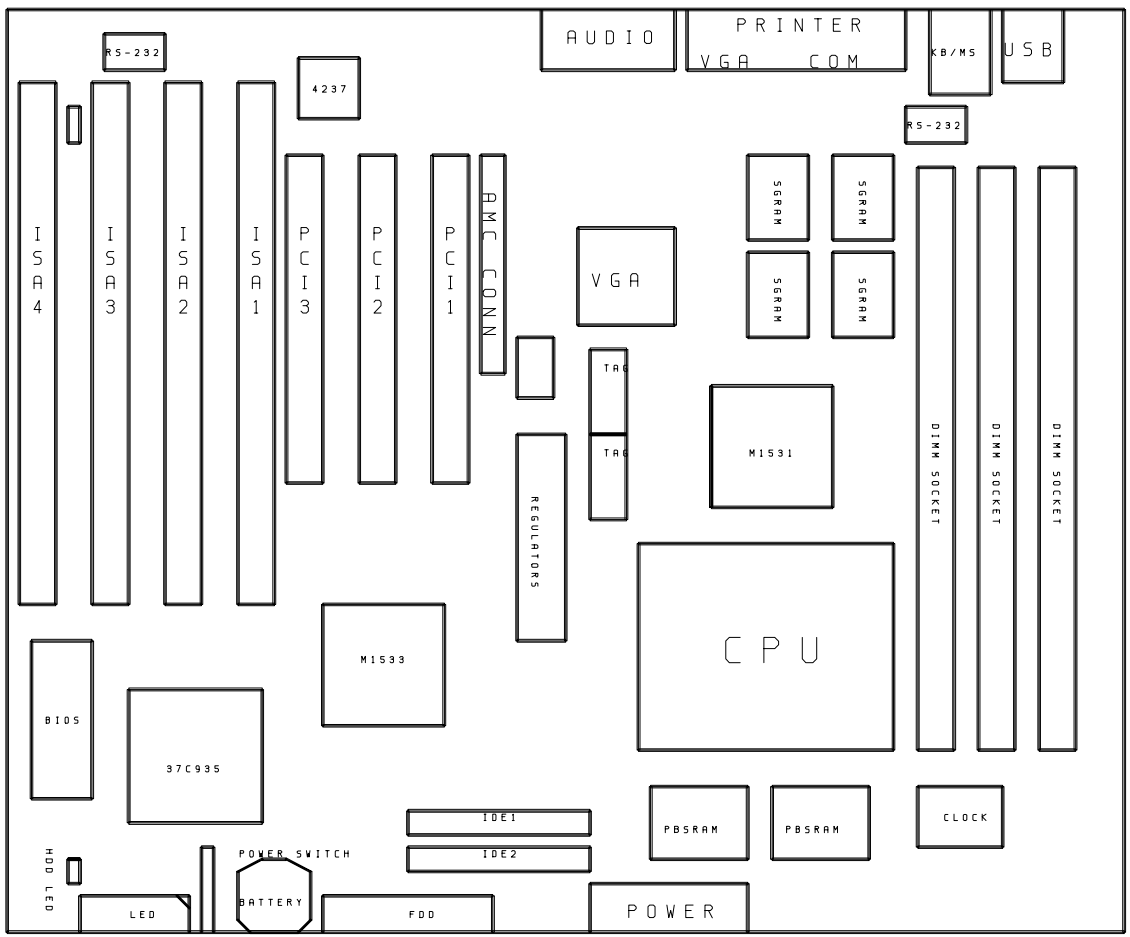
DESCRIPTION

V58XA

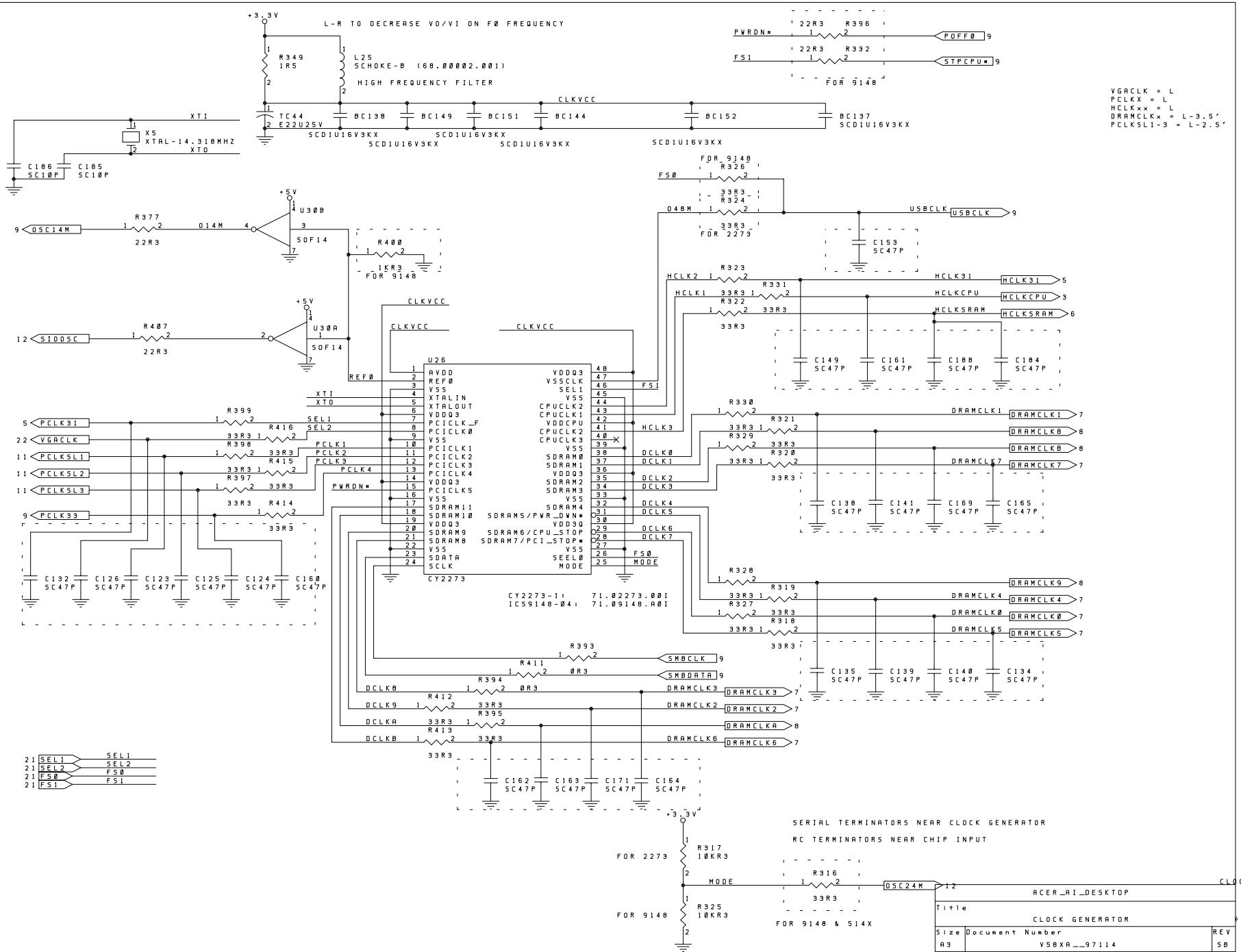
97114-SB

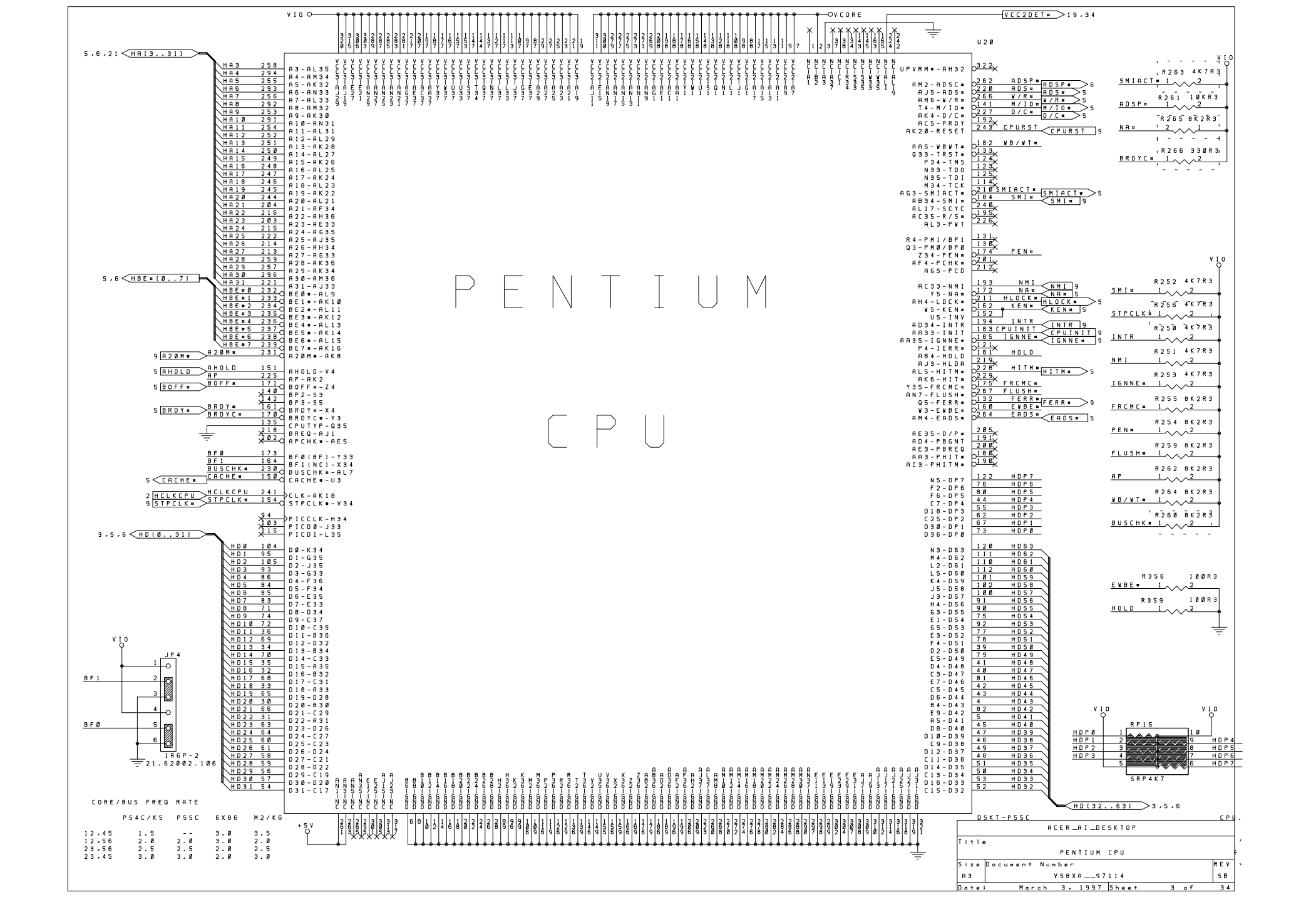
MAY 24, 1997

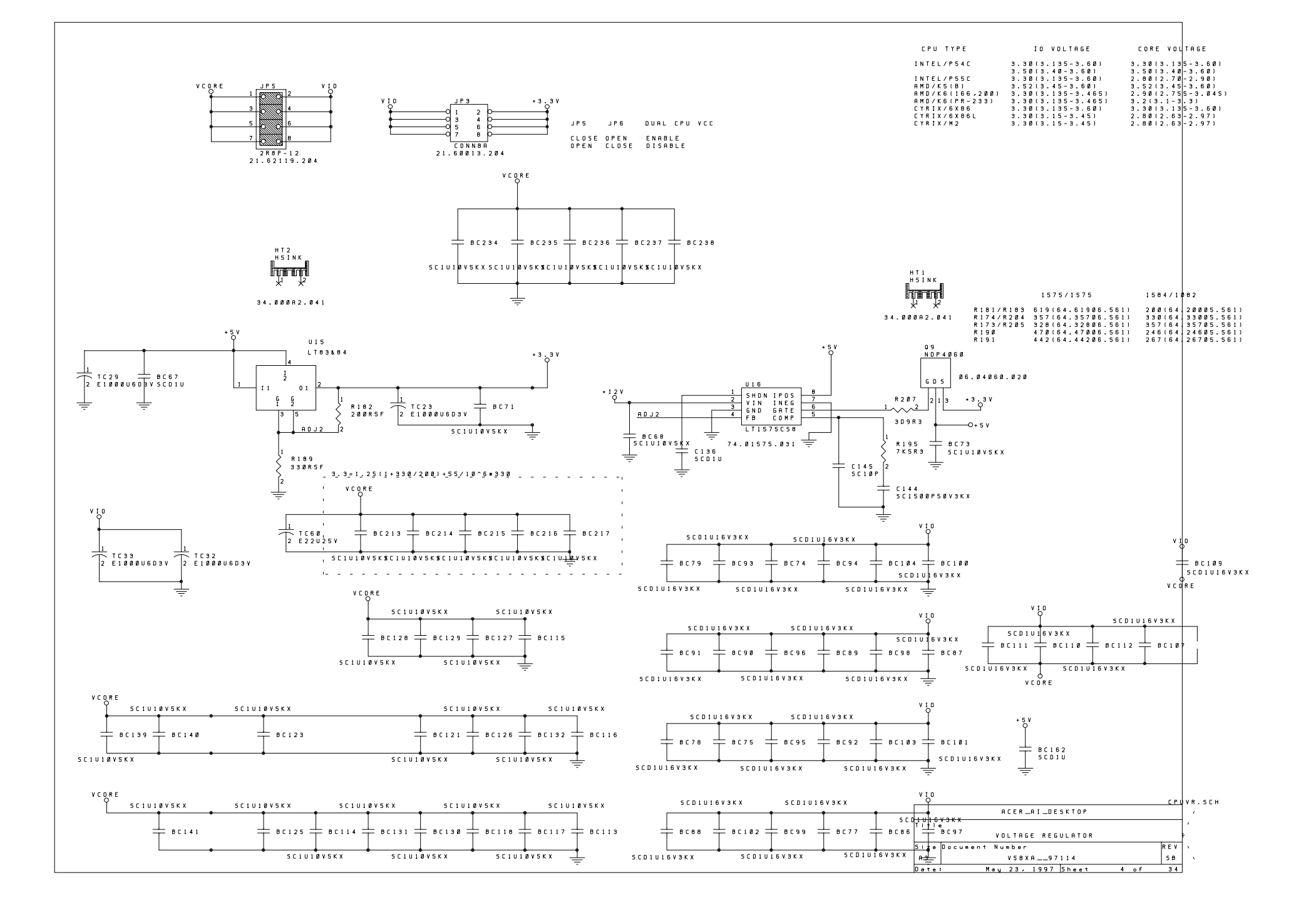
SH01:	CLOCK GENERATOR	ILINK
SH02:	PENTIUM CPU	ICLOCK
SH03:	VOLTAGE REGULATOR	ICPU.S
SH04:	ALI M1531	ICPUVR
SH05:	PBSRAM & TAG	IM1531
SH06:	SDRAM SKT 1 & 2	ICACHE
SH07:	SDRAM SKT 3	IDRAM1
SH08:	ALI M1533	IDRAM2
SH09:	IDE & FDD CONN	IM1533
SH10:	PCI SLOTS	IIDEFD
SH11:	SMC 37C935	IPCI.S
SH12:	ROM & RTC	ISMC93
SH13:	ISA SLOTS	IROMRT
SH14:	PS/2 KB & MS	IISA.S
SH15:	PARALLEL/COM PORT	IKBMS.
SH16:	USB PORTS	IPNT-C
SH17:	FAN, LED CONN	IUSB.S
SH18:	H/W MONITOR	ICONN.
SH19:	POWER SWITCHES	IHWMON
SH20:	FREQUENCY SEL	IPOWER
SH21:	ATI 264GT-B2	IFREQ.
SH22:	VGA POWER	IV264G
SH23:	VGA TO PNT-VGA-RS	IVGAPO
SH24:	VGA HARDWARD TRAP	IVGACO
SH25:	VGA SGRAM 2MB	IVGATR
SH26:	VGA SGRAM 4MB	IVGARS
SH27:	AMC CONNECTOR	IVGARS
SH28:	BULK CAPACITORS	IVGAAM
SH29:	BYPASS CAPACITORS	IBULK.
SH30:	CRYSTAL 4237	IBYPAS
SH31:	CD / LINE/ MIC-IN	ICS423
SH32:	LINE-OUT/ MIDI / IO PORT	ICD_MI
		IAIO.S
		ISWITC

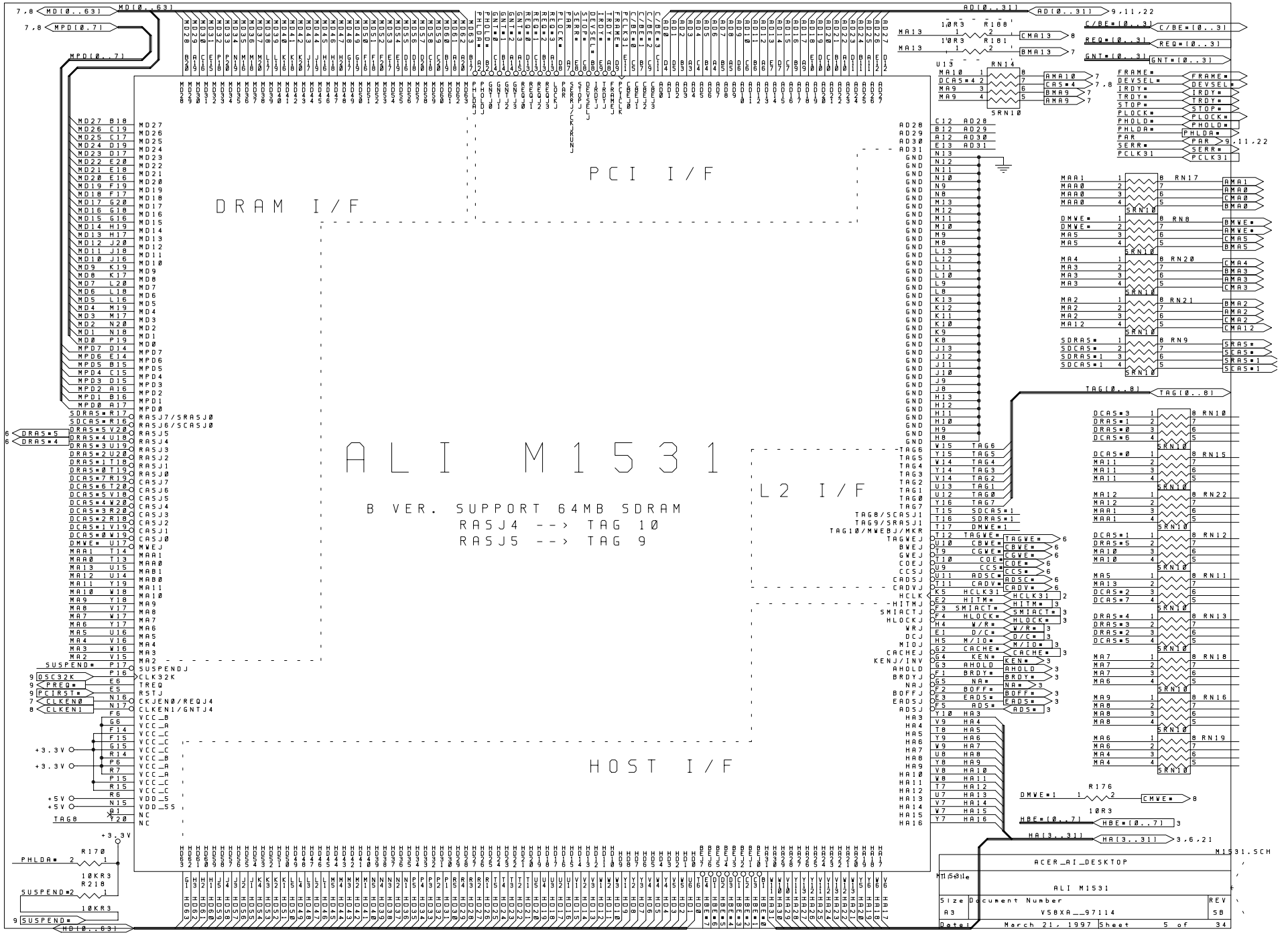


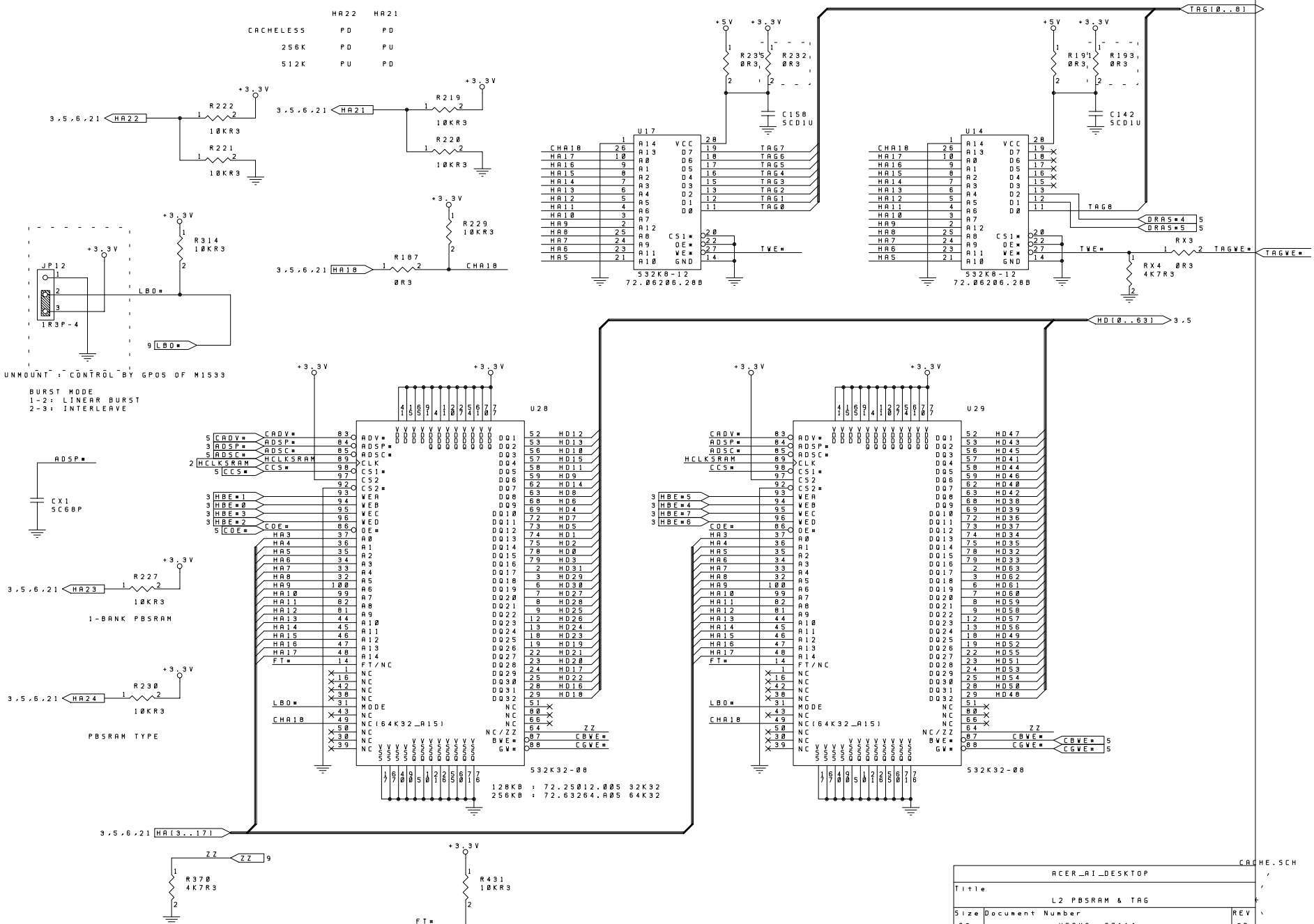
ACER_AI_DESKTOP		
Title	JUMPER SETTING	
Size A3	Document Number V58XA__97114	REV SB
Date: May 24, 1997	Sheet 1 of 34	

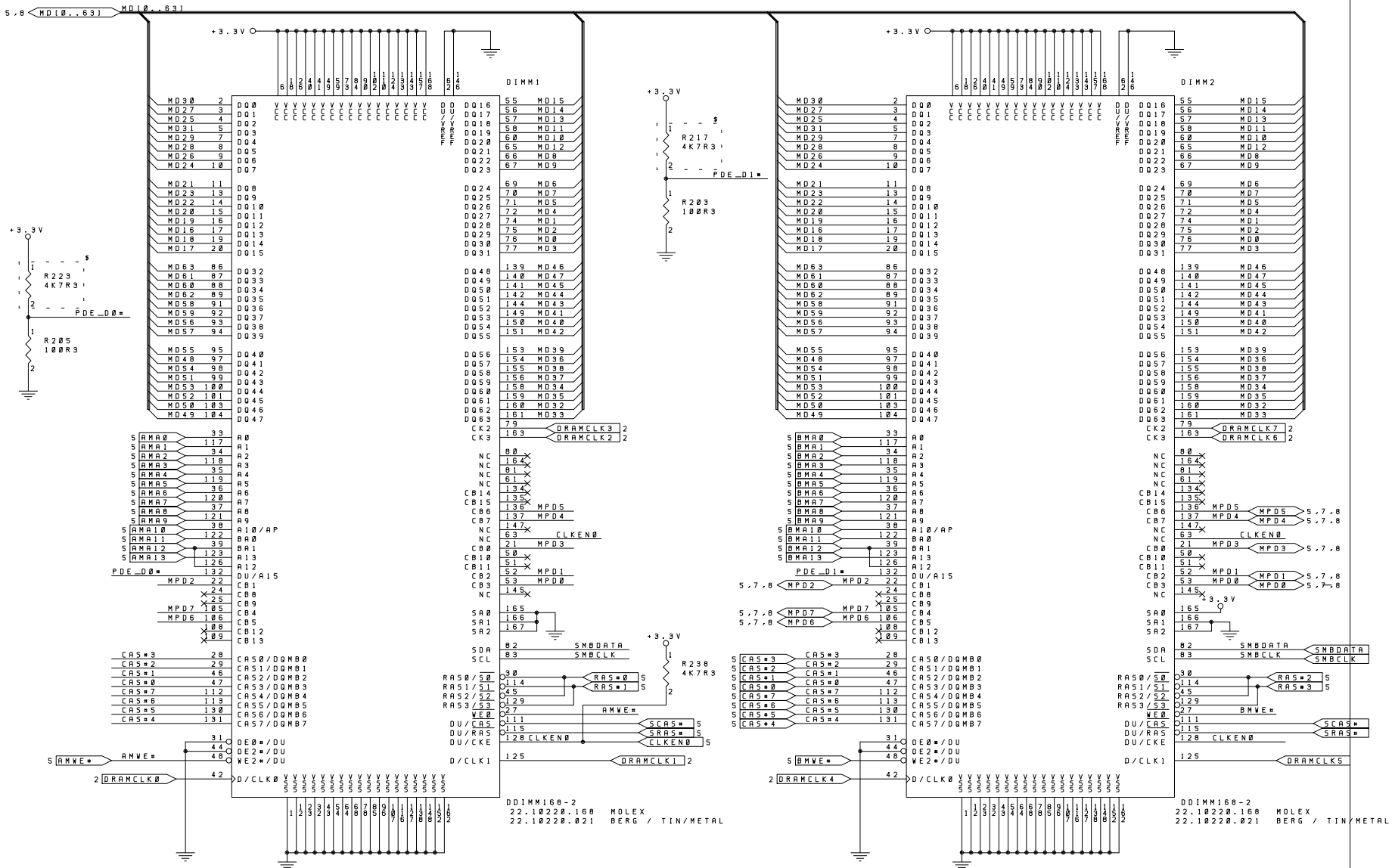

L-R TO DECREASE VO/VI ON F0 FREQUENCY
HIGH FREQUENCY FILTER
FOR 9148
FOR 2273
VGACLK = L
PCLKX = L
HCLKxx = L
DRAMCLKx = L-3.5'
PCLK5L1-3 = L-2.5'
SERIAL TERMINATORS NEAR CLOCK GENERATOR
RC TERMINATORS NEAR CHIP INPUT
CY2273-1: 71.02273.001
ICS9148-04: 71.09148.A01
ACER_AI_DESKTOP
CLOCK GENERATOR
V58XA__97114
April 7, 1997
2 of 34

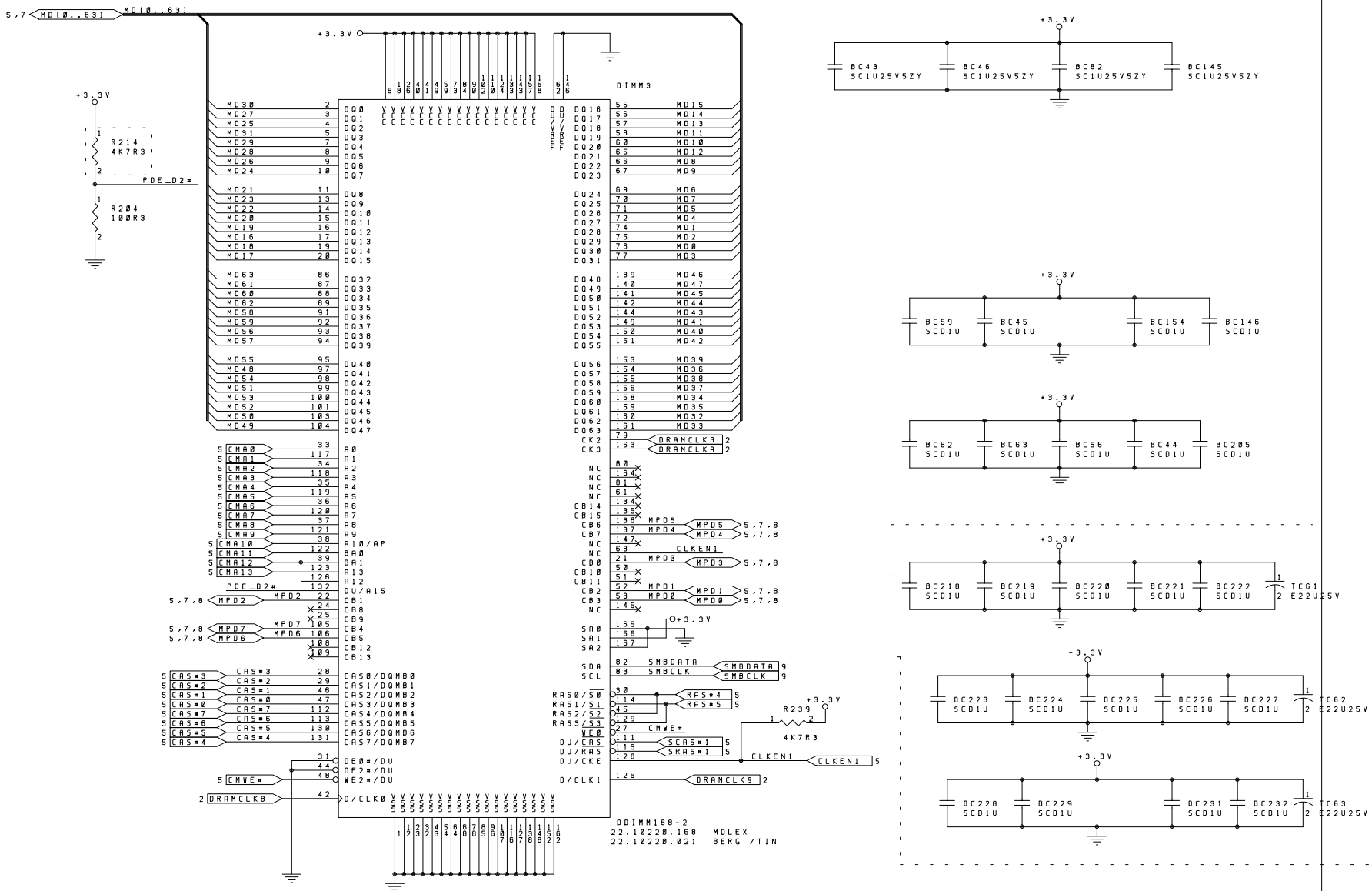

PENTIUM
CPU
U20
VIO
VCORE
VCC2DET#
JP4
RP15
SRP4K7
1R6P-2
21.62002.106
CORE/BUS FREQ RATE
P54C/K5 P55C 6X86 M2/K6
12,45 1.5 -- 3.0 3.5
12,56 2.0 2.0 3.0 2.0
23,56 2.5 2.5 2.0 2.5
23,45 3.0 3.0 2.0 3.0
DSKT-P55C
CPU.
ACER_AI_DESKTOP
Title
PENTIUM CPU
Size A3
Document Number V58XA__97114
REV 5B
Date: March 3, 1997
Sheet 3 of 34


CPU TYPE
IO VOLTAGE
CORE VOLTAGE
INTEL/P54C 3.30(3.135-3.60) 3.30(3.135-3.60)
3.50(3.40-3.60) 3.50(3.40-3.60)
INTEL/P55C 3.30(3.135-3.60) 2.80(2.70-2.90)
AMD/K5(B) 3.52(3.45-3.60) 3.52(3.45-3.60)
AMD/K6(166,200) 3.30(3.135-3.465) 2.90(2.755-3.045)
AMD/K6(PR-233) 3.30(3.135-3.465) 3.2(3.1-3.3)
CYRIX/6X86 3.30(3.135-3.60) 3.30(3.135-3.60)
CYRIX/6X86L 3.30(3.15-3.45) 2.80(2.63-2.97)
CYRIX/M2 3.30(3.15-3.45) 2.80(2.63-2.97)
JP5 JP6 DUAL CPU VCC
CLOSE OPEN ENABLE
OPEN CLOSE DISABLE
1575/1575 1584/1082
R181/R183 619(64.61906.561) 200(64.20005.561)
R174/R204 357(64.35706.561) 330(64.33005.561)
R173/R205 328(64.32806.561) 357(64.35705.561)
R190 470(64.47006.561) 246(64.24605.561)
R191 442(64.44206.561) 267(64.26705.561)
VCORE
VIO
+5V
+3.3V
+12V
JP5
JP3
2R8P-12
21.62119.204
CONN8A
21.60013.204
HT2 HSINK
HT1 HSINK
34.000A2.041
U15 LT83&84
U16 LT1575CS8
Q9 NDP4060
GD5
06.04060.020
74.01575.031
ADJ2
3.3*1.25(1+330/200)+55/10^6*330
TC29 E1000U6D3V
BC67 SC1U
TC23 E1000U6D3V
BC71 SC1U10V5KX
R182 200R5F
R189 330R5F
BC68 SC1U10V5KX
C136 SC1U
R207 3D9R3
R195 7K5R3
BC73 SC1U10V5KX
C145 SC10P
C144 SC1500P50V3KX
TC33 E1000U6D3V
TC32 E1000U6D3V
TC60 E22U25V
BC234 BC235 BC236 BC237 BC238
BC213 BC214 BC215 BC216 BC217
BC79 BC93 BC74 BC94 BC104 BC100
BC109
BC128 BC129 BC127 BC115
BC91 BC90 BC96 BC89 BC98 BC87
BC111 BC110 BC112 BC107
BC139 BC140 BC123 BC121 BC126 BC132 BC116
BC78 BC75 BC95 BC92 BC103 BC101
BC162 SC1U
BC141 BC125 BC114 BC131 BC130 BC118 BC117 BC113
BC88 BC102 BC99 BC77 BC86 BC97
SC1U10V5KX
SCD1U16V3KX
ACER_AI_DESKTOP
VOLTAGE REGULATOR
CPUVR.SCH
Size Document Number REV
A3 V58XA__97114 5B
Date: May 23, 1997 Sheet 4 of 34


DRAM I/F
PCI I/F
ALI M1531
B VER. SUPPORT 64MB SDRAM
RASJ4 --> TAG 10
RASJ5 --> TAG 9
L2 I/F
HOST I/F
ACER_AI_DESKTOP
ALI M1531
Size
Document Number
V58XA__97114
REV
5B
Date: March 21, 1997
Sheet 5 of 34
M1531.SCH

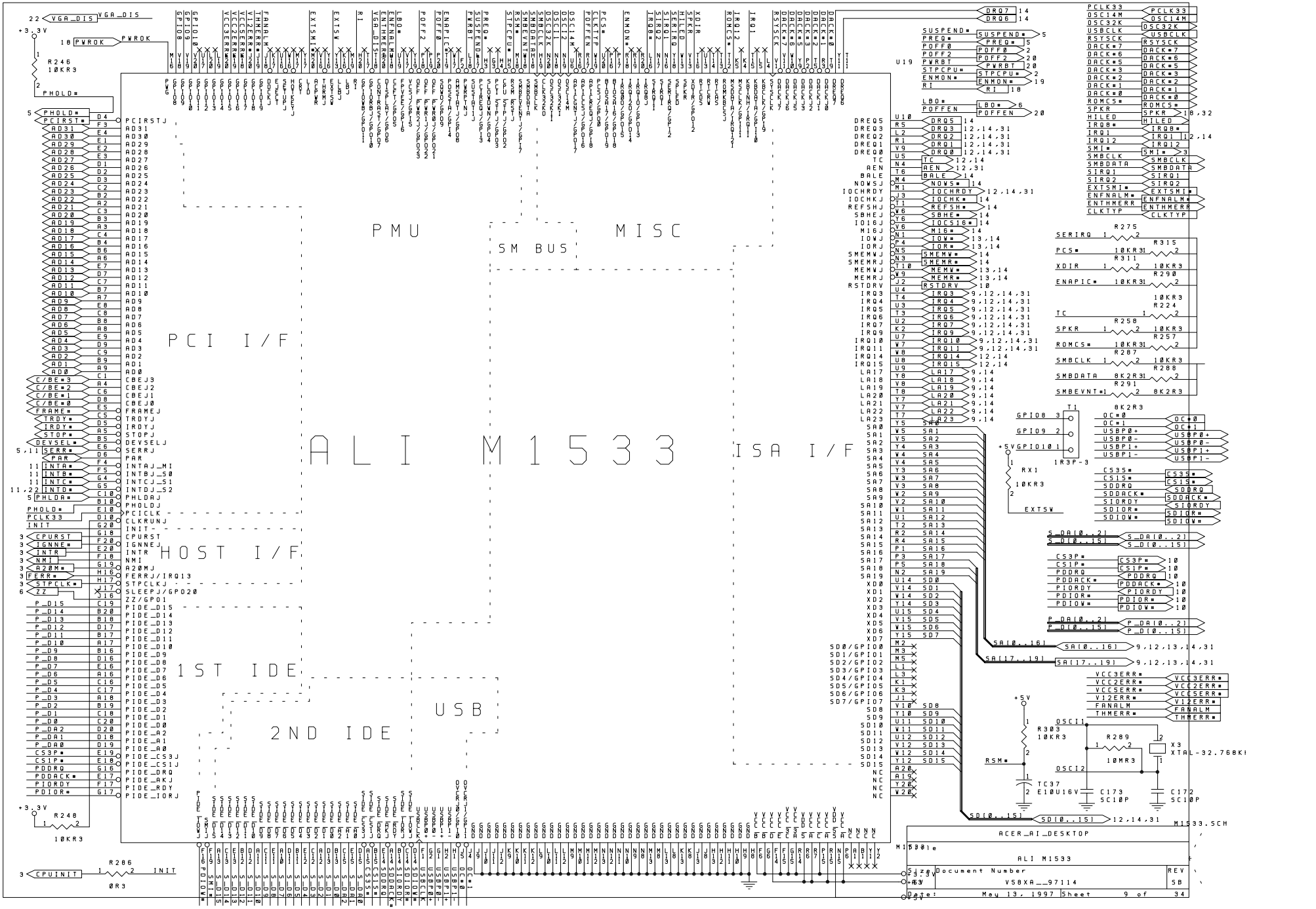

HA22 HA21
CACHELESS PD PD
256K PD PU
512K PU PD
R222 10KR3
R221 10KR3
R219 10KR3
R220 10KR3
R229 10KR3
R187 0R3
R314 10KR3
JP12
1R3P-4
LB0*
UNMOUNT : CONTROL BY GPOS OF M1533
BURST MODE
1-2: LINEAR BURST
2-3: INTERLEAVE
R235 0R3
R232 0R3
C158 SCD1U
U17
532K8-12
72.06206.28B
TAG[0..8]
R191 0R3
R193 0R3
C142 SCD1U
U14
TAG8
DRAS*4
DRAS*5
TWE*
RX3
RX4 0R3
4K7R3
TAGWE*
HD[0..63]
U28
U29
CADV*
ADSP*
ADSC*
HCLKSRAM
CCS*
HBE*1
HBE*0
HBE*3
HBE*2
COE*
HBE*5
HBE*4
HBE*7
HBE*6
CX1 5C68P
R227 10KR3
1-BANK PBSRAM
R230 10KR3
PBSRAM TYPE
532K32-08
128KB : 72.25012.005 32K32
256KB : 72.63264.A05 64K32
CBWE*
CGWE*
HA[3..17]
R370 4K7R3
R431 10KR3
FT*
ZZ
CACHE.SCH
ACER_AI_DESKTOP
L2 PBSRAM & TAG
Size A3
Document Number V58XA__97114
REV 5B
Date: May 16, 1997
Sheet 6 of 34

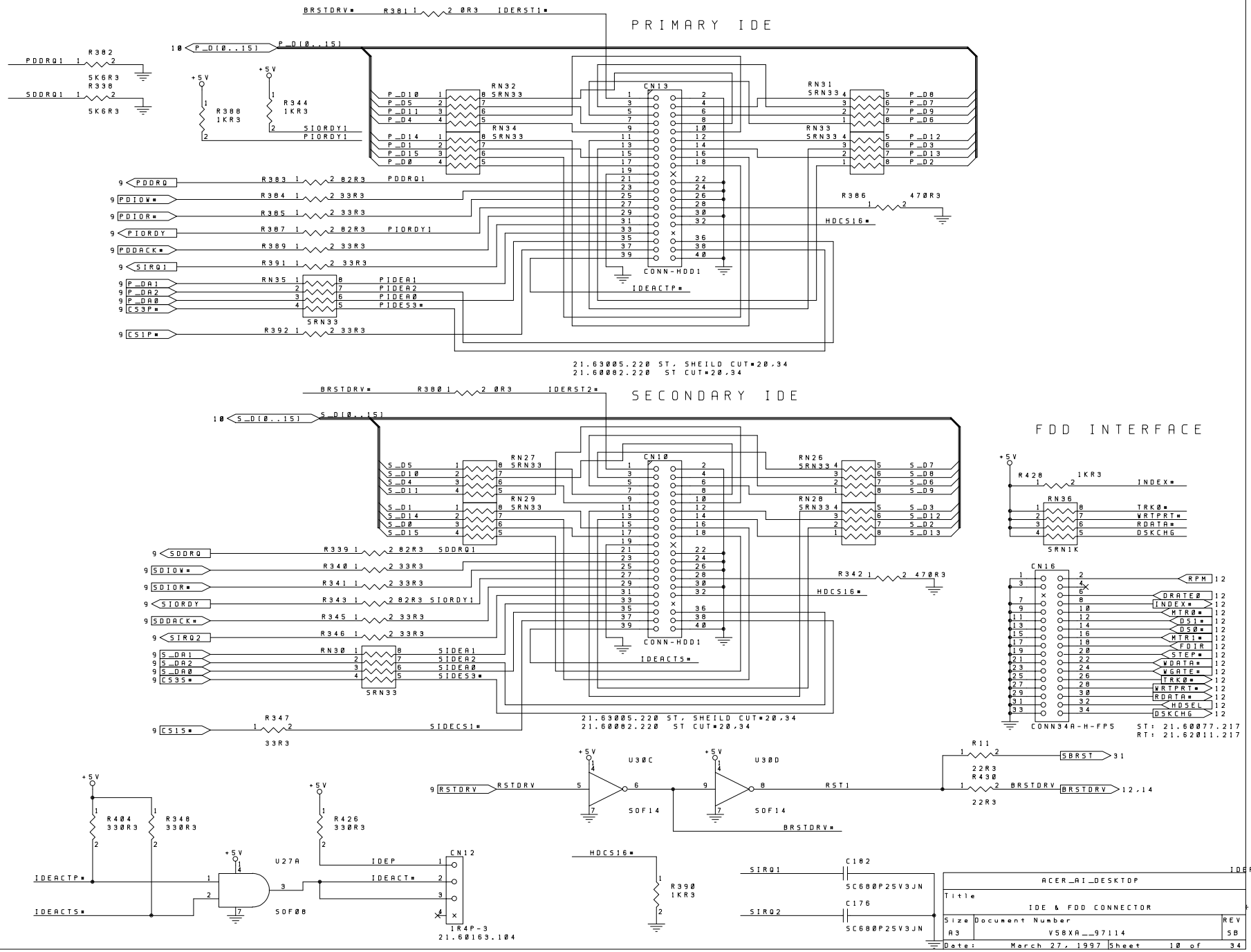

5,8 MD[0..63]
MD[0..63]
+3.3V
DIMM1
DIMM2
R223 4K7R3
R205 100R3
PDE_D0#
R217 4K7R3
R203 100R3
PDE_D1#
R238 4K7R3
DRAMCLK3
DRAMCLK2
DRAMCLK7
DRAMCLK6
SMBDATA
SMBCLK
AMWE#
SCAS#
SRAS#
CLKEN0
DRAMCLK1
DRAMCLK5
DRAMCLK0
DRAMCLK4
DDIMM168-2
22.10220.168 MOLEX
22.10220.021 BERG / TIN/METAL
ACER_AI_DESKTOP
SDRAM SKT 1 & 2
Size A3
Document Number VS8XA__97114
REV 5B
Date: March 27, 1997
Sheet 7 of 34
DRAM1.SC

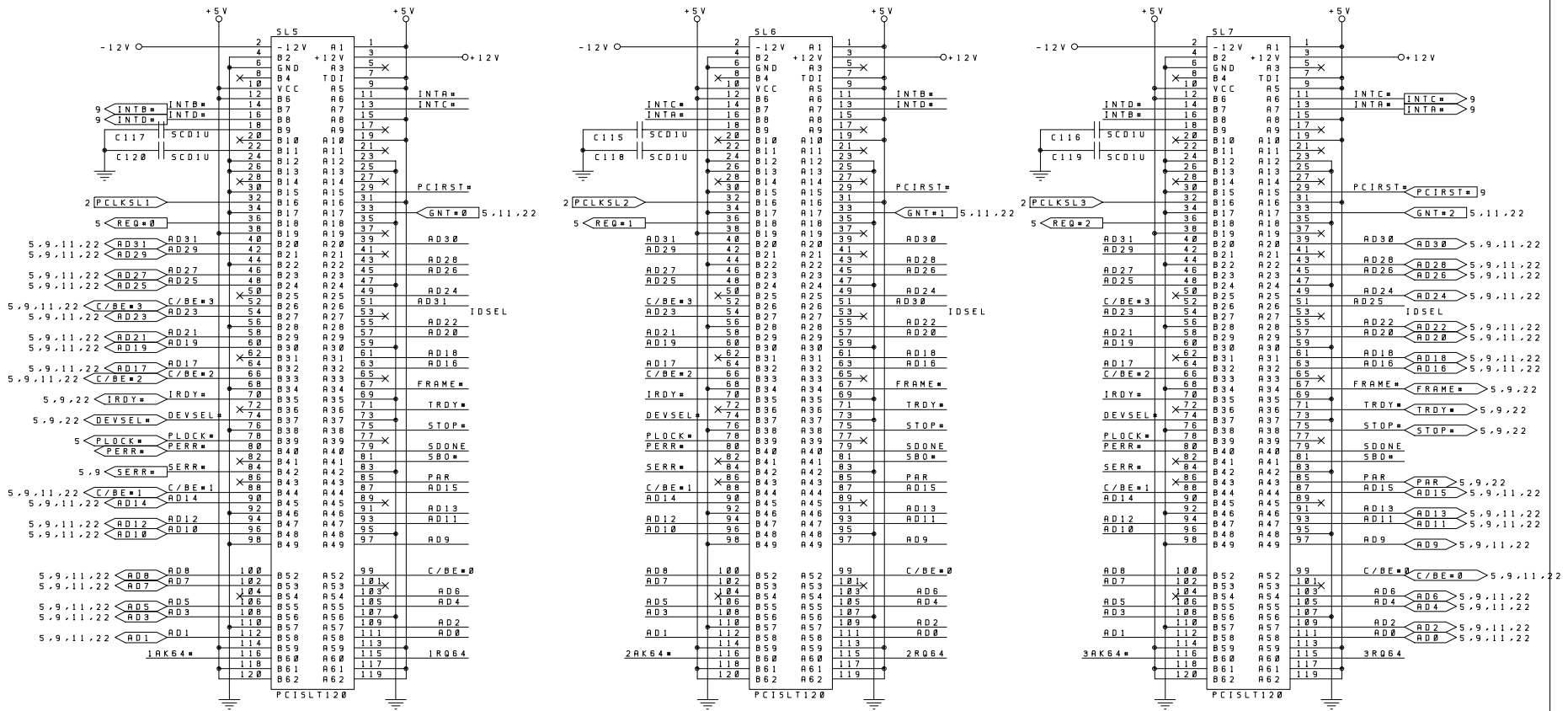


DRAM2.SCH

ACER_AI_DESKTOP		
Title: SDRAM SKT 3		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: May 22, 1997	Sheet 8 of 34	

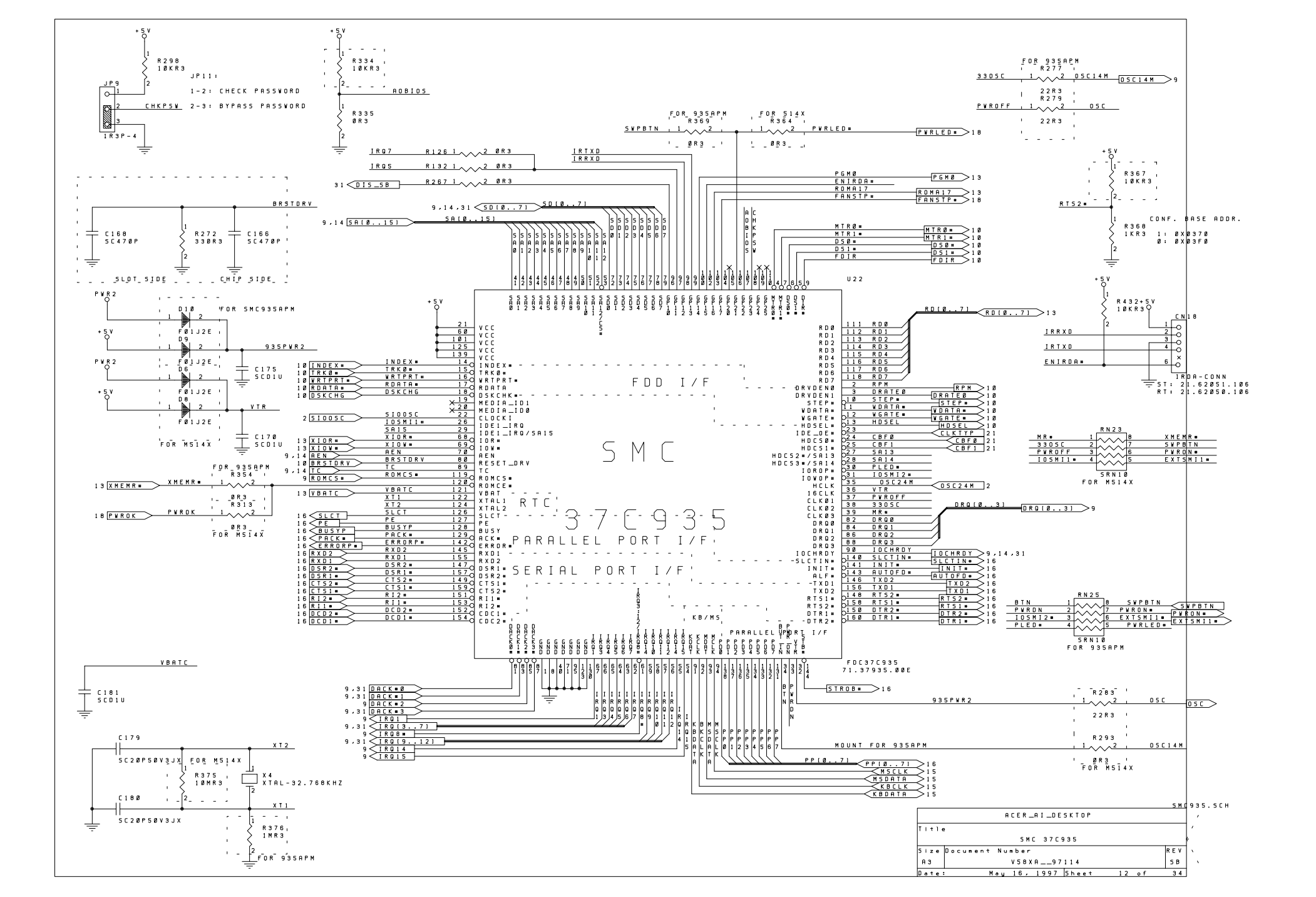

ALI M1533
PMU
MISC
SM BUS
PCI I/F
ISA I/F
HOST I/F
1ST IDE
2ND IDE
USB
ACER_AI_DESKTOP
ALI M1533
Document Number
V58XA__97114
REV
5B
Date: May 13, 1997
Sheet 9 of 34

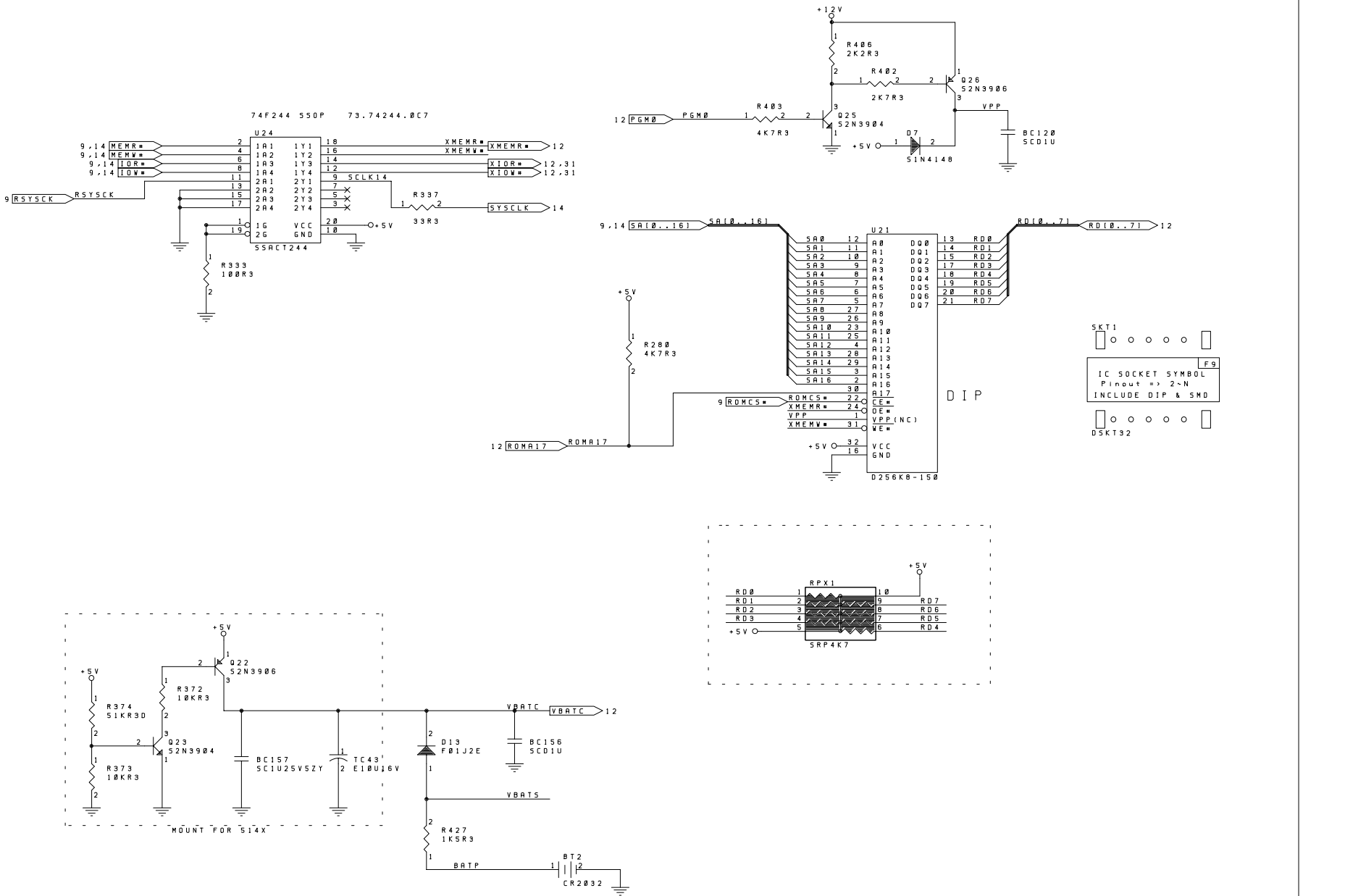

PRIMARY IDE
BRSTDRV*
R381 1 2 0R3
IDERST1*
P_D[0..15]
R382
PDDRQ1
5K6R3
R336
SDDRQ1
5K6R3
+5V
R388 1KR3
R344 1KR3
SIORDY1
PIORDY1
RN32 SRN33
RN34 SRN33
RN31 SRN33
RN33 SRN33
CN13
CONN-HDD1
IDEACTP*
HDCS16*
R386 470R3
PDDRQ
PDIOW*
PDIOR*
PIORDY
PDDACK*
SIRQ1
R383 82R3 PDDRQ1
R384 33R3
R385 33R3
R387 82R3 PIORDY1
R389 33R3
R391 33R3
P_DA1
P_DA2
P_DA0
CS3P*
RN35 SRN33
PIDEA1
PIDEA2
PIDEA0
PIDES3*
CS1P*
R392 33R3
21.63005.220 ST, SHEILD CUT=20,34
21.60002.220 ST CUT=20,34
SECONDARY IDE
BRSTDRV*
R380 1 2 0R3
IDERST2*
S_D[0..15]
RN27 SRN33
RN29 SRN33
RN26 SRN33
RN28 SRN33
CN10
CONN-HDD1
IDEACTS*
HDCS16*
R342 1 2 470R3
SDDRQ
SDIOW*
SDIOR*
SIORDY
SDDACK*
SIRQ2
R339 82R3 SDDRQ1
R340 33R3
R341 33R3
R343 82R3 SIORDY1
R345 33R3
R346 33R3
S_DA1
S_DA2
S_DA0
CS3S*
RN30 SRN33
SIDEA1
SIDEA2
SIDEA0
SIDES3*
CS1S*
R347 33R3
SIDECS1*
21.63005.220 ST, SHEILD CUT=20,34
21.60002.220 ST CUT=20,34
FDD INTERFACE
R428 1KR3
INDEX*
RN36 SRN1K
TRK0*
WRTPRT*
RDATA*
DSKCHG
CN16
CONN34A-H-FPS
RPM
DRATE0
INDEX*
MTR0*
DS1*
DS0*
MTR1*
FDIR
STEP*
WDATA*
WGATE*
TRK0*
WRTPRT*
RDATA*
HDSEL
DSKCHG
ST: 21.60077.217
RT: 21.62011.217
U30C
U30D
RSTDRV
RST1
R11 22R3
R430 22R3
SBRST
BRSTDRV
BRSTDRV*
12,14
R404 330R3
R348 330R3
R426 330R3
U27A
IDEP
IDEACT*
CN12
IR4P-3
21.60163.104
R390 1KR3
C182 SC680P25V3JN
C176 SC680P25V3JN
ACER_AI_DESKTOP
IDEFDD.SC
Title
IDE & FDD CONNECTOR
Size A3
Document Number V58XA__97114
REV 5B
Date: March 27, 1997 Sheet 10 of 34



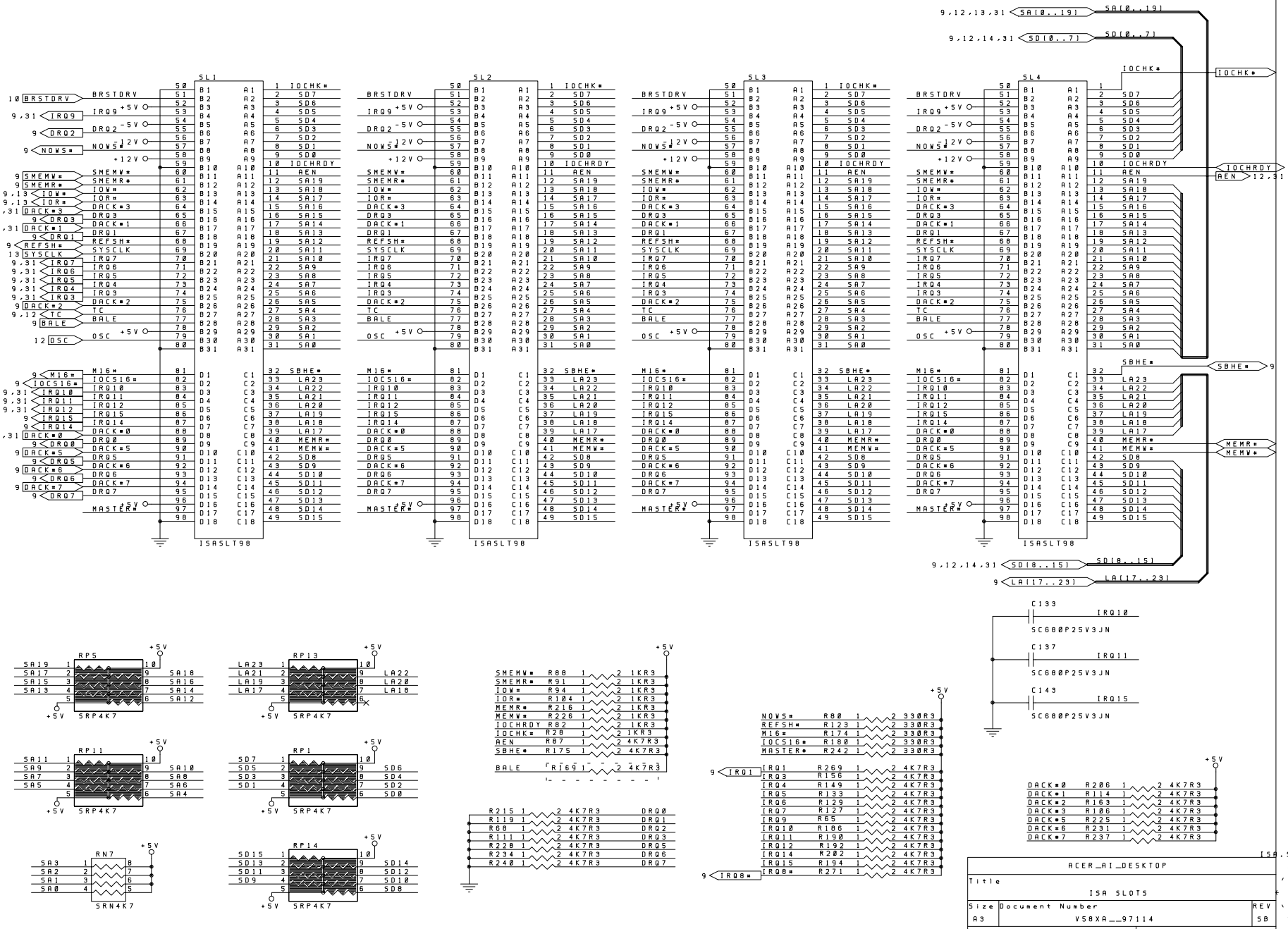
ACER_AI_DESKTOP		
Title	PCI SLOTS	
Size: A3	Document Number: V58XA__97114	REV: SB
Date: May 23, 1997	Sheet 11 of 34	

PCI.SC


SMC
37C935
FDD I/F
RTC
PARALLEL PORT I/F
SERIAL PORT I/F
KB/MS
PARALLEL PORT I/F
U22
FDC37C935
71.37935.00E
JP11:
1-2: CHECK PASSWORD
2-3: BYPASS PASSWORD
CHKPSW
SLOT_SIDE
CHIP_SIDE
BRSTDRV
FOR 935APM
FOR MS14X
FOR 514X
935PWR2
VTR
MOUNT FOR 935APM
CONF. BASE ADDR.
IRDA-CONN
ST: 21.62051.106
RT: 21.62050.106
SMC935.SCH
ACER_AI_DESKTOP
SMC 37C935
A3
V58XA__97114
5B
Date: May 16, 1997 Sheet 12 of 34



ACER_AI_DESKTOP		ROMRTC.SCH
Title: FLASH ROM & RTC		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: May 16, 1997	Sheet 13 of 34	


SL1
SL2
SL3
SL4
ISASLT98
SA[0..19]
SD[0..7]
IOCHK#
IOCHRDY
AEN
SBHE#
MEMR#
MEMW#
SD[8..15]
LA[17..23]
C133
IRQ10
SC680P25V3JN
C137
IRQ11
SC680P25V3JN
C143
IRQ15
SC680P25V3JN
RP5
RP13
RP11
RP1
RP14
RN7
SRP4K7
SRN4K7
R88 1K R3
R91 1K R3
R94 1K R3
R184 1K R3
R216 1K R3
R226 1K R3
R82 1K R3
R28 1K R3
R87 2K 7R3
R175 2K 7R3
R169 2K 7R3
R80 330R3
R123 330R3
R174 330R3
R180 330R3
R242 330R3
R269 4K7R3
R156 4K7R3
R149 4K7R3
R133 4K7R3
R129 4K7R3
R127 4K7R3
R65 4K7R3
R186 4K7R3
R190 4K7R3
R192 4K7R3
R202 4K7R3
R194 4K7R3
R271 4K7R3
R206 4K7R3
R114 4K7R3
R163 4K7R3
R106 4K7R3
R225 4K7R3
R231 4K7R3
R237 4K7R3
R215 4K7R3
R119 4K7R3
R60 4K7R3
R111 4K7R3
R228 4K7R3
R234 4K7R3
R240 4K7R3
ACER_AI_DESKTOP
ISA 5SLOTS
VS8XA__97114
Date: February 28, 1997 Sheet 14 of 34

FUCNTION MODULE
Keyboard/Mouse
for ATX

function module name:

component group:

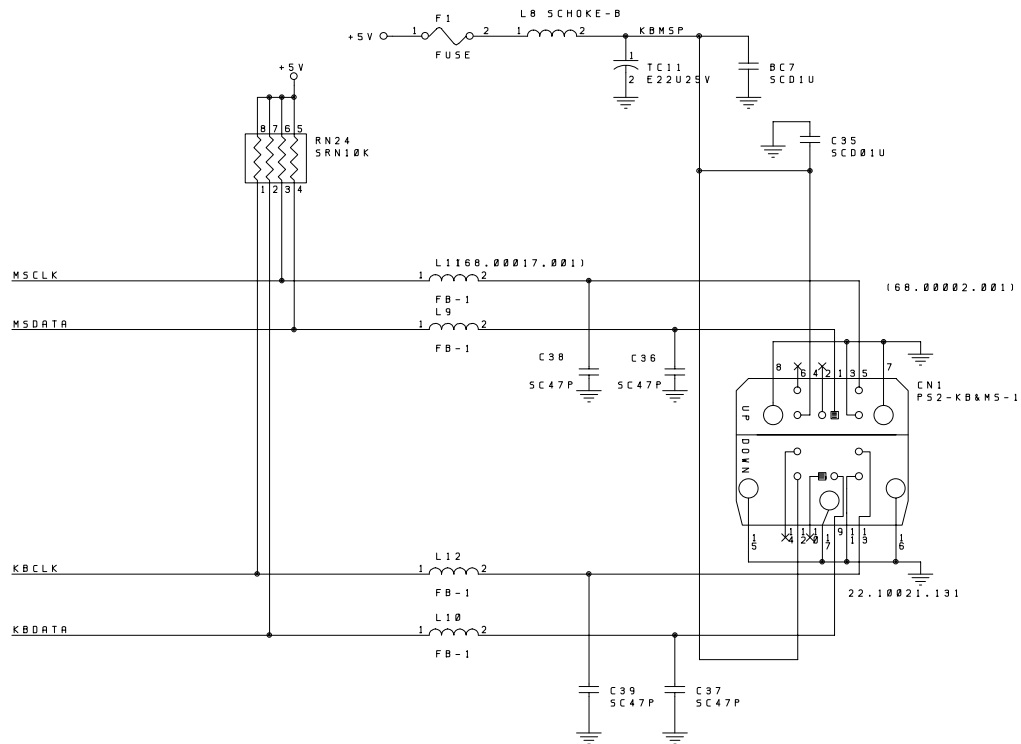
remarks: for SMC93X-like I/O

12 MSCLK MSCLK

12 MSDATA MSDATA

12 KBCLK KBCLK

12 KBDATA KBDATA



KBMS.SCH

ACER_AI_DESKTOP		
Title: PS/2 KB & MS		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: March 18, 1997	Sheet 15 of 34	

function module name:

component group: for ATX
remarks:

Interface

Parallel Port

SERIAL PORT

VGA

FUNCTION MODULE
Printer Port for ATX
function module name:
component group:
remarks:

PRINTER PORT

EMI Components

EMI Filter

COM1

21.60013.009

CONN10A-FP10

U6

U2

75C185

PRINTER

COM2

PNT-RS-VGA

EMI Components

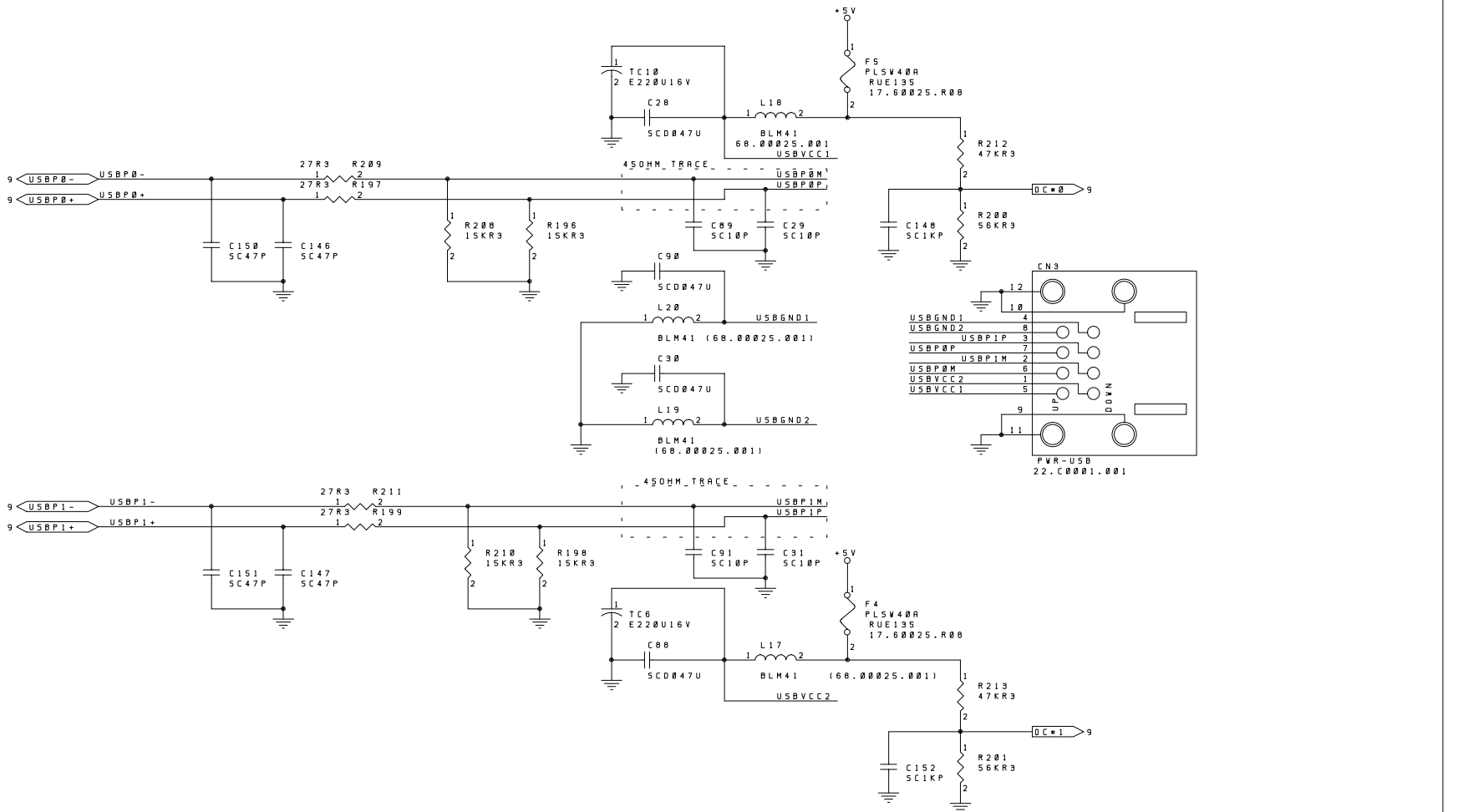
ACER_AI_DESKTOP

PRNT.SCH

PARALLEL PORT

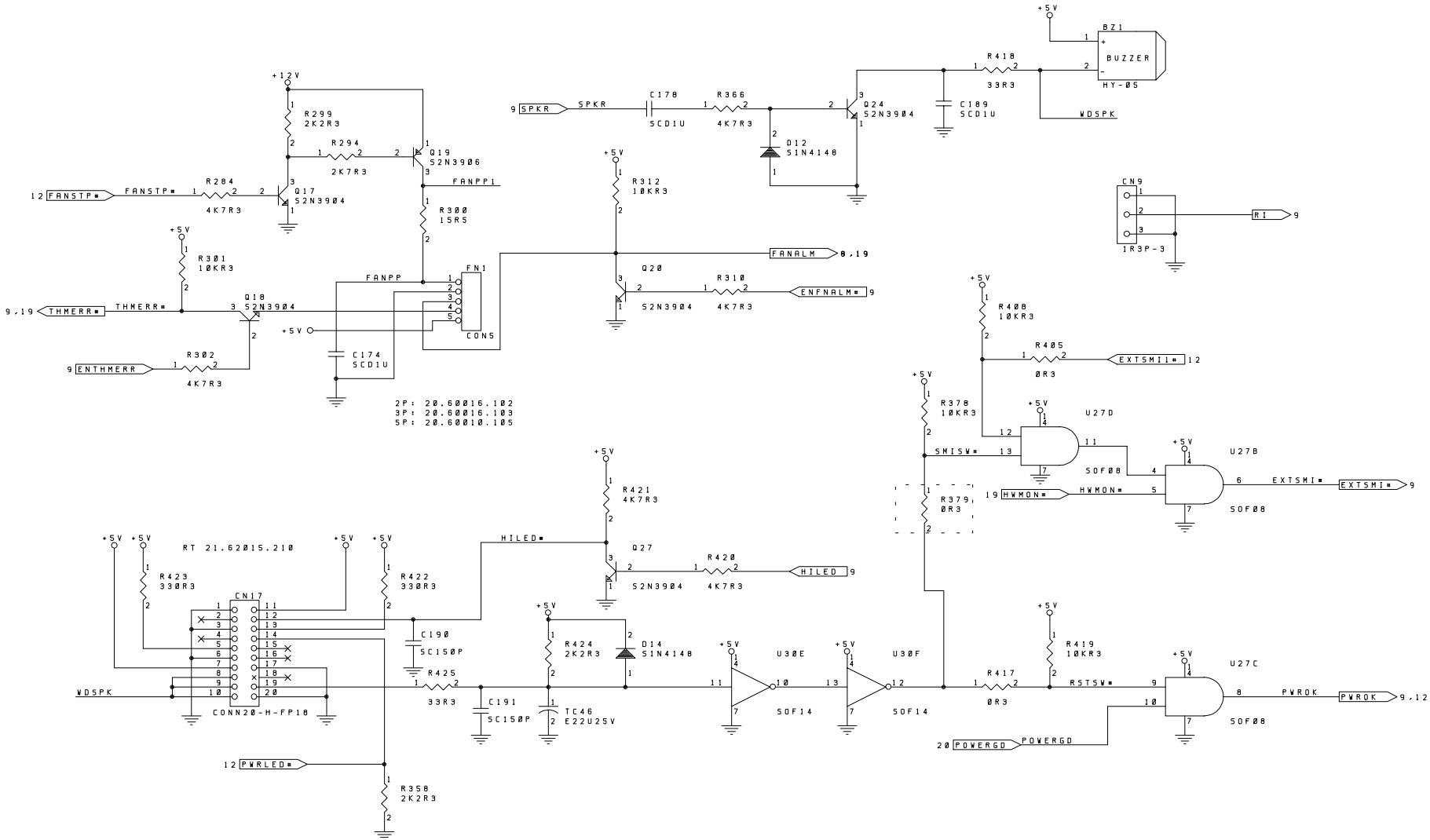
Size	Document Number	REV
A3	V50XA__97114	5B

Date: May 24, 1997 Sheet 16 of 34



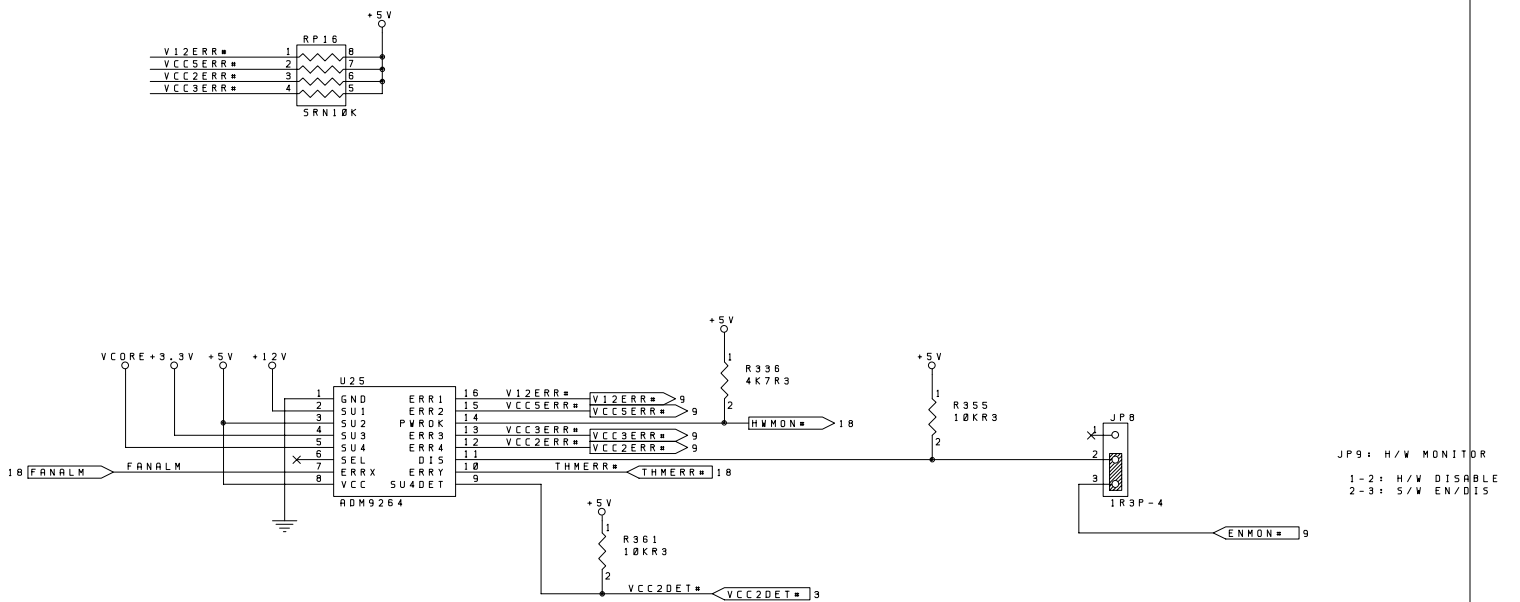
USB.SCH

ACER_AI_DESKTOP		
Title: USB PORTS		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: March 3, 1997	Sheet 17 of 34	



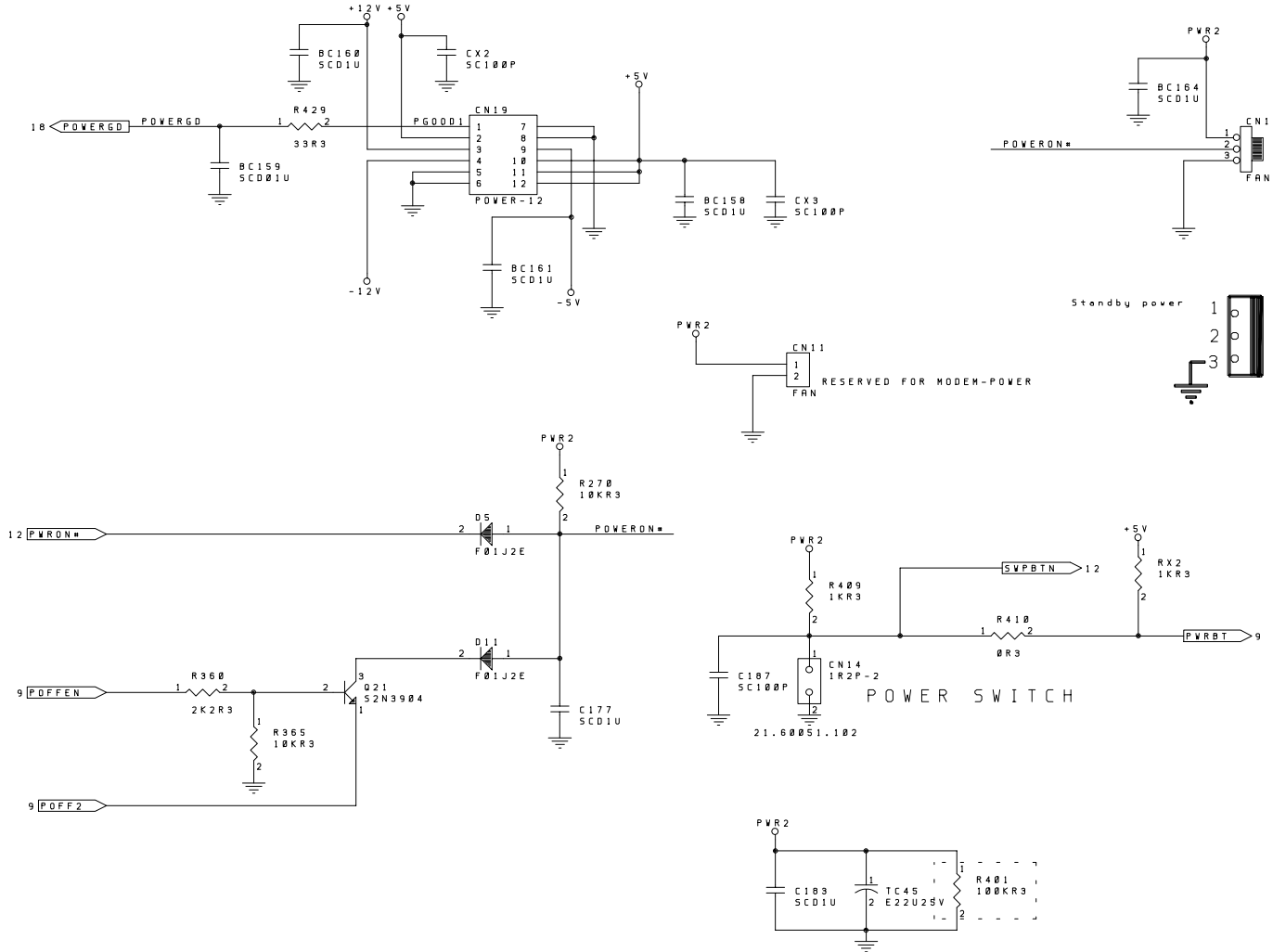
ACER_AI_DESKTOP		
Title: FAN, LED CONNECTORS		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: March 18, 1997	Sheet 18 of 34	

CONN.SCH



ACER_AI_DESKTOP		
Title: H/W MONITOR		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: February 27, 1997	Sheet 19 of 34	

HWMON.SCH

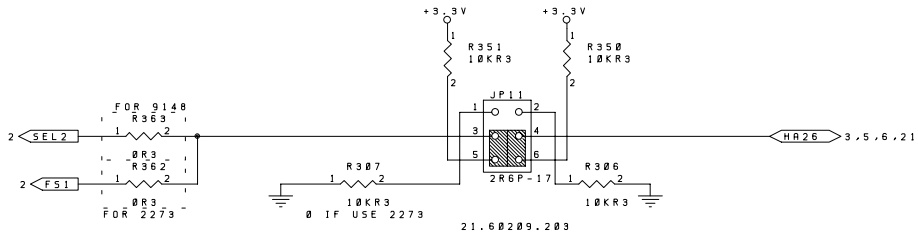


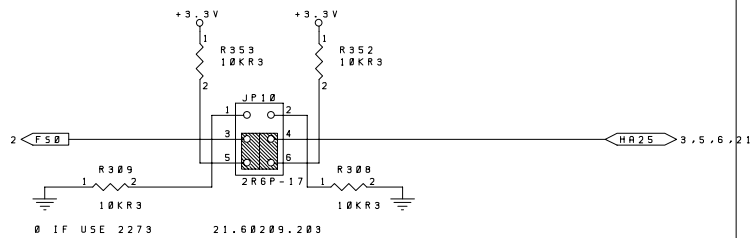
ACER_AI_DESKTOP		POWER.SCH
Title: POWER SWITCHES		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: May 16, 1997	Sheet 20 of 34	

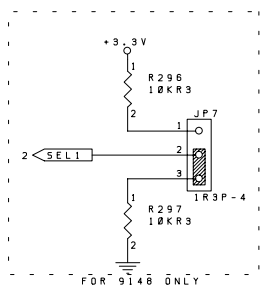
JP3	JP2	JP1 (FOR 9148)	HCLK/PCLK (CY22273)	HCLK/PCLK (ICS9148)
1-3 & 2-4	1-3 & 2-4	1-2	60/30MHZ	83/33MHZ
1-3 & 2-4	3-5 & 4-6	2-3	66/33MHZ	75/30MHZ
3-5 & 4-6	1-3 & 2-4	1-2	75/30MHZ	60/30MHZ
3-5 & 4-6	3-5 & 4-6	1-2	83/33MHZ	66/33MHZ

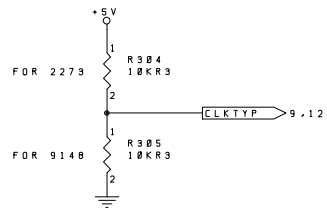
CLKTYP	CBF1	CBF0	CPU BUS FREQ.
1	0	0	60MHZ
1	0	1	66MHZ
1	1	0	75MHZ
1	1	1	83.3MHZ
0	0	0	83.3MHZ
0	0	1	75MHZ
0	1	0	60MHZ
0	1	1	66MHZ

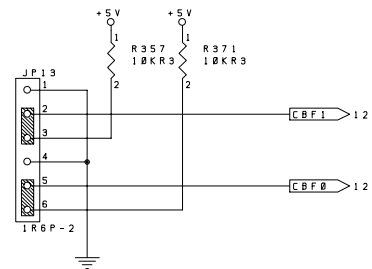
CLKTYP	HA26	HA25	CPU BUS FREQ.
1	0	0	60MHZ
1	0	1	66MHZ
1	1	0	75MHZ
1	1	1	83.3MHZ
0	0	0	83.3MHZ
0	0	1	75MHZ
0	1	0	60MHZ
0	1	1	66MHZ





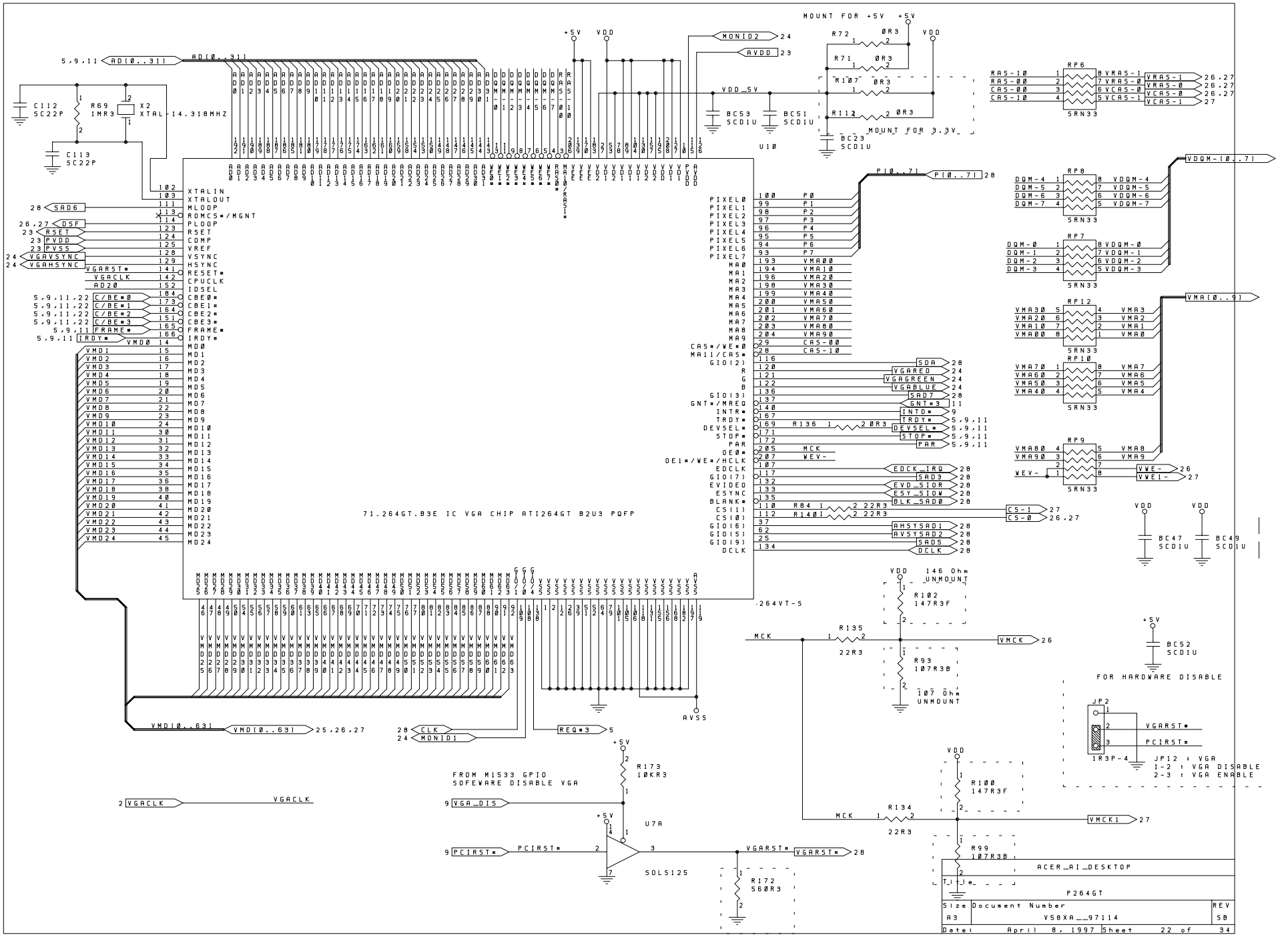


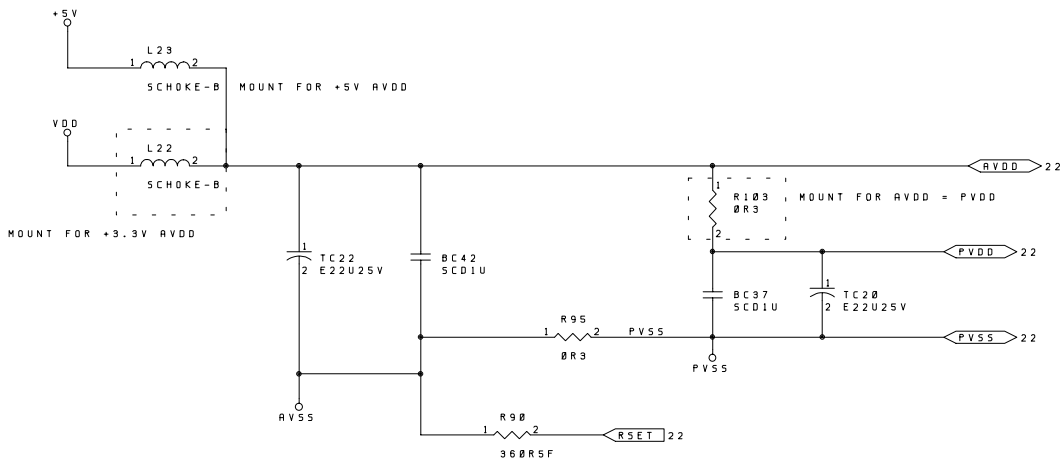


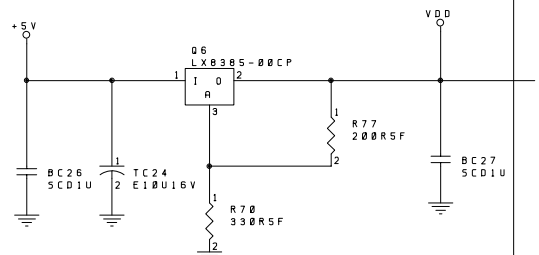


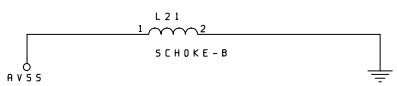
FREQ.SCH

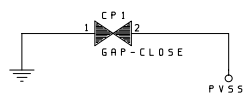
ACER_AI_DESKTOP		
Title: FREQUENCY SELECTION		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: March 11, 1997	Sheet 21 of 34	


71.264GT.B3E IC VGA CHIP ATI264GT B2U3 PQFP
U10
U7A
MOUNT FOR +5V
MOUNT FOR 3.3V
FOR HARDWARE DISABLE
FROM M1533 GPIO
SOFEWARE DISABLE VGA
264VT-5
SOLS125
XTALIN
XTALOUT
MLOOP
ROMCS#/MGNT
PLOOP
RSET
COMP
VREF
VSYNC
HSYNC
RESET#
CPUCLK
IDSEL
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
IRDY#
PIXEL0
PIXEL1
PIXEL2
PIXEL3
PIXEL4
PIXEL5
PIXEL6
PIXEL7
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
CAS#/WE#0
MA11/CAS#
GIO(2)
R
G
B
GIO(3)
GNT#/MREQ
INTR#
TRDY#
DEVSEL#
STOP#
PAR
OE0#
OE1#/WE#/HCLK
EDCLK
GIO(7)
EVIDEO
ESYNC
BLANK#
CS(1)
CS(0)
GIO(6)
GIO(5)
GIO(9)
DCLK
ACER_AI_DESKTOP
P264GT
V58XA__97114
April 8, 1997
Sheet 22 of 34

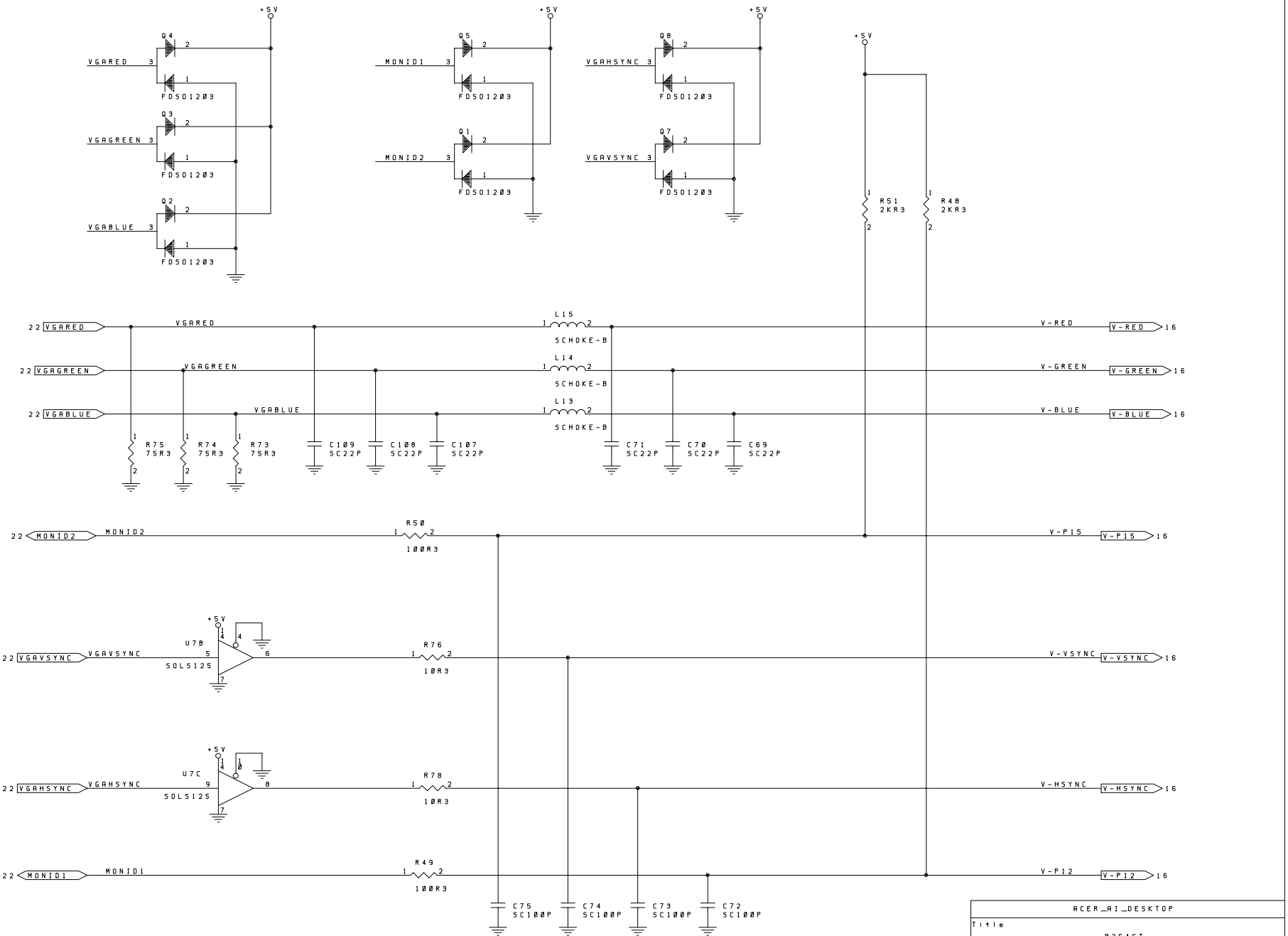




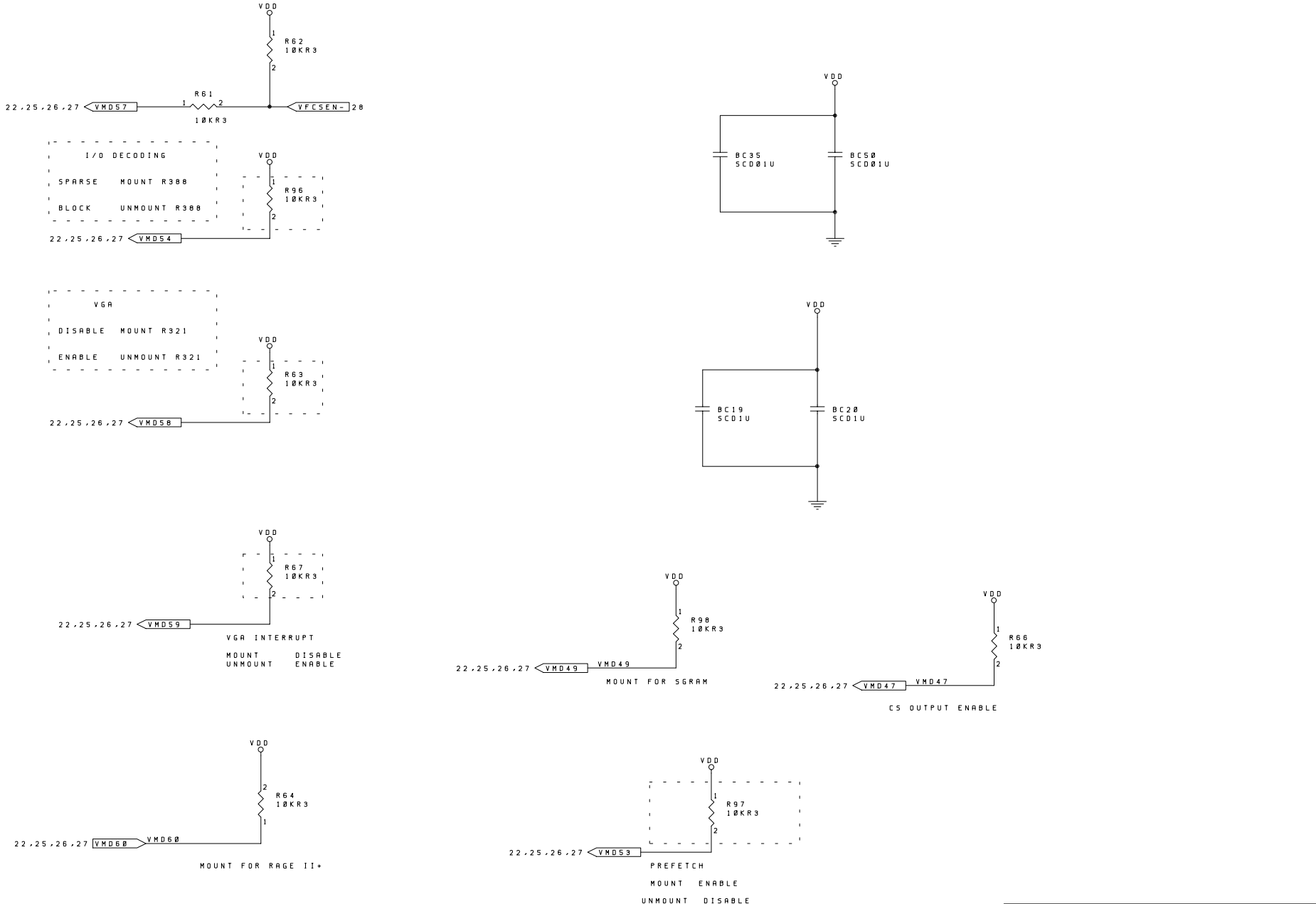




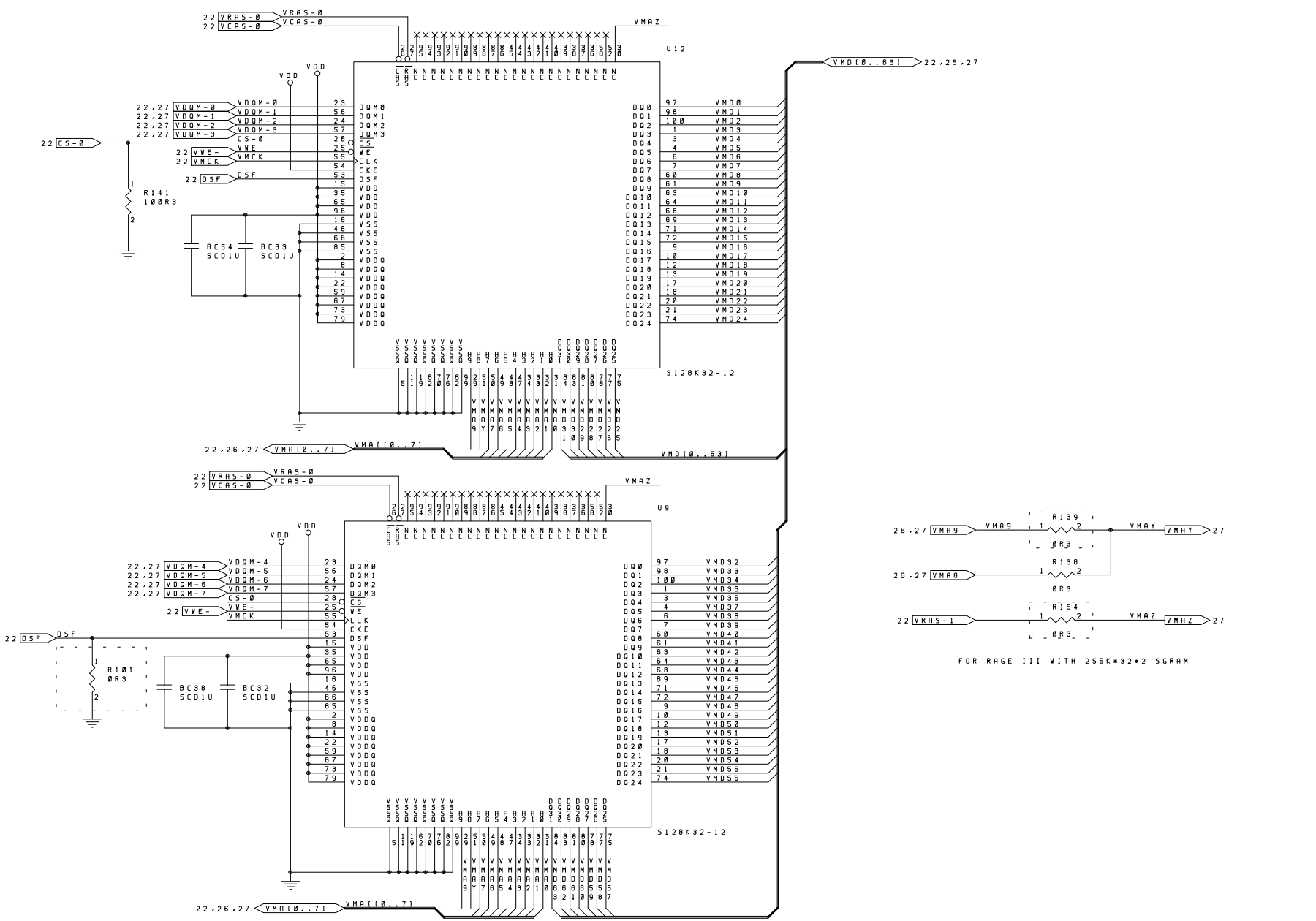
ACER_AI_DESKTOP		
Title: P264GT		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: April 8, 1997	Sheet 23 of 34	



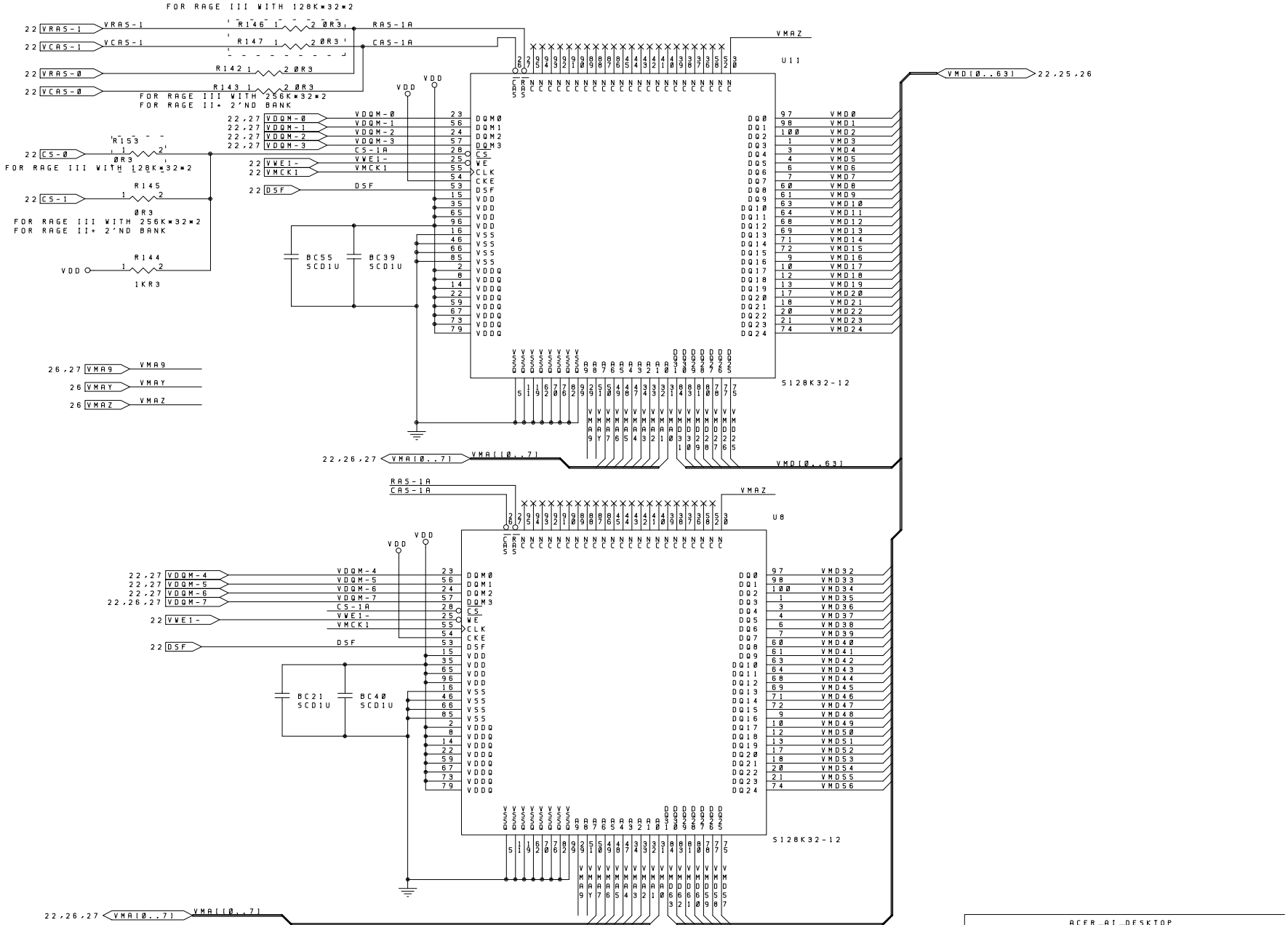
ACER_AI_DESKTOP		
Title: P264GT		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: April 8, 1997	Sheet 24 of 34	



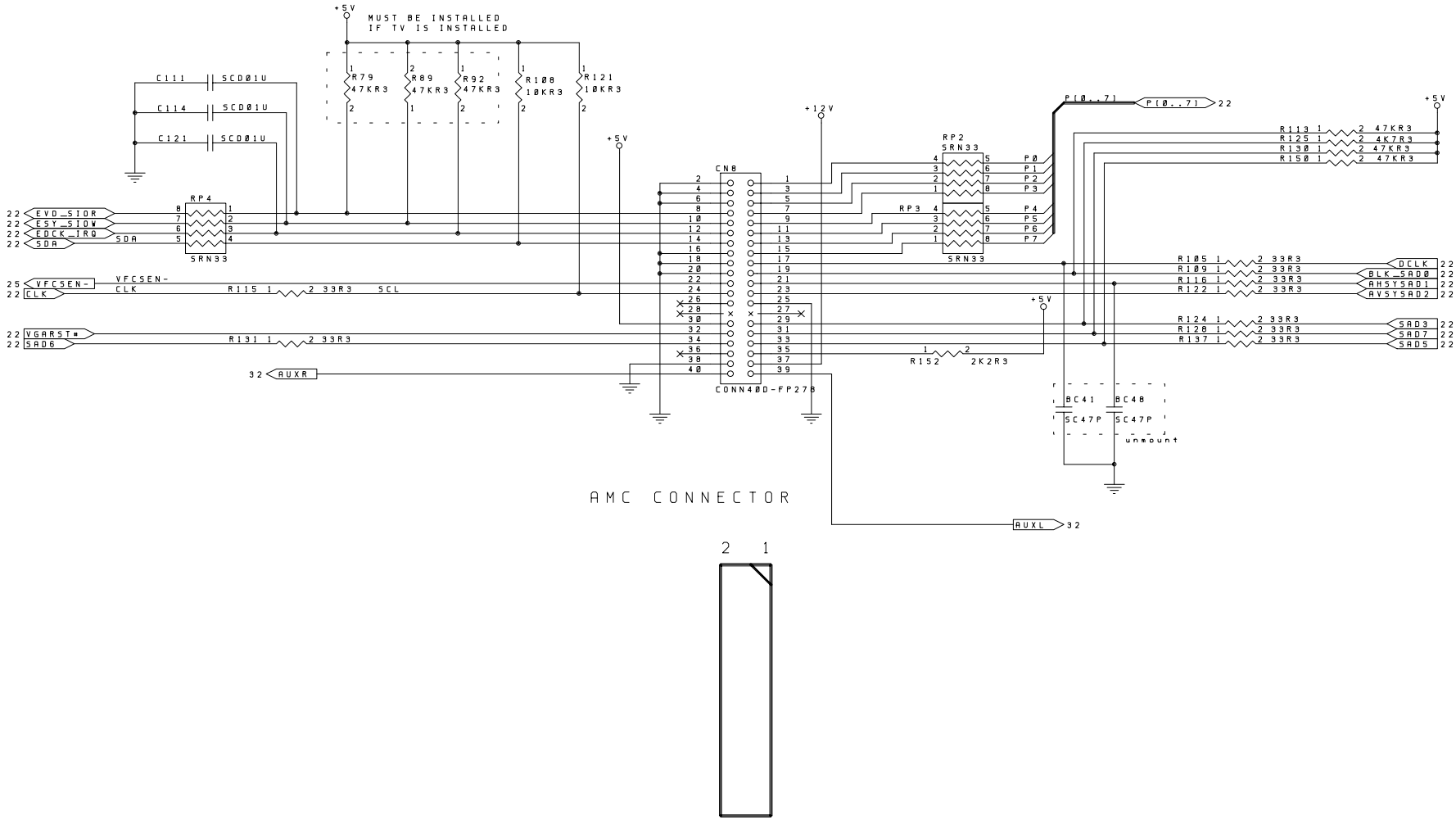
ACER_AI_DESKTOP		
Title: P264GT		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: April 8, 1997	Sheet 25 of 34	



ACER_AI_DESKTOP		
Title: P264GT		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: April 8, 1997	Sheet 26 of 34	



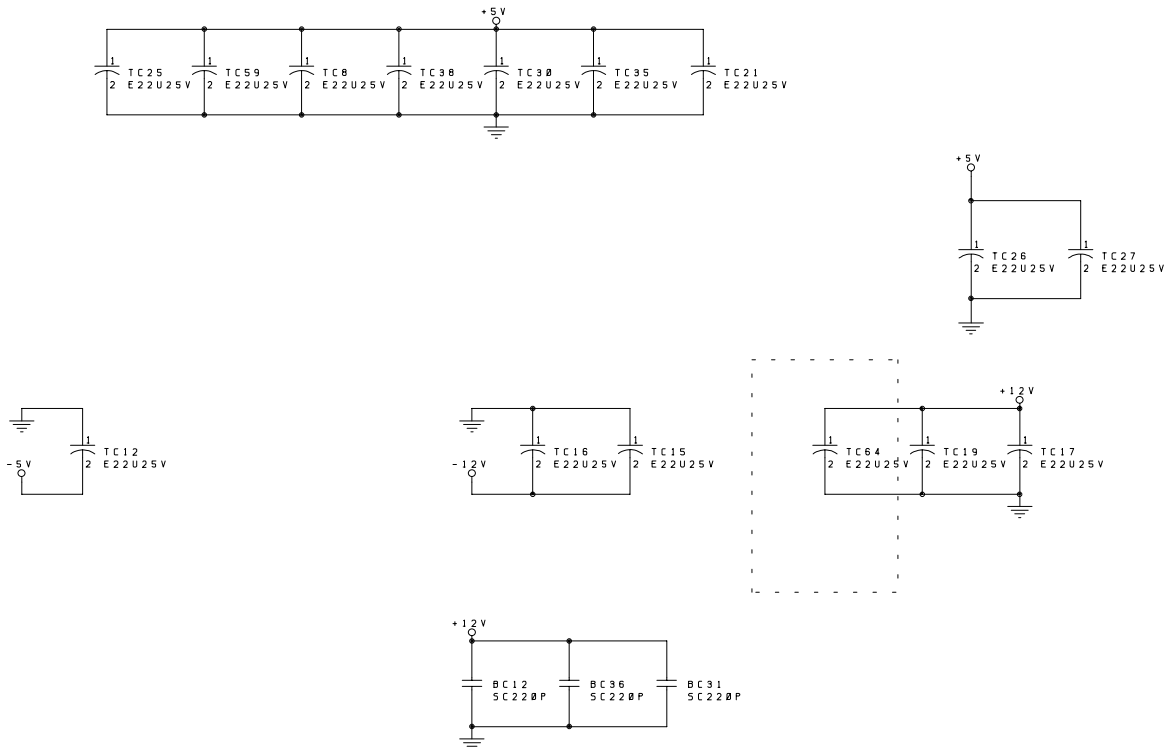
ACER_AI_DESKTOP		
Title: P264GT		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: April 8, 1997	Sheet 27 of 34	



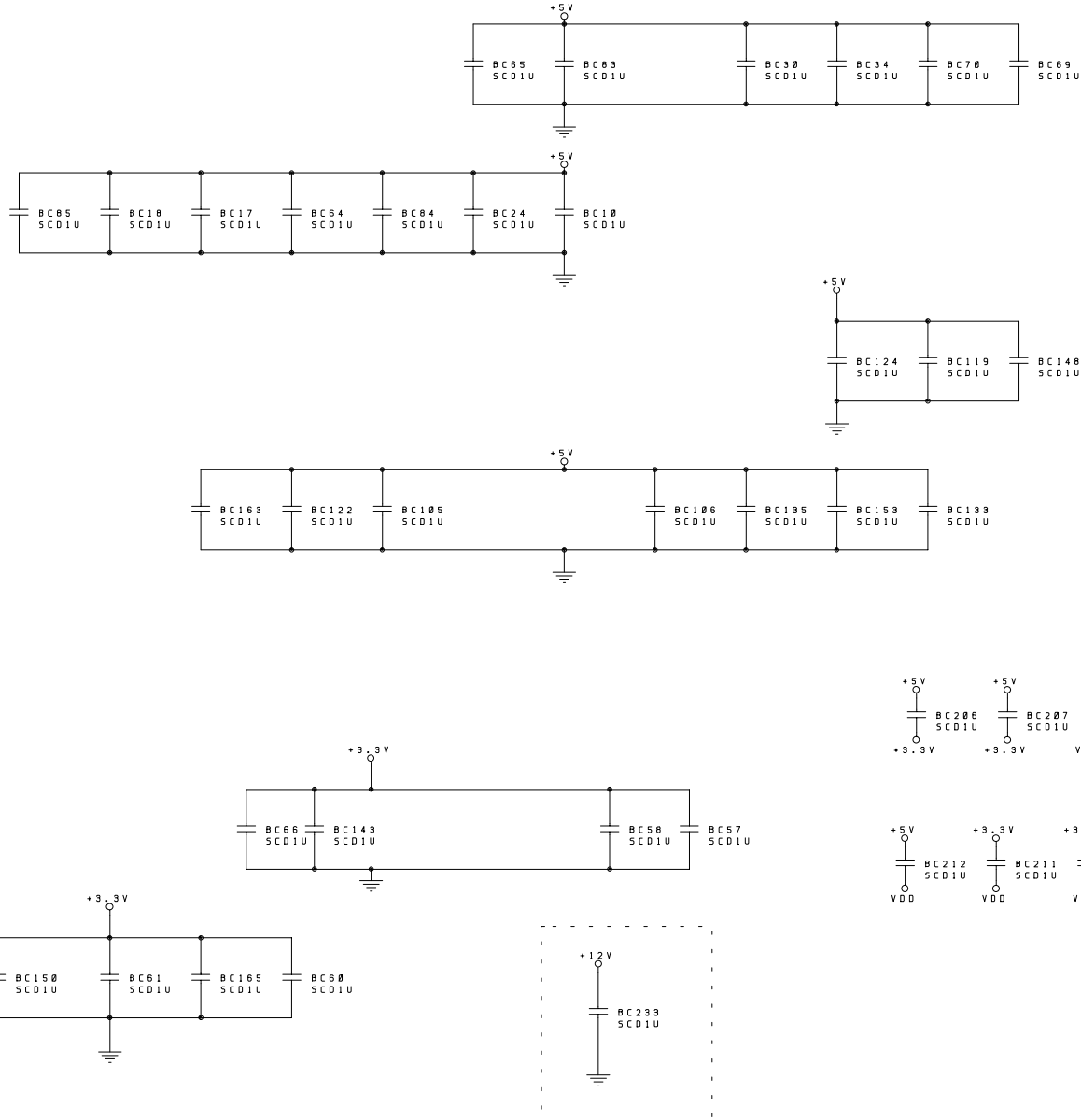
AMC CONNECTOR

2 1

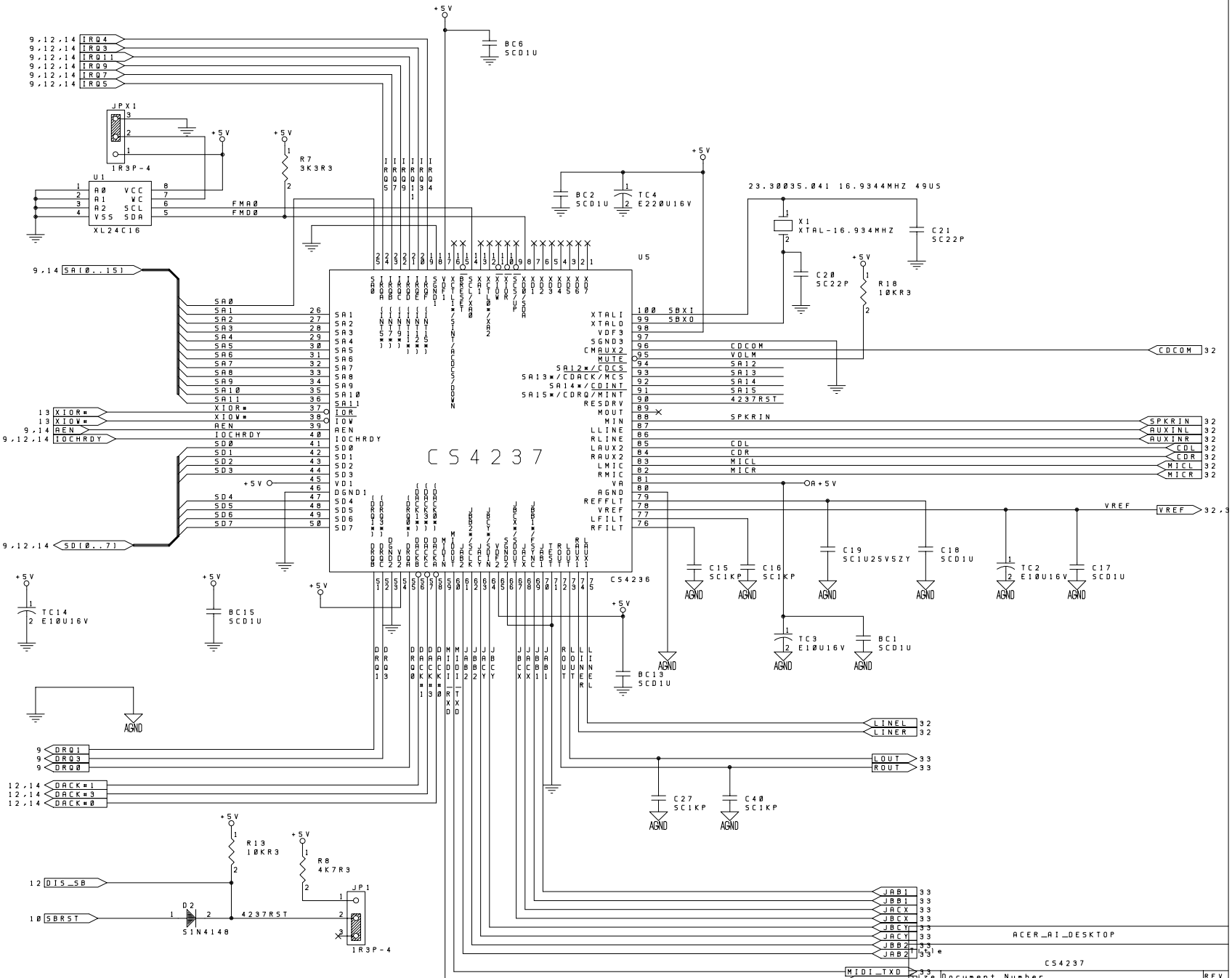
ACER_AI_DESKTOP		
Title: P264GT/ AMC CONNECTOR		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: April 8, 1997	Sheet 28 of 34	



ACER_AI_DESKTOP		
Title: BULK CAPACITORS		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: May 22, 1997	Sheet 29 of 34	



ACER_AI_DESKTOP		
Title: BYPASS CAPACITORS		
Size: A3	Document Number: V58XA__97114	REV: 5B
Date: May 22, 1997	Sheet 30 of 34	


CS4237
CS4236
U5
U1
XL24C16
JPX1
1R3P-4
JP1
S1N4148
D2
R7 3K3R3
R8 4K7R3
R13 10KR3
R18 10KR3
BC6 SCD1U
BC2 SCD1U
TC4 E220U16V
X1 XTAL-16.934MHZ
C21 SC22P
C20 SC22P
23.30035.041 16.9344MHZ 49US
TC14 E10U16V
BC15 SCD1U
C15 SC1KP
C16 SC1KP
C19 SC1U25V5ZY
C18 SCD1U
TC2 E10U16V
C17 SCD1U
TC3 E10U16V
BC1 SCD1U
BC13 SCD1U
C27 SC1KP
C40 SC1KP
AGND
+5V
VREF
CDCOM
SPKRIN
AUXINL
AUXINR
CDL
CDR
MICL
MICR
LINEL
LINER
LOUT
ROUT
IRQ4
IRQ3
IRQ11
IRQ9
IRQ7
IRQ5
SA0
SA1
SA2
SA3
SA4
SA5
SA6
SA7
SA8
SA9
SA10
SA11
SA12
SA13
SA14
SA15
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
XIOR#
XIOW#
AEN
IOCHRDY
SBRST
DIS_SB
DRQ1
DRQ3
DRQ0
DACK#1
DACK#3
DACK#0
FMA0
FMD0
JAB1
JBB1
JACX
JBCX
JBCY
JACY
JBB2
JAB2
MIDI_TXD
MIDI_RXD
4237RST
ACER_AI_DESKTOP
CS4237
Document Number
V58XA__97114
REV 5B
Date: May 16, 1997
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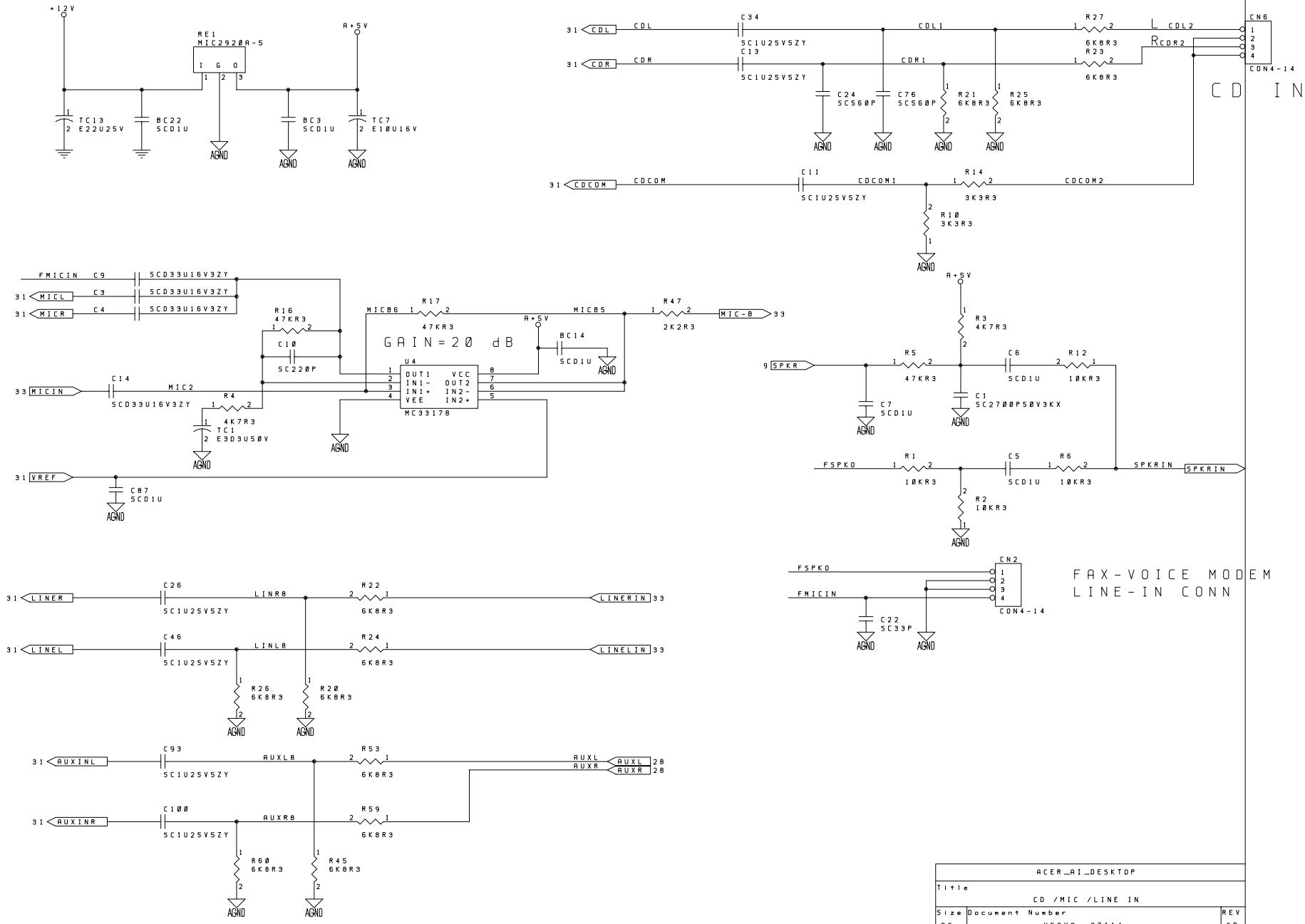
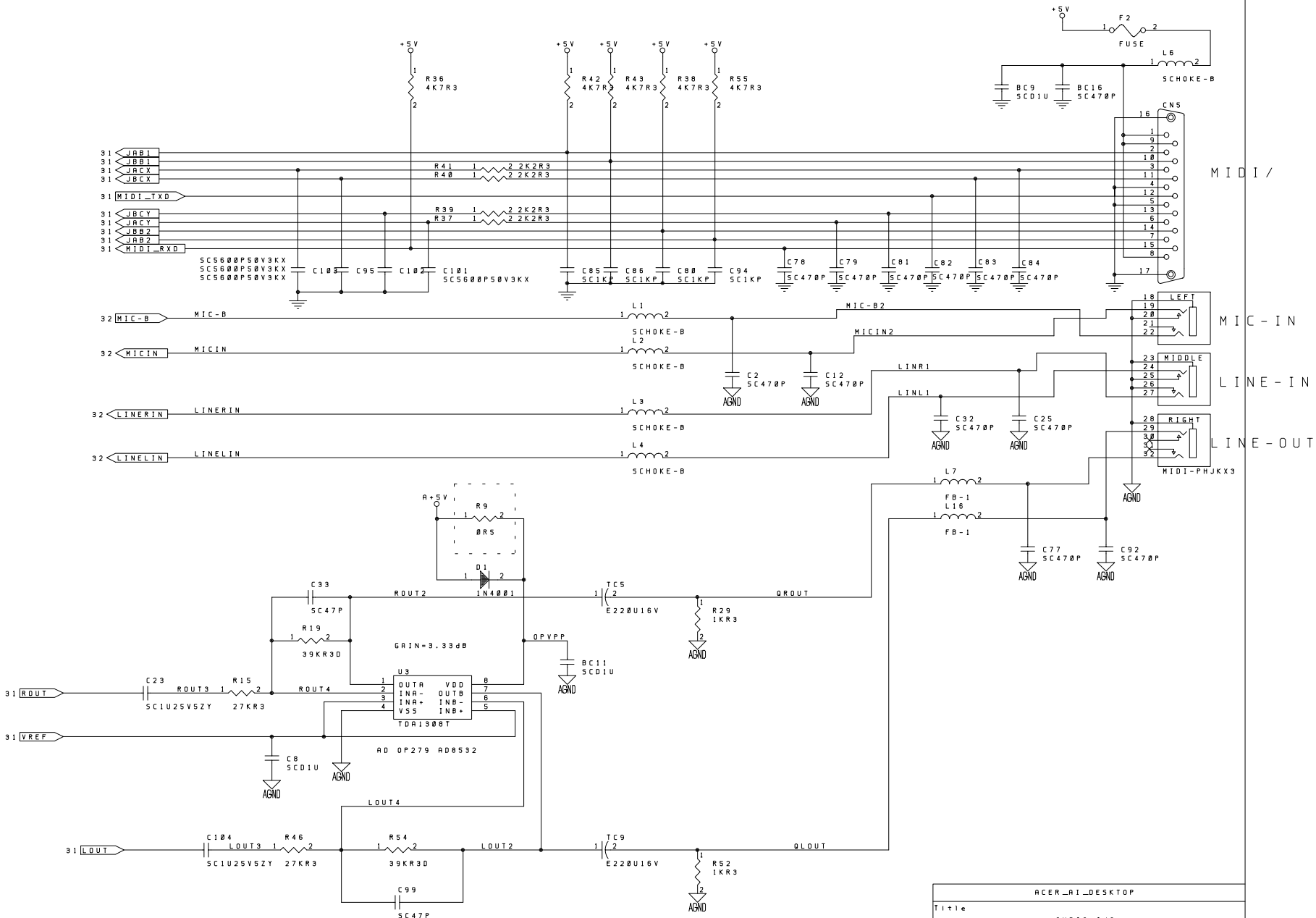
Size A3



ACER_AI_DESKTOP		
Title: CD /MIC /LINE IN		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: April 8, 1997	Sheet 32 of 34	


+5V
F2
FUSE
L6
5CHOKE-B
BC9
5CD1U
BC16
5C470P
CN5
MIDI/
R36
4K7R3
R42
4K7R3
R43
4K7R3
R38
4K7R3
R55
4K7R3
JAB1
JBB1
JBCX
JBCY
JBCY
JRB2
JRB2
MIDI_TXD
MIDI_RXD
R41
R40
R39
R37
2K2R3
SC5600P50V3KX
C103
C95
C102
C101
C85
5C1KP
C86
5C1KP
C80
5C1KP
C94
5C1KP
C78
C79
C81
C82
C83
C84
5C470P
MIC-B
MIC-B2
L1
5CHOKE-B
MIC-IN
MICIN
MICIN2
L2
5CHOKE-B
C2
C12
LINERIN
L3
5CHOKE-B
LINE-IN
LINELIN
L4
5CHOKE-B
LINR1
LINL1
C32
C25
LEFT
MIDDLE
RIGHT
MIDI-PHJX3
LINE-OUT
AGND
L7
FB-1
L16
FB-1
C77
C92
A+5V
R9
0R5
D1
1N4001
C33
5C47P
ROUT2
TC5
E220U16V
QROUT
R29
1KR3
R19
39KR3D
GAIN=3.33dB
OPVPP
BC11
5CD1U
U3
OUTA
INA-
INA+
VSS
VDD
OUTB
INB-
INB+
TDA1308T
C23
5C1U25V5ZY
ROUT3
R15
27KR3
ROUT4
ROUT
VREF
AD OP279 AD8532
C8
5CD1U
LOUT4
C104
5C1U25V5ZY
LOUT3
R46
27KR3
R54
39KR3D
LOUT2
TC9
E220U16V
QLOUT
R52
1KR3
C99
5C47P
LOUT
ACER_AI_DESKTOP
Title
AUDIO I/O
Size
A3
Document Number
V58XA__97114
REV
SB
Date: April 7, 1997
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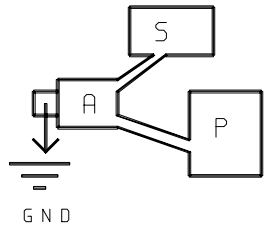

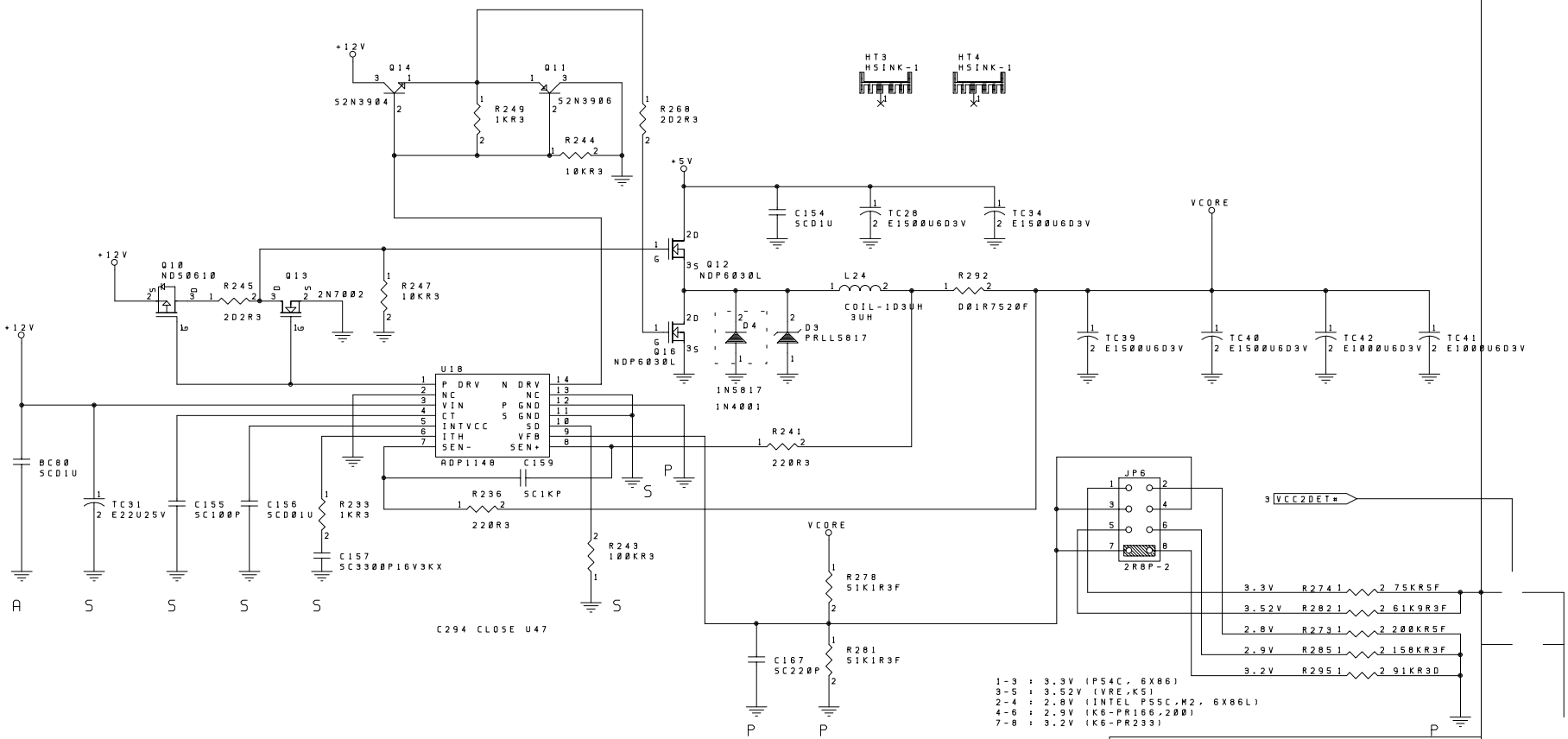

ACER_AI_DESKTOP		
Title: SWITCH POWER		
Size: A3	Document Number: V58XA__97114	REV: SB
Date: May 21, 1997	Sheet 34 of 34	