C440GX+ Server Board Specification Update

Release Date: June 1999

Order Number: 245192-001

The C440GX+ Server Board may contain design defects or errors known as errata that may cause the product to deviate from the published specifications. Current characterized errata are documented in this Specification Update.

REVISION HISTORY

Date of Revision	Description
June, 1999	This document is the first Specification Update for the C440GX+ Server Board.

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PREFACE

This document is an update to the specifications contained in the *C440GX+ Server Board Technical Product Specification (Order Number 245191)*, the *Intel Cabrillo-C Chassis Technical Product Specification (Order Number 245217).* It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Specification Clarifications, Errata, and Document Changes.

Refer to the *Pentium® II Xeon™ Processor Specification Update* (Order Number 243776) for specification updates concerning the Pentium II Xeon™ processors. Items contained in the Pentium® II Xeon™ Processor Specification Update that either do not apply to the C440GX+ Server Board or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Refer to the latest *Intel 82440GX AGPset Specification Update* for specification updates concerning the Intel 82440GX AGPset. Items contained in these Specification Updates that either do not apply to the C440GX+ Server Board or have been worked around are noted in this document. Otherwise, it should be assumed that any AGPset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revisions(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications for the C440GX+ Server Board. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the C440GX+ Server Board to deviate from published specifications. Hardware and software designed to be used with any given processor stepping must assume that all errata documented for that processor stepping are present on all devices.

GENERAL INFORMATION

Identification Information

Below are the specific boards, BIOS and components covered by this update.

C440GX+

Baseboard PBA #	BIOS	BMC Firmware Rev.	
726134-403	Production 1	BMC 08	

Summary Table of Changes

The following tables indicate the Errata and the Document Changes that apply to the C440GX+ Server Board. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Intel intends to update the appropriate documentation in a future revision.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	Plans	ERRATA
1	Fix	ISC 1.8 shows the slot width for PCI Slot #4 as a 64 bit slot
2	No Fix	Turning on an external modem will power up the system
3	No Fix	Wake On LAN fails after AC power is applied to the board the 1st time
4	No Fix	The BMC will not generate SEL events for either Upper or Lower non-recoverable threshold crossings for analog sensors, even when enabled to do so.
5	No Fix	Manually re-arming digital sensors events via the “Re-Arm Sensor Event” command does not work.
6	No Fix	Single Processor Systems must have a Pentium® III Xeon™ or Pentium® II Xeon™ inserted into the Primary Processor slot and a Terminator in the Secondary Processor slot for proper functioning.
7	No Fix	BIOS boot block write protect jumper does not function

NO.	Plans	DOCUMENT CHANGES

ERRATA

1. ISC 1.8 shows the slot width for PCI Slot #4 as a 64 bit slot

Problem: PCI Slot-4 as referenced by ISC 1.8 shows a 64 bit slot when it is actually a 32 bit slot.

Workaround: None

Status: To be fixed in a future BIOS release

2. Turning on an external modem will power up the system

Problem: If the system is configured with the modem enabled and EMP is disabled, applying power to the modem will cause the system to power up. When an external modem is attached to either COM port, the system powers up when the modem is turned on.

Implication: This is a side effect of having the wake on ring event enabled

Workaround: If the system and modem are both powered at the same time with power state retention not set, both the system and modem will function as expected. Or, If the system has AC removed but the modem has AC power applied, both the modem and the system will function as expected.

Status: No Fix planned

3. Wake On LAN fails after AC power is applied to the board the 1st time

Problem: Failure only seen when a device is attached to the IMB connector that is powered when the board has ac power removed. This condition causes the 5V_stby rail to maintain 0.5V. This is enough power to hold the data stored in the SRAM of the BMC

Workaround: Cold Boot system after Wake On LAN fails the 1st time.

Status: No Fix

4. The BMC will not generate SEL events for either Upper or Lower non-recoverable threshold crossings for analog sensors, even when enabled to do so.

Problem: If the Baseboard Management Controller (BMC) detects an Upper or Lower value for a “Non-Recoverable” event, the event is not logged in the System Event Log (SEL). This affects all analog voltage, temperature and fan sensors.

Implications: If “Non-Recoverable” events are programmed into the Server Management Software, the Upper and Lower limits programmed for these events are not logged.

Workaround: Only program the BMC to log Upper and Lower limits for critical and Non-critical events.

Status: – No Fix for C440GX+. This will be addressed in future platforms.

5. Manually re-arming digital sensor events via the "Re-Arm Sensor Event" command does not work

Problem: Manually re-arming digital sensor events via the "Re-Arm Sensor Event" command does not work. This affects the digital fans and chassis intrusion sensor.

Workaround: None – The sensors will automatically re-arm when the sensor state goes from a triggered to a non-triggered state.

Status: No fix for C440GX+ - this will be addressed in future platforms

6. Single Processor Systems must have a Pentium® III Xeon™ or Pentium® II Xeon™ inserted into the Primary Processor slot and a Terminator in the Secondary Processor slot for proper functioning.

Problem: The VRM labeled "Primary VRM" is used to power both L2 caches and receives voltage setting information from the primary processor only.

Workaround: Single processor C440GX+ based server systems must have their primary processor slot populated with a Pentium® III Xeon™ or Pentium® II Xeon™ Processor.

Status: No fix for C440GX+ - this server functions as designed.

7. BIOS boot block write protect jumper does not function.

Problem: The BIOS boot block write protect jumper does not actually prevent the Intel Pflash* utility from writing over the boot block. This cannot occur using the typical Iflash* utility provided for post-release BIOS updates. At the beginning of an update, BIOS checks the utility to make sure it is an Intel Pflash utility. If it is not an Intel Pflash* utility, or if it is a third-party utility without the Pflash identifiers, BIOS aborts the update process and prevents any writes to the Boot Block area.

Workaround: Continue using the post-release BIOS updates as instructed. Most updates will consist of an automated batch file which will update the operational code only (non-boot block) using the Iflash utility. In the event that a Pflash utility is required, instructions in the Readme.txt will instruct the user on proper use.

Status: No fix.