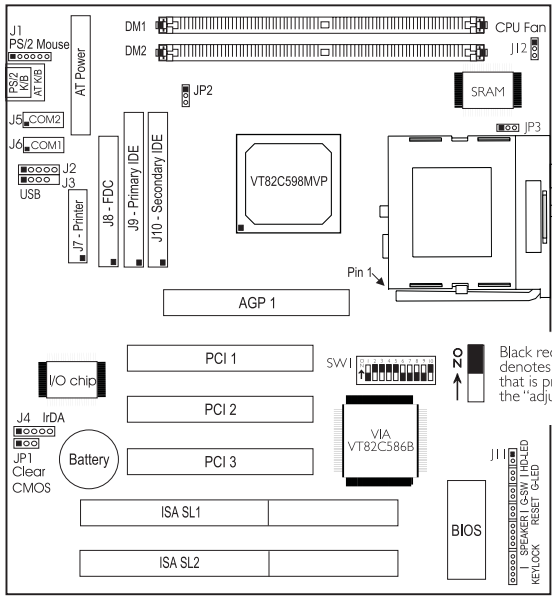
P5BV3+/e

rev. C+



AMD - SW1: 1-6	Cyrix - SW1: 1-6	IDT - SW1: 1-6
K6-2/266 - 66MHz - 4x	M II-200 - 66MHz - 2.5x	WinChip2-200 - 66MHz - 3x
K6-2/300 - 66MHz - 4.5x	M II-266 - 66MHz - 3x	WinChip2-225 - 75MHz - 3x
K6-2/300 - 100MHz - 3x	M II-300 - 66MHz - 3.5x	WinChip2-233 - 66MHz - 3.5x
K6-2/333 - 66MHz - 5x	M II-300 - 75MHz - 3x	WinChip2-240 - 60MHz - 4x
K6-2/333 - 95MHz - 3.5x	M II-333 - 66MHz - 4x	WinChip2-266 - 100MHz - 2.33x
K6-2/350 - 100MHz - 3.5x	M II-333 - 75MHz - 3.5x	WinChip2-300 - 100MHz - 2.5x
K6-2/366 - 66MHz - 5.5x	M II-333 - 83MHz - 3x	**Intel - SW1: 1-6**
K6-2/380 - 95MHz - 4x	M II-366 - 83MHz - 3.5x	MMX166MHz* - 66MHz - 2.5x
K6-2/400 - 100MHz - 4x	M II-366 - 100MHz - 2.5x	MMX200MHz - 66MHz - 3x
K6-2/450 - 100MHz - 4.5x	M II-380 - 100MHz - 3x	MMX233MHz - 66MHz - 3.5x
K6-III/400 - 100MHz - 4x	M II-400 - 95MHz - 3.5x	

*** denotes default setting

Voltage	JP3	SW1: 7-10
2.1V	1 2 3	ON
2.2V	1 2 3	ON
2.3V	1 2 3	ON
2.4V	1 2 3	ON
2.5V	1 2 3	ON
2.8V	1 2 3	ON
2.9V	1 2 3	ON
3.2V	1 2 3	ON
3.3V	1 2 3	ON
3.5V	1 2 3	ON

Jumper JP1 (CMOS Clear) - 1-2 On: Clear CMOS Data; 2-3 On: Normal (default)

Jumper JP2 (SDRAM Clcok)
1-2 On : SDRAM CLK = AGP CLK (default) ; 2-3 On : SDRAM CLK = CPU CLK

Note: Please refer to the user's manual for the settings of older CPU's.