Intel® Desktop Board YA810E
Technical Product Specification

December 1999

Order Number A00984-001

The Intel® Desktop Board YA810E may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board YA810E Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board YA810E Technical Product Specification.	December 1999

This product specification applies to only standard YA810E boards with BIOS identifier YA810E10A.86A.

Changes to this specification will be published in the Intel® Desktop Board YA810E Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the YA810E desktop board. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the YA810E board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on this board
2	A map of the resources of the board
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions which, if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the YA810E board, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
MB	Megabyte (1,048,576 bytes)
Mbit	Megabit (1,048,576 bits)
GB	Gigabyte (1,073,741,824 bytes)
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

5 Error Messages and Beep Codes

Figures

Tables

1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the YA810E board's major features.

Table 1. Feature Summary

Form Factor	FlexATX (9.0 inches by 7.5 inches)
Processor	Support for either an: • Intel® Pentium® III processor with 512 KB L2 cache (in an FCPGA package) • Intel® Celeron™ processor with 128 KB L2 cache (in a PGA package)
Memory	• Two 168-pin dual inline memory module (DIMM) sockets • Supports up to 512 MB of 100 MHz non-ECC synchronous DRAM (SDRAM) • Support for serial presence detect (SPD) and non-SPD DIMMs
Chipset	Intel® 810E chipset, consisting of: • Intel® 82810E Graphics/Memory Controller Hub (GMCH) • Intel® 82801AA I/O Controller Hub (ICH) • Intel® 82802AB 4 Mbit Firmware Hub (FWH)
Direct AGP Video	• Intel 82810E DC-133 GMCH • VGA port connector on back panel
Audio	Audio Codec '97 (AC'97) compatible audio subsystem, consisting of the following: • Intel 82801AA ICH (AC link output) • Analog Devices AD1881 analog codec
I/O Control	LPC47B277 Low Pin Count (LPC) I/O controller
Peripheral Interfaces	• Three back-panel mounted universal serial bus (USB) ports • Two IDE interfaces with Ultra DMA support
BIOS	• Intel/AMI BIOS stored in an Intel 82802AB 4 Mbit firmware hub (FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS
LAN Controller	Intel® 82559 local area network (LAN) controller
Instantly Available PC	• Support for *PCI Local Bus Specification*, Revision 2.2 • Suspend-to-RAM support • Wake from USB ports

NOTE

The YA810E board is designed to support only USB-aware operating systems.

For information about	Refer to
The board's compliance level with ACPI, Plug and Play, and SMBIOS	Table 3, page 16

1.1.2 Manufacturing Options

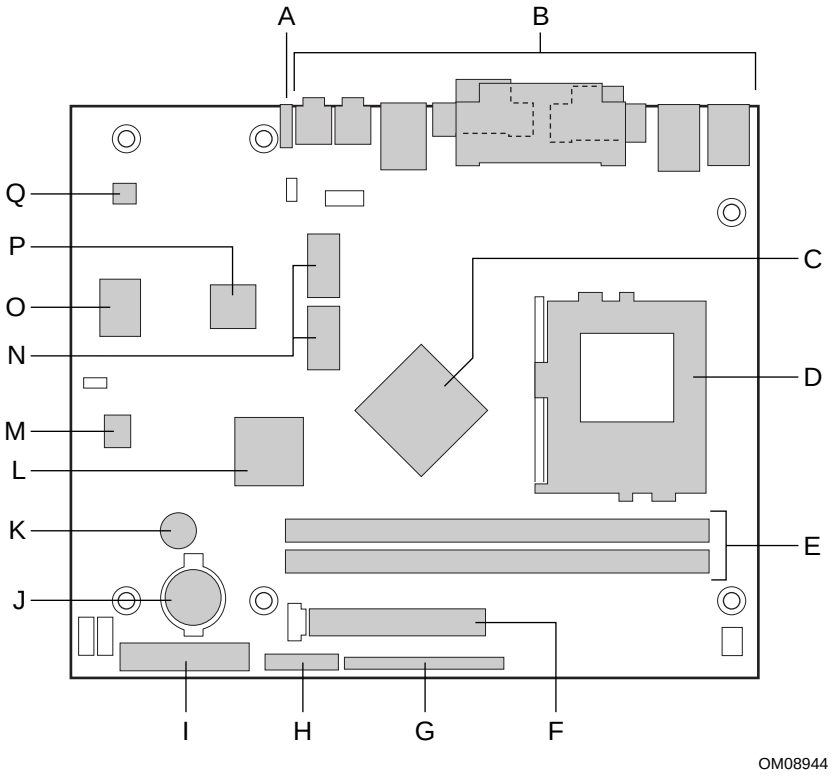
Table 2 describes the YA810E board's manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 2. Manufacturing Options

Legacy I/O Connectors	• One back panel 9-pin serial port connector, or one internal serial port connector • One back panel 25-pin parallel port connector • PS/2 keyboard and mouse connectors
Diagnostic LEDs	Extended diagnostics back-panel four-LED set
USB	Two internal USB ports are available for front panel access
Slimline IDE	ATA-5 compliant connector
Enhanced Video	4 MB SDRAM display cache (optional)
Management Level 4	Hardware monitor

1.1.3 YA810E Board Layout

Figure 1 shows the location of the major components on the YA810E board.



A	Diagnostic LEDs	J	Battery
B	Back panel connectors	K	Speaker
C	Intel 82810E GMCH (Graphics/Memory Controller Hub)	L	Intel 82801AA ICH (I/O Controller Hub)
D	Processor socket	M	Intel 82802AB FWH (Firmware Hub)
E	DIMM sockets	N	4 MB display cache (optional)
F	Primary IDE connector	O	SMSC LPC47B277 I/O Controller
G	Secondary IDE connector (Slimline)	P	Intel 82559 Ethernet Controller
H	Front panel connector	Q	AD1881 Audio Codec
I	Power connector		

Figure 1. YA810E Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the YA810E board.

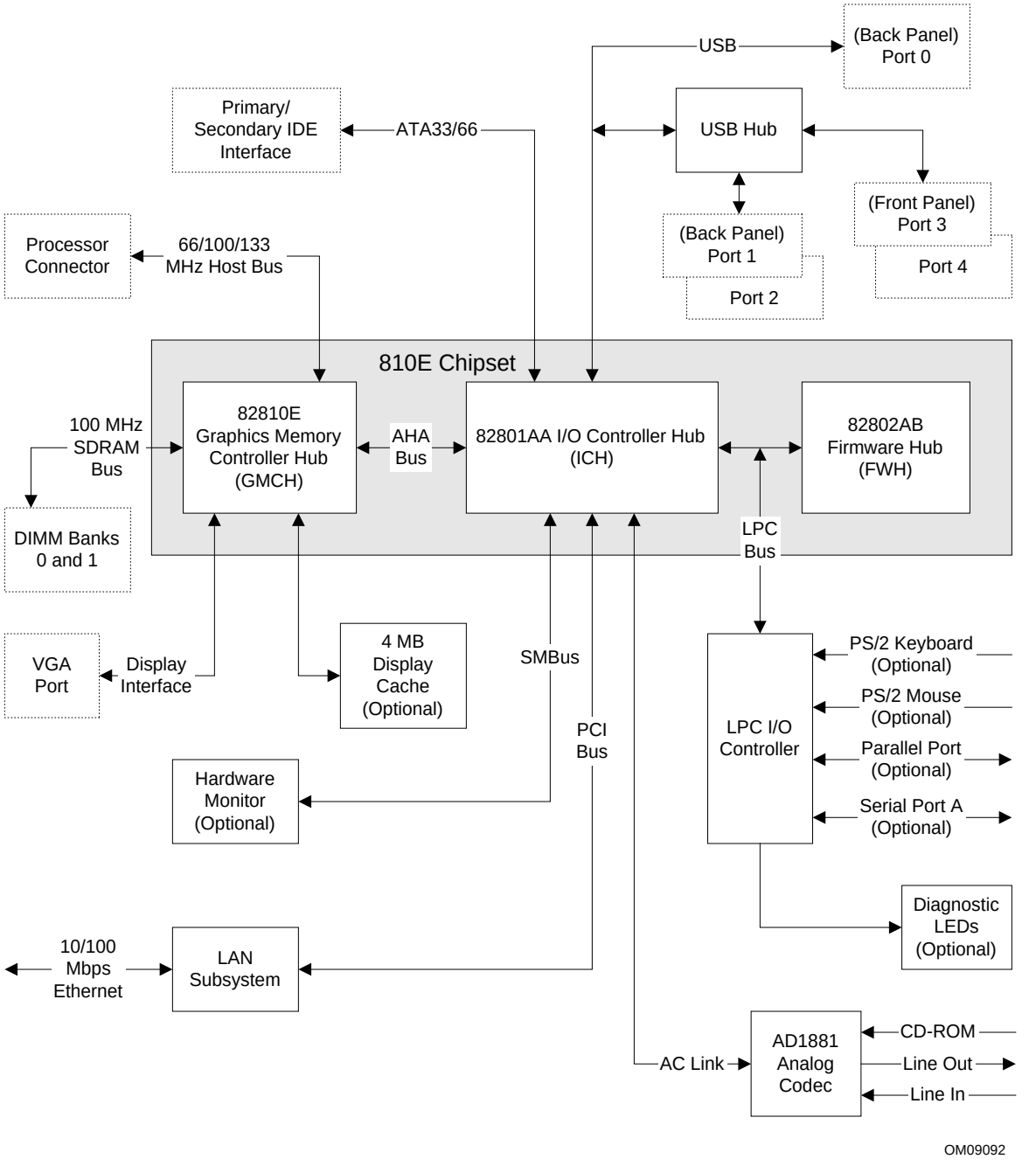


Figure 2. Block Diagram

1.2 Online Support

Find information about YA810E desktop boards under “Product Info” or “Customer Support” at these World Wide Web sites:

http://www.intel.com/design/motherbd
http://support.intel.com/support/motherboards/desktop

1.3 Design Specifications

Table 3 lists the specifications applicable to the YA810E board.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	This specification is available from:
AC ‘97	*Audio Codec ‘97*	Version 2.1, May 1998, Intel Corporation.	ftp://download.intel.com/pc-supp/platform/ac97
ACPI	*Advanced Configuration and Power Interface Specification*	Version 1.0b, July 1, 1998, Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification* (2X only)	Version 2.0, May 4, 1998, Intel Corporation.	the Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, 1999 American Megatrends, Inc.	http://www.amibios.com, or http://www.ami.com/download/amibios99.pdf
ATA-3	*Information Technology - AT Attachment-3 Interface, X3T10/2008D*	Version 6, October 1998, ASC X3T10.	ATA Anonymous FTP Site: ftp://www.dt.wdc.com/ata/ata-3/
ATA-5	*Information Technology - AT Attachment-3 Interface, X3T10/2008D*	Version 6, October 1998, ASC X3T10.	ATA Anonymous FTP Site: ftp://www.dt.wdc.com/ata/ata-3/
ATAPI	*Information Technology AT Attachment with Packet Interface Extensions T13/1153D*	Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology.	T13 Anonymous FTP Site: ftp://fission.dt.wdc.com/x3t13/project/d1153r18.pdf
ATX	*ATX Specification*	Version 2.01, February 1997, Intel Corporation.	http://developer.intel.com/design/motherbd/atx.htm
El Torito	*Bootable CD-ROM format specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd. and IBM Corporation.	the Phoenix Web site at: http://www.ptltd.com/techs/specs.html

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	This specification is available from:
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
FlexATX	FlexATX Addendum to the microATX Specification, Version 1.0	Version 1.0 March 1999, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/FlexATXaddn1_01.pdf
MicroATX	*microATX Motherboard Interface Specification*	Version 1.0, December 1997, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/
	SFX Power Supply Design Guide	Version 1.0, December 1997, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/microatx/sfx11_ps.pdf
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	ftp://download.intel.com/ial/wfm/bio10a.pdf
SDRAM DIMMs (64-and 72-bit)	*PC SDRAM Unbuffered DIMM Specification*	Version 1.0, February 1998, Intel Corporation.	http://www.intel.com/design/chipsets/memory/
	PC SDRAM DIMM Specification	Version 1.5, November 1997, Intel Corporation.	http://www.intel.com/design/chipsets/memory/
	PC Serial Presence Detect (SPD) Specification	Version 1.2A, December 1997, Intel Corporation.	http://www.intel.com/design/chipsets/memory/
SMBIOS	*System Management BIOS*	Version 2.3.1, August 12, 1998, Award Software International Inc., Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, American Megatrends Inc., SystemSoft Corporation, and Compaq Computer Corporation.	http://developer.intel.com/ial/wfm/design/smbios

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	This specification is available from:
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://www.usb.org/developers
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC.	http://www.usb.org/developers
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

CAUTION

The YA810E board supports processors that draw a maximum of 22 A. Using a processor that draws more than 22 A can damage the processor, the board, and the power supply. See the processor's data sheet for current usage requirements.

CAUTION

Before installing or removing the processor, make sure that AC power has been removed by unplugging the power cord from the computer. Failure to do so could damage the processor and the board.

The YA810E board supports either an Intel Pentium III processor (FCPGA package), or an Intel Celeron processor (PGA package) as shown in Table 4. The host bus speed is automatically selected.

Table 4. Supported Processors

Processor Type	Processor Designation	Host Bus Speed (MHz)	L2 Cache Size (KB)
Pentium III processors	500E, 550E, and 600E	100	512
	533B and 600B	133	512
	533EB, 600EB, 667, and 733	133	256
Celeron processors	300A, 333, 366, 400, 433, 466, 500, and 533	66	128

All supported onboard memory can be cached, up to the cachability limit of the processor.

For information about	Refer to
Processor support for the YA810E board	http://support.intel.com/support/motherboards/desktop
Processor data sheets	http://www.intel.com/design/litcentr

1.5 System Memory

⚠ CAUTION

To be compliant with applicable Intel® SDRAM memory specifications, the YA810E board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, the BIOS will attempt to configure the memory controller for normal operation; however, the DIMMs may not function at their optimum speed.

⚠ CAUTION

Before installing or removing memory, make sure that AC power has been removed by unplugging the power cord from the computer. Failure to do so could damage the memory and the board.

⚠ CAUTION

Because the main system memory is also used as video memory, the board requires 100 MHz SDRAM DIMMs even though the processor's host bus speed is 66 MHz. It is highly recommended that SPD DIMMs be used, since this allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted.

The YA810E board has two DIMM sockets. The minimum memory size is 16 MB and the maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Memory can be installed in one or both sockets. Memory size can vary between sockets.

The YA810E board supports the following memory features:

- 3.3 V, 168-pin DIMMs with gold-plated contacts
- 100 MHz SDRAM
- Serial Presence Detect (SPD) or non-SPD memory (BIOS recovery requires SPD DIMMs)
- Non-ECC (64-bit) memory
- Unbuffered single- or double-sided DIMMs

The board is designed to support DIMMs in the configurations listed in Table 5 below.

Table 5. System Memory Configuration

DIMM Size	Non-ECC Configuration
16 MB	2 Mbit x 64
32 MB	4 Mbit x 64
64 MB	8 Mbit x 64
128 MB	16 Mbit x 64
256 MB	32 Mbit x 64

For information about	Refer to
The *PC Serial Presence Detect Specification*	Table 3, page 16
Obtaining copies of PC SDRAM specifications	http://www.intel.com/design/pcisets/memory

1.6 Intel® 810E Chipset

The Intel 810E chipset consists of the following devices:

- 82810E Graphics Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801AA I/O Controller Hub (ICH) with AHA bus
- 82802AB Firmware Hub (FWH)

The chipset provides the host, memory, display, and I/O interfaces shown in Figure 3.

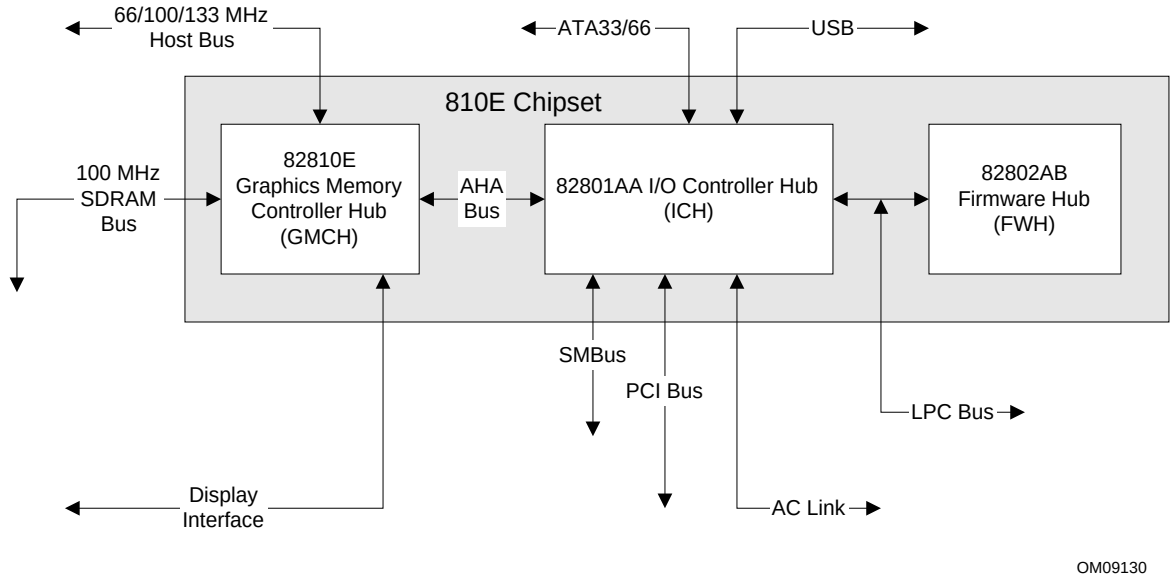


Figure 3. Intel 810E Chipset Block Diagram

For information about	Refer to
The Intel 810E chipset	http://www.developer.intel.com
The resources used by the chipset	Chapter 2
The chipset's compliance with ACPI and AC '97	Table 3, page 16

1.6.1 Direct AGP

Direct (integrated) AGP is a high-performance bus (independent of the PCI bus) for graphics-intensive applications, such as 3D applications. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

For information about	Refer to
The location of the VGA port connector	Figure 6, page 46
Obtaining the *Accelerated Graphics Port Interface Specification*	Table 3, page 16

1.6.2 USB

The YA810E board has five USB ports; one USB peripheral can be connected to each port. For more than five USB devices, an external hub can be connected to any of the ports. Three USB ports are implemented with stacked back panel connectors. The other two ports can be routed via a cable to the front panel. The YA810E board fully supports UHCI and uses UHCI-compatible software drivers. USB features include:

- Support for self-identifying peripherals that can be connected or disconnected while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 6, page 46
The signal names of the USB connectors on the back panel	Table 19, page 47
The location of the USB connectors on the front panel	Figure 7, page 50
The signal names of the USB connectors on the front panel	Table 32, page 53
The USB and UHCI specifications	Table 3, page 16

1.6.3 IDE Support

The YA810E board has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 56 on page 85

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The YA810E board supports laser servo (LS-120) diskette technology through its IDE interfaces. The LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

The board has two IDE interface connectors. The primary IDE connector is a standard 40-pin IDE interface. The secondary IDE connector is a 50-pin Slimline IDE connector, intended for use with devices such as 2.5-inch hard disk drives and mobile CD-ROM drives. The Slimline IDE connector has the standard IDE interface pins but also includes audio and power signals.

For information about	Refer to
The location of the IDE connectors	Figure 7, page 50
The signal names of the primary IDE connector	Table 28, page 51
The signal names of the Slimline IDE connector	Table 29, page 52
BIOS Setup program's Boot menu	Table 60, page 89

1.6.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, standard defaults, not custom defaults, will be loaded into CMOS SRAM at power on.

NOTE

The recommended method of accessing the date in systems with Intel® desktop boards is indirectly from the Real-Time Clock (RTC) via the BIOS. The BIOS on Intel desktop boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For information about	Refer to
Proper date access in systems with Intel desktop boards	http://support.intel.com/support/year2000/

1.7 I/O Controller

The LPC47B277 I/O controller provides the following features:

- Low pin count (LPC) interface
- 3.3V operation
- One serial port (optional)
- Plug and Play compatible register set
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support (optional)
- PS/2-style mouse and keyboard interfaces (optional)
- Intelligent power management, including a programmable wake up event interface
- PME (Power Management Event) interface
- Fan control:
  - One fan control output
  - One fan tachometer input

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
The LPC47B277 I/O controller	www.smsc.com/main/catalog/lpc47b27x.html

1.7.1 Serial Port (Optional)

The YA810E board has one serial port connector the location of which is a manufacturing option. The serial port's NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial port can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
The location of the back panel serial port connector	Figure 6, page 46
The signal names of the back panel serial port connector	Table 20, page 47
The location of the optional midboard serial port connector	Figure 7, page 50
The signal names of the optional midboard serial port connector	Table 35, page 54

1.7.2 Parallel Port (Optional)

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (PC AT†-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 6, page 46
The signal names of the parallel port connector	Table 21, page 48

1.7.3 PS/2 Keyboard and Mouse (Optional)

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the power-on self-test (POST).

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 6, page 46
The signal names of the keyboard and mouse connectors	Table 18, page 47

1.8 Graphics Subsystem

The Intel 82810E DC-133 GMCH graphics memory controller hub component provides the following graphics support features:

- Integrated 2-D and 3-D graphics engines
- Integrated hardware motion compression engine
- Integrated 230 MHz DAC

Table 6 lists the refresh rates supported by the graphics subsystem.

Table 6. Supported Graphics Refresh Rates

Resolution	Available Refresh Rates (Hz)
640 x 200 x 16 colors	70
640 x 350 x 16 colors	70
640 x 400 x 256 colors	60, 70, 75, 85
640 x 400 x 64 K colors	60, 70, 75, 85
640 x 400 x 16 M colors	70
640 x 480 x 16 colors	60, 72, 75, 85
640 x 480 x 256 colors	60, 70, 72, 75, 85
640 x 480 x 32 K colors	60, 75, 85
640 x 480 x 64 K colors	60, 70, 72, 75, 85
640 x 480 x 16 M colors	60, 70, 72, 75, 85
800 x 600 x 256 colors	60, 75, 85
800 x 600 x 32 K colors	60, 70, 72, 75, 85
800 x 600 x 64 K colors	60, 70, 72, 75, 85
800 x 600 x 16 M colors	60, 70, 72, 75, 85
1024 x 768 x 256 colors	60, 70, 75, 85
1024 x 768 x 32 K colors	60, 75, 85
1024 x 768 x 64 K colors	60, 70, 72, 75, 85
1024 x 768 x 16 M colors	60, 70, 72, 75, 85
1056 x 800 x 16 colors	70
1280 x 1024 x 256 colors	60, 70, 72, 75, 85
1280 x 1024 x 32 K colors	60, 75, 85
1280 x 1024 x 64 K colors	60, 70, 72, 75
1280 x 1024 x 16 M colors	60, 70, 72, 75, 85

For information about	Refer to
Obtaining graphics software and utilities	http://support.intel.com/support/motherboards/desktop

1.9 Audio Subsystem

The YA810E board includes an Audio Codec ’97 (AC ’97) compatible audio subsystem consisting of these devices:

- Intel 82801AA ICH (AC link output)
- Analog Devices AD1881 analog codec

Figure 4 is a block diagram of the audio subsystem.

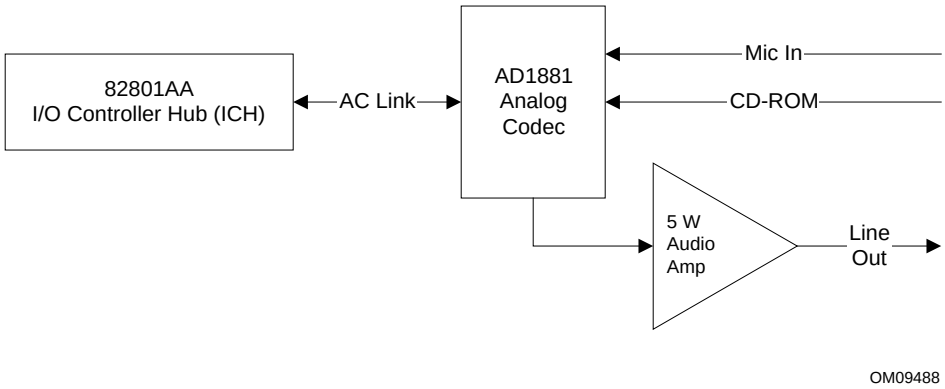


Figure 4. Block Diagram of Audio Subsystem with AD1881 Codec

Features of the audio subsystem include:

- Independent channels for PCM in, PCM out, and Mic in
- 16-bit stereo I/O up to 48 kHz
- Multiple sample rates

For information about	Refer to
Obtaining audio software and utilities	http://support.intel.com/support/motherboards/desktop

1.9.1 AD1881 Analog Codec

The AD1881 is a fully AC ’97 compliant codec. The codec's features include:

- 16-bit stereo full-duplex operation
- High quality CD-ROM input with ground sense
- Stereo line level output
- Power management support
- Full duplex variable sampling rate (7 kHz to 48 kHz) with 1 Hz resolution
- Phat† Stereo 3-D stereo enhancement

1.9.2 Audio Connectors

The audio connectors include the following:

- ATAPI CD-ROM (connects an internal ATAPI CD-ROM drive to the audio mixer)
- Line out (front panel audio connector and back panel)
- Line in (front panel audio connector and back panel)

For information about	Refer to
The location of the front panel audio connectors	Figure 7, page 50
The signal names of the front panel audio connectors	Table 26, page 51
The location of the ATAPI CD-ROM connector	Figure 7, page 50
The signal names of the ATAPI CD-ROM connector	Table 30, page 52
The back panel audio connectors	Section 2.8.1, page 46
The front panel line out connector	Section 2.8.3, page 55

NOTE

Some of the audio connectors are optional and are not installed on all versions of the board.

1.10 Hardware Monitor Component (Optional)

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+12, +5, +3.3, +2.5, V_{CCP}) to detect levels above or below acceptable values
- SMBus interface
- The hardware monitor component enables the board to be compatible with the Wired for Management (WfM) specification.

For information about	Refer to
The board's compatibility with the WfM specification	Table 3, page 16

1.11 LAN Subsystem

The Intel 82559 Fast Ethernet Wired for Management (WfM) PCI LAN subsystem provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit, 33 MHz direct bus mastering on the PCI bus
- 10Base-T and 100Base-TX capability using a single RJ-45 connector with connection and activity status LEDs
- IEEE 802.3u Auto-Negotiation for the fastest available connection
- Jumperless configuration; the LAN subsystem is completely software-configurable

For information about	Refer to
The WfM specification	Table 3, page 16

1.11.1 Intel® 82559 PCI LAN Controller

The Intel 82559 PCI LAN controller's features include:

- CSMA/CD Protocol Engine
- PCI bus interface
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - Complete functionality necessary for the 10Base-T and 100Base-TX network interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - A complete set of Media Independent Interface (MII) management registers for control and status reporting
  - 802.3u Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices, whether half- or full-duplex capable
  - Integrated power management features, including support for Wake on LAN† technology

For information about	Refer to
The LAN subsystem's PCI specification compliance	Table 3, page 16

1.11.2 LAN Subsystem Software

The Intel 82559 Fast Ethernet WfM PCI LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 16

1.11.3 RJ-45 LAN Connector LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec speed is selected.
	On	100 Mbit/sec speed is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.12 Power Management Features

Power management is implemented at several levels, including:

- Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN technology
  - Instantly Available† technology
  - Wake on Ring
  - Resume on Ring
  - Wake from USB
  - PME# wakeup support

1.12.1 ACPI

If the board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires the support of an operating system that provides full ACPI functionality. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to RAM sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 10 on page 34)
- Support for a front panel power and sleep mode switch. Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 8. Effects of Pressing the Power Switch

If the system is in this state…		…and the power switch is pressed for	…the system enters this state
Off	(ACPI G2/S5 state)	Less than four seconds	Power on
On	(ACPI G0 state)	Less than four seconds	Soft off/Suspend
On	(ACPI G0 state)	More than four seconds	Fail safe power off
Sleep	(ACPI G1 state)	Less than four seconds	Wake up
Sleep	(ACPI G1 state)	More than four seconds	Power off

For information about	Refer to
The board's compliance level with ACPI	Table 3, page 16

1.12.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the YA810E board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 9. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power*
G0 - working state	S0 - working	C0 - working	D0 - working state	Full power > 30 W
G1 - sleeping state	S1 - CPU stopped	C1 - stop grant	D1, D2, D3 - device specification specific.	5 W < power < 30 W
G1 - sleeping state	S3 - Suspend-to-RAM. Context saved to RAM.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G2/S5	S5 - Soft off. Context not saved. Cold boot is required.	No power	D3 - no power except for wake up logic.	Power < 5 W **
G3 - mechanical off. (AC power is disconnected from the computer.)	No power to the system.	No power	D3 - no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

* Total system power is dependent on the system configuration, including peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

1.12.1.2 Wake-Up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

Table 10. Wake Up Devices and Events

These devices/events can wake-up the computer…	…from this state
Power switch	S1, S3, S5
RTC alarm	S1, S3, S5
LAN	S1, S3
PME#	S1, S3
USB	S1, S3

1.12.1.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure devices that do not have other hardware standards for enumeration and configuration. PCI devices on a desktop board, for example, are not enumerated by ACPI.

1.12.2 Hardware Support

CAUTION

If Wake on LAN and Instantly Available technology features are used, the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.2 on page 63 for additional information.

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring
- Wake from USB
- PME# wakeup support

Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Wake on Ring and Resume on Ring enable telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (ACPI).

NOTE

The use of Wake on Ring, Resume on Ring, and Wake from USB technologies from an ACPI state require the support of an operating system that provides full ACPI functionality.

1.12.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the YA810E board can turn off the system power through software control.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

For information about	Refer to
The location of the power connector	Figure 7, page 50
The signal names of the power connector	Table 31, page 53
The ATX specification	Table 3, page 16

1.12.2.2 Fan Connectors

The board has two fan connectors, one of which is a manufacturing option. The functions of these connectors are described in Table 11.

Table 11. Fan Connector Descriptions

Connector	Function
Processor fan	Provides +12 V DC for a processor fan or active fan heatsink.
Chassis fan (optional)	Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer.

For information about	Refer to
The location of the fan connectors	Figure 7, page 50
The signal names of the processor fan connector	Table 27, page 51
The signal names of the chassis fan connector	Table 33, page 53

1.12.2.3 Wake on LAN Technology

CAUTION

For Wake on LAN technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply. Refer to Section 2.11.2 on page 63 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem, monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. The YA810E board supports Wake on LAN technology through the PCI bus PME# signal.

1.12.2.4 Instantly Available Technology

CAUTION

For Instantly Available technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when using this feature can damage the power supply. Refer to Section 2.11.2 on page 63 for additional information.

Instantly Available technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off. The power supply appears to be off, the fans are off, and the front panel power LED will be yellow (unless a single color LED is installed, in which case, it will be off.) See Table 37 and Table 38 for additional front panel LED information. When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 10 on page 34 lists the devices and events that can wake the computer from the S3 state.

The YA810E board supports the *PCI Bus Power Management Interface Specification.* For information on the versions of this specification, see Section 1.3.

1.12.2.5 Wake on Ring

NOTE

Wake on Ring requires the use of a modem (external USB, or modem connected to serial port A) that supports the Wake on Ring feature.

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from the ACPI S5 state
- Requires two calls to access the computer:
  - First call restores the computer.
  - Second call enables access (when the appropriate software is loaded).
- Detects incoming calls for external USB modems. The USB bus is monitored for the RING_DETECT signal.

1.12.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems

1.12.2.7 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.12.2.8 PME# Wakeup Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1 or S3 state.

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 – 2.6 contain several standalone tables. Table 12 describes the system memory map, Table 13 shows the I/O map, Table 14 lists the DMA channels, Table 15 defines the PCI configuration space map, and Table 16 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 1FFFFFFF	511 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 I/O Map

Table 13. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Controller (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte – reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD/STAT byte
0070 - 0071	2 bytes	System CMOS / Real-Time Clock (RTC)
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	Reserved
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
02E8 - 02EF[1]	8 bytes	COM4/video (8514A)
02F8 - 02FF[1]	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port

continued

Table 13. I/O Map (continued)

Address (hex)	Size	Description
03B0 - 03BB	12 bytes	Intel 82810E – DC100 Graphics/Memory Controller Hub (GMCH)
03C0 - 03DF	32 byte	Intel 82810E – Graphics/Memory Controller Hub (GMCH)
03E8 - 03EF	8 bytes	COM3
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0CF8 - 0CFB[2]	4 bytes	PCI configuration address register
0CF9[3]	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary		Desktop Board Resource
256 contiguous bytes starting on a 256-byte divisible boundary		ICH Audio Mixer
64 contiguous bytes starting on a 64-byte divisible boundary		ICH Audio Bus Mixer
32 contiguous bytes starting on a 32-byte divisible boundary		ICH (USB)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801AA PCI Bridge
32 contiguous bytes starting on a 32-byte divisible boundary		Intel 82559 LAN Controller
96 contiguous bytes starting on a 128-byte divisible boundary		LPC47B277 PME Status

Notes:

1. Default, but can be changed to another address range
2. Dword access only
3. Byte access only

NOTE

Some additional I/O addresses are not available due to ICH addresses aliasing. For information about ICH addressing, refer to the Intel web site at:

http://developer.intel.com/design/chipsets/datashts/

2.4 DMA Channels

Table 14. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio
2	8- or 16-bits	Open
3	8- or 16-bits	Open / Audio
4		Reserved - cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.5 PCI Configuration Space Map

Table 15. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82810E component
00	01	00	Graphics controller of Intel 82810E component
00	1E	00	Link to PCI bridge
00	1F	00	PCI-to-LPC bridge
00	1F	01	IDE controller
00	1F	02	USB controller #1
00	1F	03	SMBus controller
00	1F	04	Reserved
00	1F	05	AC '97 audio controller
00	1F	06	AC '97 modem controller
01	01	00	Intel 82559 PCI LAN controller

2.6 Interrupts

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2*
4	COM1*
5	Audio / User available
6	User available
7	LPT1 (Parallel port if present, or else, user available)
8	Real-time clock
9	Reserved for ICH system management bus
10	User available
11	User available
12	Onboard mouse port (if present, or else, user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, or else, user available)
15	Secondary IDE (if present, or else, user available)

* Default, but can be changed to another IRQ

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the onboard PCI devices. The PCI specification shows how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices.

The ICH PCI-to-LPC bridge has four programmable interrupt request (PIRQ) input signals. All PCI interrupt sources connect to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the YA810E board and therefore share the same interrupt.

Table 17 lists the PIRQ signals and shows how the signals are connected to the onboard PCI interrupt sources.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name			
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**
AGP Controller	INTA	INTB		
ICH Audio Controller		INTB		
ICH USB Controller				INTD
PCI LAN Controller				INTA

NOTE

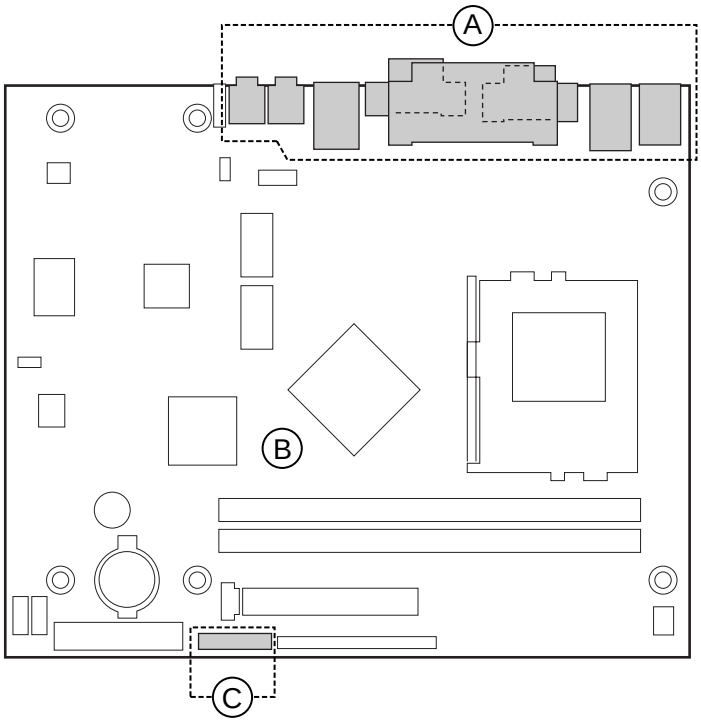
The ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 10, 11, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

CAUTION

Only the back panel connectors of the board and the front panel USB connectors have overcurrent protection. The other internal board connectors are not overcurrent protected and should connect only to devices inside the computer chassis such as fans and internal peripherals. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by an external device could cause damage to the computer, the interconnecting cable, and the external device itself.

This section describes the YA810E board's connectors. The connectors can be divided into three groups, as shown in Figure 5.



A. Back panel connectors (see page 46)

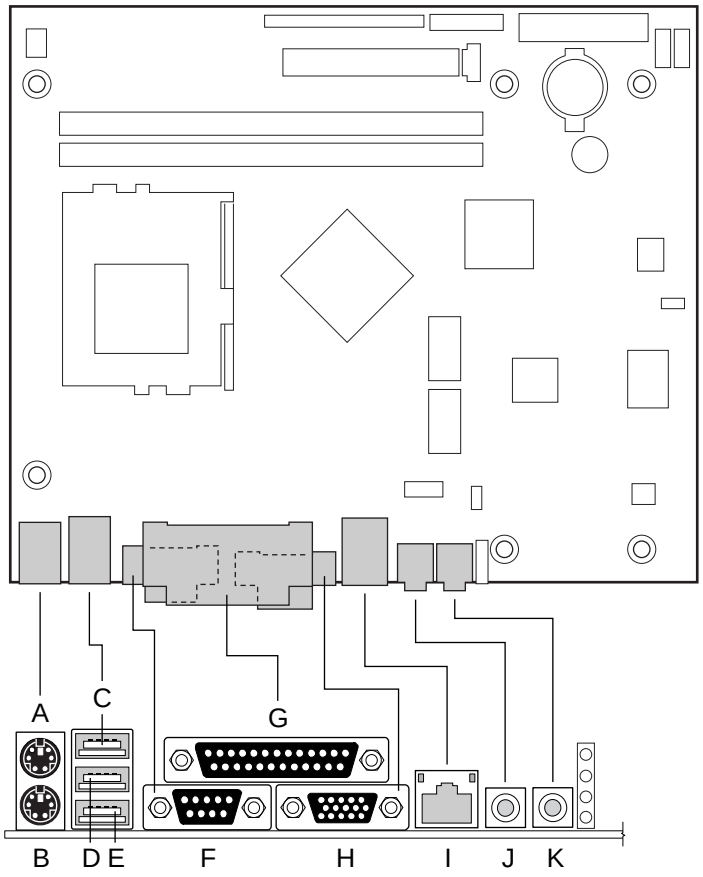
B. Midboard connectors (see page 49)

C. Front panel connectors (see page 55)

Figure 5. Connector Groups

2.8.1 Back Panel Connectors

Figure 6 shows the location of the back panel connectors.



Item	Description	Connector Color	For additional Information…
A	PS/2 mouse port	Lime green	See Table 18, page 47
B	PS/2 keyboard port	Purple	See Table 18, page 47
C	USB port 0	Black	See Table 19, page 47
D	USB port 1	Black	See Table 19, page 47
E	USB port 2	Black	See Table 19, page 47
F	Serial port A	Teal	See Table 20, page 47
G	Parallel port	Burgundy	See Table 21, page 48
H	VGA	Blue	See Table 22, page 48
I	LAN	Not color specific	See Table 23, page 49
J	Audio Line In	Lime green	See Table 24, page 49
K	Audio Line Out	Light blue	See Table 25, page 49

Figure 6. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.

Table 18. PS/2 Mouse/Keyboard (Optional)

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	Fused +5 V
5	Clock
6	Not connected

Table 19. USB Ports 0, 1, and 2

Pin	Signal Name
1	+5 V (fused)
2	USBP0# / USBP1# / USBP2#
3	USBP0 / USBP1 / USBP2
4	Ground

Table 20. Serial Port (Optional)

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	SIN# (Serial Data In)
3	SOUT# (Serial Data Out)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 21. Parallel Port (Optional)

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 – 25	GND	GND	GND

Table 22. VGA Port

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No connect
5	Ground
6	Ground
7	Ground
8	Ground
9	Fused VCC
10	Ground
11	No connect
12	MONID1
13	HSYNC
14	VSYNC
15	MONID2

Table 23. LAN

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

Table 24. Audio Line In

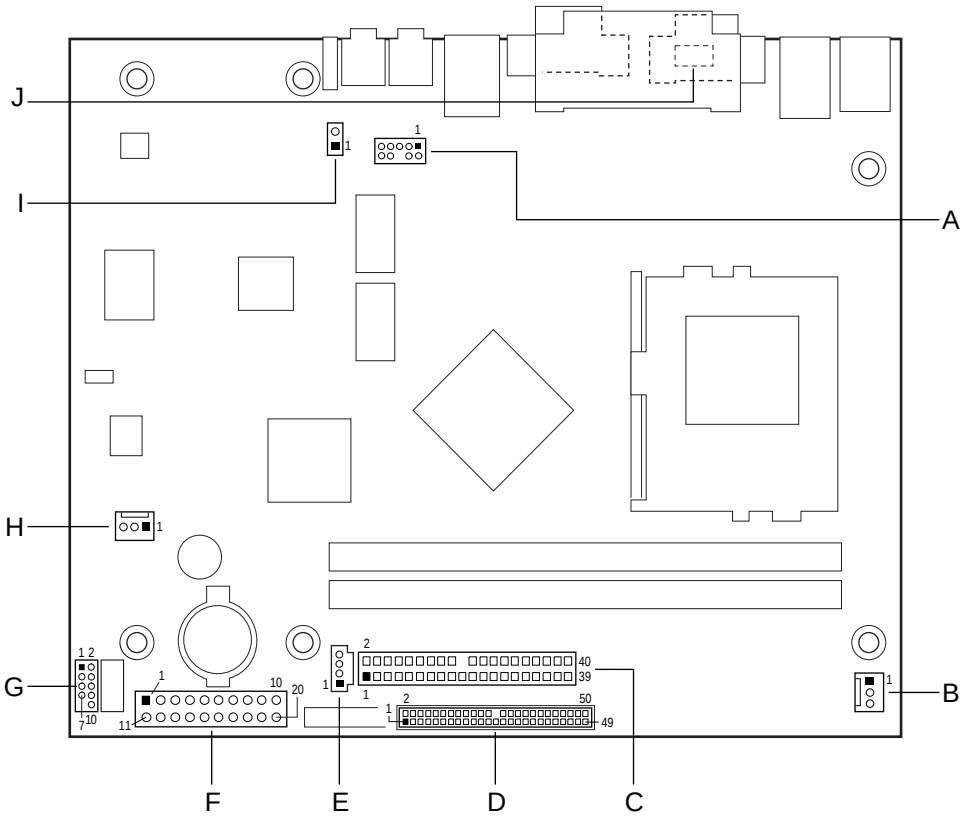
Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 25. Audio Line Out

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

2.8.2 Midboard Connectors

Figure 7 shows the location of the midboard connectors.



Item	Description	Reference Designator	For additional information see…
A	Front panel audio	J2D1	Table 26, page 51
B	Fan 2, processor	J7J1	Table 27, page 51
C	Primary IDE	J7E1	Table 28, page 51
D	Secondary IDE Slimline, (ATA-5)	J8E1	Table 29, page 52
E	ATAPI CD-ROM	J7C1	Table 30, page 52
F	Power	J8B1	Table 31, page 53
G	USB front panel (optional)	J7A1	Table 32 page 54
H	Fan 1, chassis	J6A1	Table 33, page 53
I	Speaker	J2C1	Table 34, page 53
J	Serial port (optional if back panel serial connector not installed)	J1G2	Table 35, page 54

Figure 7. Midboard Connectors

For information about…	Refer to…
The power connector	Section 1.12.2.1, page 35
The functions of the fan connectors	Section 1.12.2.2, page 35

Table 26. Front Panel Audio (J2D1)

Pin	Signal Name	Pin	Signal Name
1	Audio microphone	2	Ground
3	Audio microphone bias voltage	4	N/C
5	Ground	6	Key (no pin)
7	Audio rear left out	8	Audio front right out
9	Audio front left out	10	Audio rear right out

Table 27. Fan 2, Processor (J7J1)

Pin	Signal Name
1	Ground
2	+12 V
3	Ground

Table 28. Primary IDE (J7E1)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable select pullup)
29	DDACK0#	30	Ground
31	IRQ 14	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P#	38	Chip Select 3P#
39	Activity#	40	Ground

Table 29. Secondary IDE, Slimline, ATA-5 (J8E1)

Pin	Signal Name	Pin	Signal Name
1	AUD_LCR_R	2	AUD_RCD_R
3	AUD_CDGND_R	4	AUD_CDGND_R
5	N/C	6	N/C
7	Reset IDE	8	Ground
9	Data 7	10	Data 8
11	Data 6	12	Data 9
13	Data 5	14	Data 10
15	Data 4	16	Data 11
17	Data 3	18	Data 12
19	Data 2	20	Data 13
21	Data 1	22	Data 14
23	Data 0	24	Data 15
25	Ground	26	Key
27	DDRQ1	28	Ground
29	I/O Write#	30	Ground
31	I/O Read#	32	Ground
33	IOCHRDY	34	P_ALE (Cable select pullup)
35	DDACK1#	36	Ground
37	IRQ 15	38	Reserved
39	DAG1 (Address 1)	40	Reserved
41	DAG0 (Address 0)	42	DAG2 (Address 2)
43	Chip Select 1S#	44	Chip Select 3S#
45	Activity#	46	Ground
47	VCC	48	VCC
49	Ground	50	VCC

Table 30. ATAPI CD-ROM (J7C1)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD-ROM audio differential ground
3	CD-ROM audio differential ground
4	Right audio input from CD-ROM

Table 31. Power (J8B1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	-5 V
9	+5 VSB	19	+5 V
10	+12 V	20	+5 V

Table 32. USB Front Panel (J7A1)

Pin	Signal Name
1	USB Power
2	USB Power
3	USBP3#
4	USBP4#
5	USBP3
6	USBP4
7	Ground
8	Ground
9	Key
10	USB Front Panel Overcurrent

Table 33. Fan 1, Chassis (J6A1)

Pin	Signal Name
1	Ground
2	+12 V
3	FAN_TACH1

Table 34. Speaker (J2C1)

Pin	Signal Name
1	SPKR_P
2	SPKR_N

Table 35. Serial Port (J1G2)

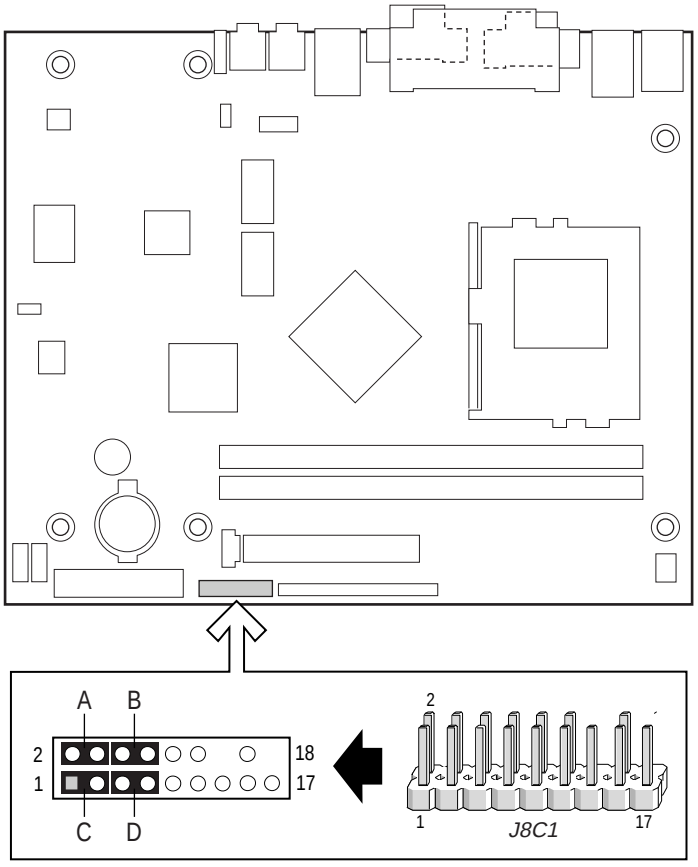
Pin	Signal Name
1	DCD (Data Carrier Detect)
2	DSR (Data Set Ready)
3	SIN# (Serial Data In)
4	RTS (Request to Send)
5	SOUT# (Serial Data Out)
6	CTS (Clear to Send)
7	DTR (Data Terminal Ready)
8	RI (Ring Indicator)
9	Ground
10	Key

NOTE

If the back panel serial connector is installed, the serial port described in Table 35 is not available.

2.8.3 Front Panel Connector

Figure 8 shows the location of the front panel connector. Table 36 lists the signal names of the front panel connector.



OM08948

Pins	Item	Description
2 and 4	A	Power / Sleep / Message waiting LED
6 and 8	B	Power switch
1 and 3	C	Hard drive activity LED
5 and 7	D	Reset switch

Figure 8. Front Panel Connector

Table 36. Front Panel Connector (J8C1)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
Hard Drive Activity LED				**Power / Sleep / Message Waiting LED**			
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Green LED
3	HDA#	Out	Hard disk activity LED	4	HDR_BLNK_YEL	Out	Yellow LED
Reset Switch				**On / Off Switch**			
5	GND		Ground	6	SW_ON#	In	On / Off switch
7	FP_RESET#	In	Reset switch	8	GND		Ground
Miscellaneous				**Miscellaneous**			
9	VCC	Out	+5 V DC	10	ICH_SERVICE	In	Reserved
11	N/A		Reserved	12	GND		Ground
13	GND		Ground	14	Pin removed		Key
15	N/A		Reserved	16	N/A		Reserved
17	VCC		+5 V DC	18	Pin removed		Key

2.8.3.1 Power / Sleep / Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 37 shows the possible states for a single-colored LED.

Table 38 shows the possible states for a dual-colored LED.

Table 37. States for a Single-Colored Power LED

LED State	Description	ACPI State
Off	Power off (not running)	S1, S3, S5
Steady Green	Running	S0
Blinking Green	Running/message waiting	S0

Table 38. States for a Dual-Colored Power LED

LED State	Description	ACPI State
Off	Power off	S5
Steady Green	Running	S0
Blinking Green	Running/message waiting	S0
Steady Yellow	Sleeping	S1, S3
Blinking Yellow	Sleeping/message waiting	S1, S3

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.2 Power Switch Connector

Pins 6 and 8 can be connected to a front panel power switch. The switch must pull pin 6 to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.3.3 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface.

2.8.3.4 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the YA810E board resets and runs the POST.

2.9 Jumper Block

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, damage to the YA810E board could occur.

Figure 9 shows the location of the BIOS Setup jumper block. This 3-pin jumper block determines the BIOS Setup program's mode. Table 39 describes the jumper settings for the three modes: normal, configure, and recovery.

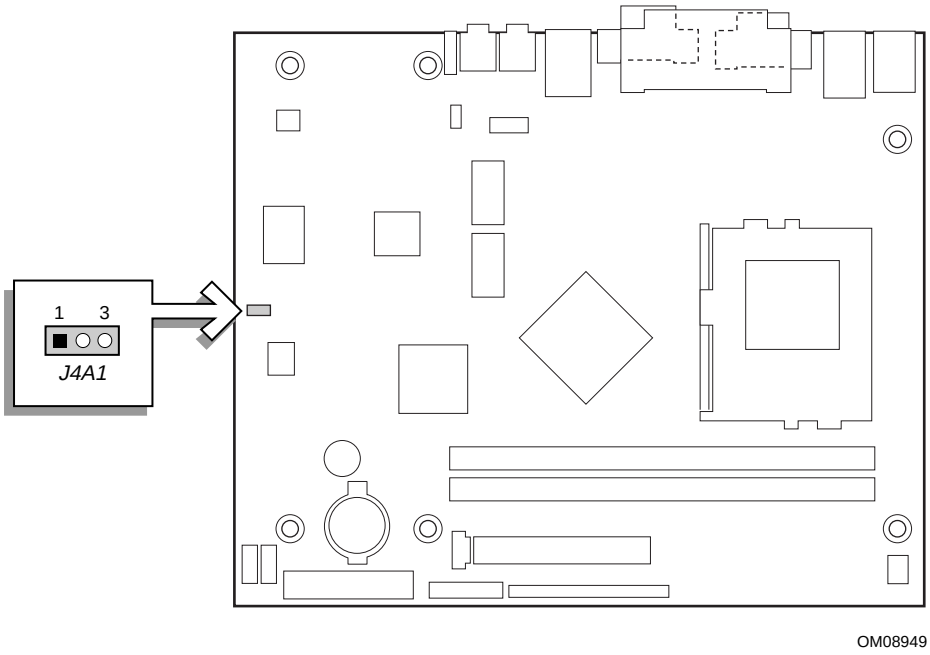
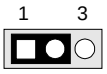
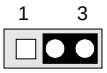
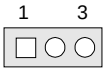


Figure 9. Location of the BIOS Setup Jumper Block

Table 39. BIOS Setup Configuration Jumper Settings (J4A1)

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette (1.44 MB) or CD–ROM is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 77
The maintenance menu of the BIOS Setup program	Section 4.2, page 78
BIOS recovery	Section 3.6, page 73

2.10 Mechanical Considerations

2.10.1 FlexATX Form Factor

The YA810E board is designed to fit into an ATX- or microATX-form-factor chassis. Figure 10 illustrates the mechanical form factor for the board. Dimensions are given in inches (millimeters). The outer dimensions are 9.0 inches by 7.5 inches (228.60 millimeters by 190.50 millimeters). Location of the I/O connectors and mounting holes are in compliance with the FlexATX addendum to the microATX specification (see Section 1.3).

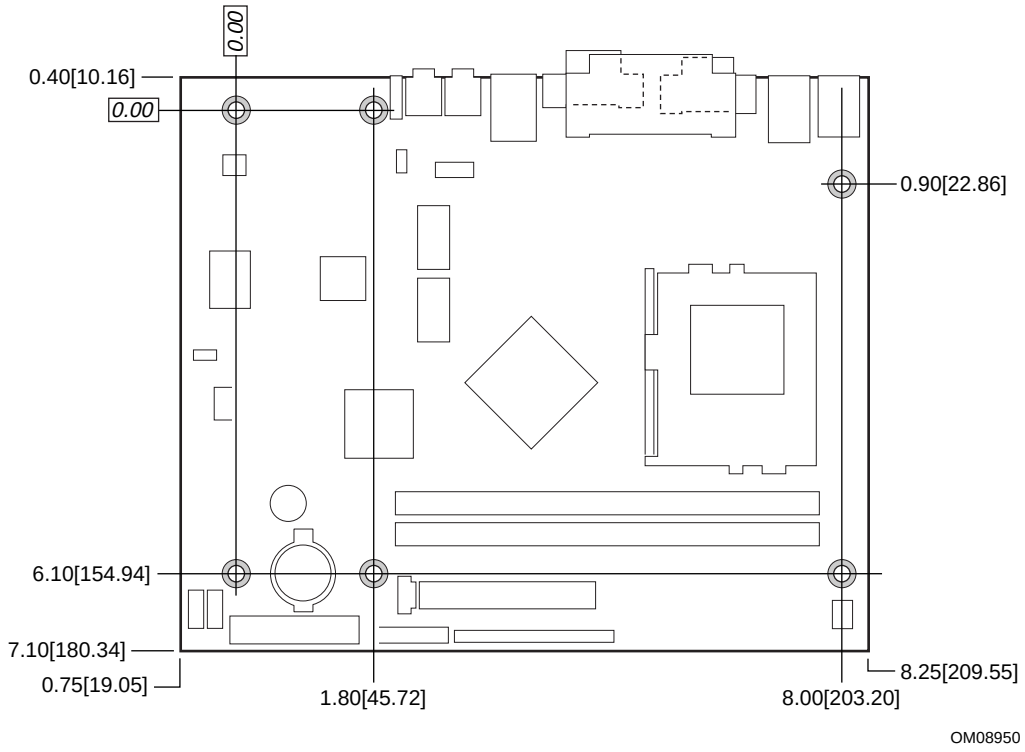


Figure 10. Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the YA810E board must meet specific dimensional requirements. Systems based on this board need the back panel I/O shield to pass certification testing. Figure 11 shows the critical dimensions of the I/O shield. Dimensions are given in inches and millimeters. For dimensions given to two decimal places, (X.XX) the tolerance is ±0.02 inches (±5.09 millimeters). Both figures indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.3 for information about the ATX specification.

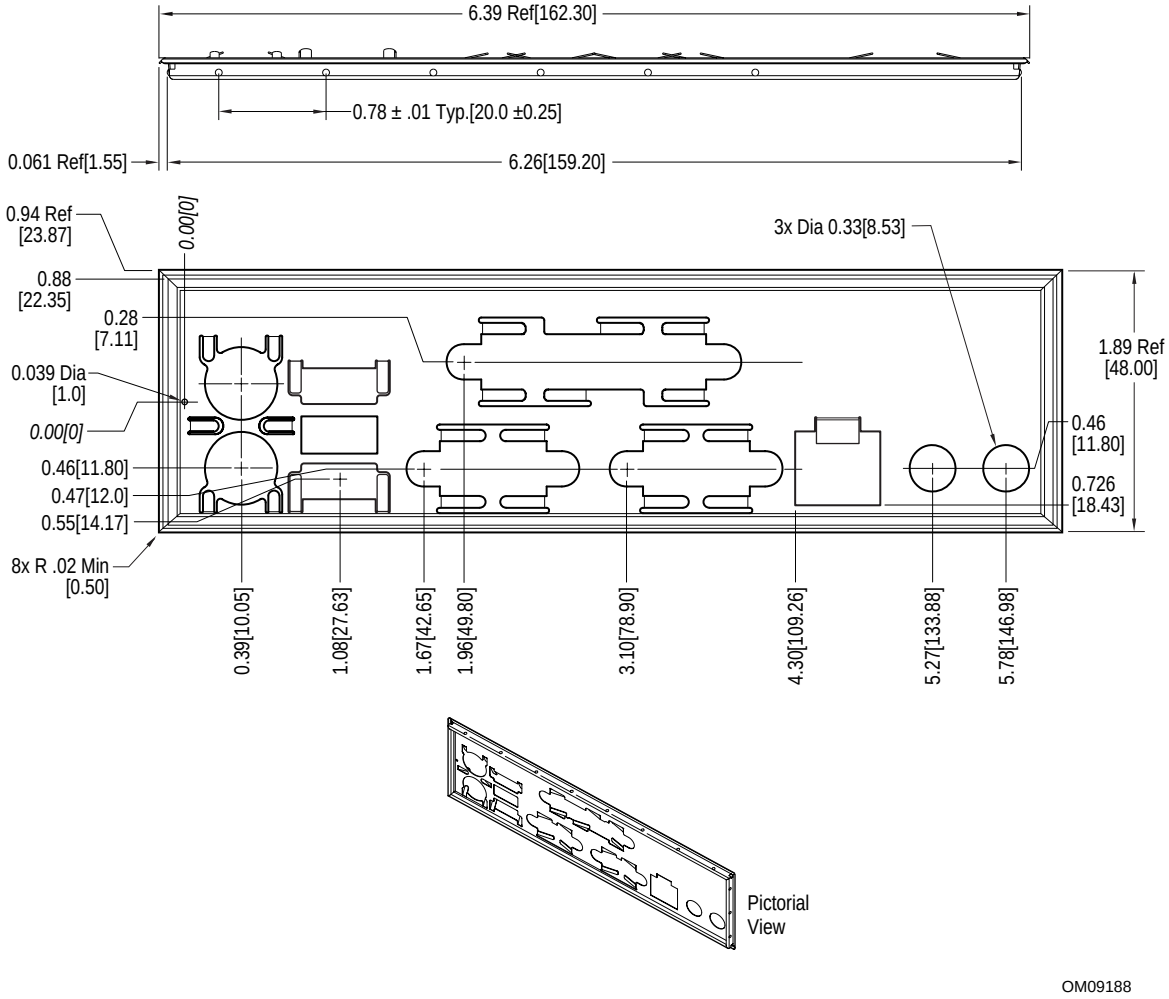


Figure 11. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 40 lists voltage and current specifications for a computer that contains the YA810E board and the following:

- 500 MHz Intel Celeron processor with a 128 KB cache
- 128 MB SDRAM
- 3.2 GB IDE hard disk drive
- 24X Slimline IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows† 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with a typical 145 W power supply, nominal input voltage and frequency, with true RMS wattmeter at the line input.

Table 40. Power Usage

		DC Amps at:				
Mode	**AC Watts**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Windows 98 ACPI S0	27.4 W	1.247 A	0.988 A	0.593 A	0.018 A	0.182 A
Windows 98 ACPI S1	23.1 W	1.235 A	0.556 A	0.446 A	0.018 A	0.153 A
Windows 98 ACPI S3	3.83 W	0.0 A	0.0 A	0.0 A	0.0 A	0.402 A
Windows 98 ACPI S5	2.31 W	0.0 A	0.0 A	0.0 A	0.0 A	0.166 A

2.11.2 Power Supply Considerations

System integrators should refer to the power usage values listed in when selecting a power supply for use with this motherboard. The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification (see Section 1.3).

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

2.11.3 Standby Current Requirements

The +5 V standby current consumed by the YA810E desktop board is 0.182 A. This does not include external peripherals.

⟹ NOTE

These standby current requirements are system configuration dependent.

2.11.4 Fan Power Requirements

Table 41 lists the maximum DC voltage and current requirements for the fans when the board is in sleep mode or normal operating mode. Power consumption is independent of the operating system used and other variables.

Table 41. Fan DC Power Requirements

Fan Type	Mode	Voltage	Maximum Current (Amps)
Chassis (J6A1)	Sleep	+ 6.9 VDC	0.250 mA (current limited)
	Normal	+ 12 VDC	0.210 mA (current limited)
Processor (J7J1)	Sleep	+ 12 VDC	0.137 mA (current limited)
	Normal	+ 12 VDC	0.137 mA (current limited)

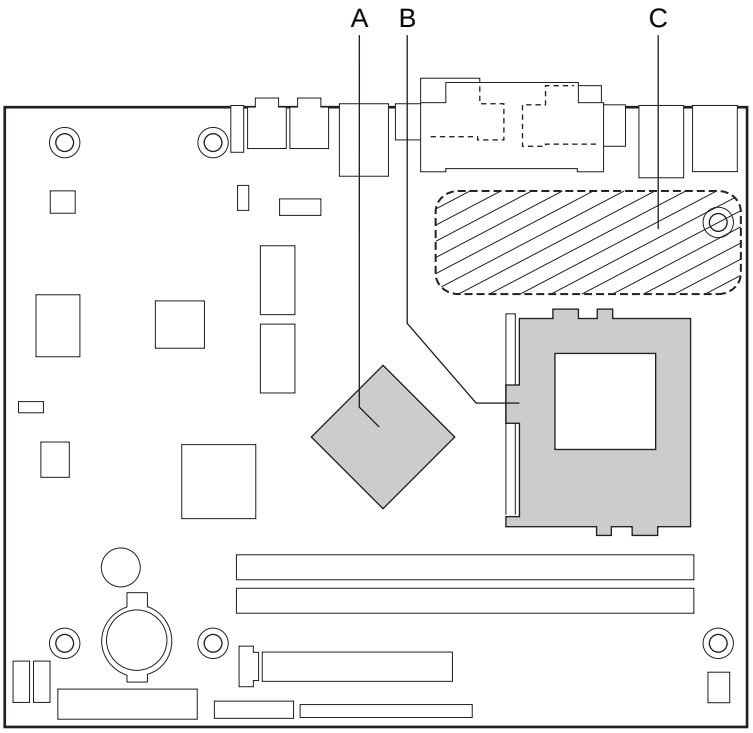
For information about	Refer to
The location of the fan connectors	Figure 7, page 50
The signal names of the chassis fan connector	Table 33, page 53
The signal names of the processor fan connector	Table 27, page 51

2.12 Thermal Considerations

CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 ºC to 10 ºC could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

Figure 12 shows the localized high-temperature zones.



A Intel 82810E GMCH
B Processor
C Processor voltage regulator area

Figure 12. High Temperature Zones

Table 42 provides maximum component case temperatures for YA810E board components that could be sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the YA810E board.

Table 42. Thermal Considerations for Components

Processor Type	Processor Designation / Host Bus Speed	Maximum Processor Temperature
Pentium III processors	500E / 100 MHz	82 °C (max thermal junction)
	550E / 100 MHz	82 °C (max thermal junction)
	600E / 100 MHz	82 °C (max thermal junction)
	533B / 133 MHz	90 °C (max thermal junction)
	600B / 133 MHz	85 °C (max thermal junction)
	533EB / 133 MHz	82 °C (max thermal junction)
	600EB / 133 MHz	82 °C (max thermal junction)
	667 / 133 MHz	82 °C (max thermal junction)
	733 / 133 MHz	80 °C (max thermal junction)
Celeron processors	300A, 333, 366, 400, 433, 466, 500, and 533 MHz (all at 66 MHz)	75 °C (max thermal junction)
Component Type	**Maximum Component Temperature**	
Intel 82810E GMCH	70 °C	

⚠ CAUTION

The voltage regulator area can reach a temperature of up to 85 ºC in an open chassis. Ensure that there is proper airflow to this area of the board. Failure to do so may result in damage to the voltage regulator circuit. System integrators should ensure that proper airflow is maintained in the voltage regulator circuit (item C in Figure 12). Components in this area could be damaged without adequate airflow.

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

YA810E board MTBF: 146,100.36 hours

2.14 Environmental

Table 43 lists the environmental specifications for the YA810E board.

Table 43. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the YA810E board's compliance with safety and EMC regulations.

2.15.1 Safety Regulations

Table 44 lists the safety regulations the YA810E board complies with when it is correctly installed in a compatible host system.

Table 44. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 45 lists the EMC regulations the board complies with when it is correctly installed in a compatible host system.

Table 45. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada)
AS/NZ 3548	Australian Communications Authority (ACA), Standard for Electromagnetic Compatibility.

2.15.3 Certification Markings

This printed circuit assembly has the following product certification markings:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (Solder side)
- UL File Number for desktop boards: E139761 (Component side)
- PB Part Number: Intel bare circuit board part number (Solder side) 752335-001
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder
- FCC Logo/Declaration: (Solder side)
- ACA (C-Tick) mark: Consists of a unique letter C, with a tick mark; followed by N-232. Located on the component side of the YA810E board and on the shipping container
- CE Mark: (Component side) The CE mark should also be on the shipping container

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The YA810E board uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

This YA810E board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as YA81011A.86A.

For information about	Refer to
The board's compliance level with Plug and Play	Table 3, page 16

3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable. Figure 13 shows the organization of the flash memory.

The last two 8 KB blocks of the fault tolerance area are the parameter blocks. These blocks contain data such as BIOS updates, vital product data (VPD), logo, System Management BIOS (SMBIOS) interface, and extended system configuration data (ESCD) information. The backup block contains a copy of the fault tolerance block.

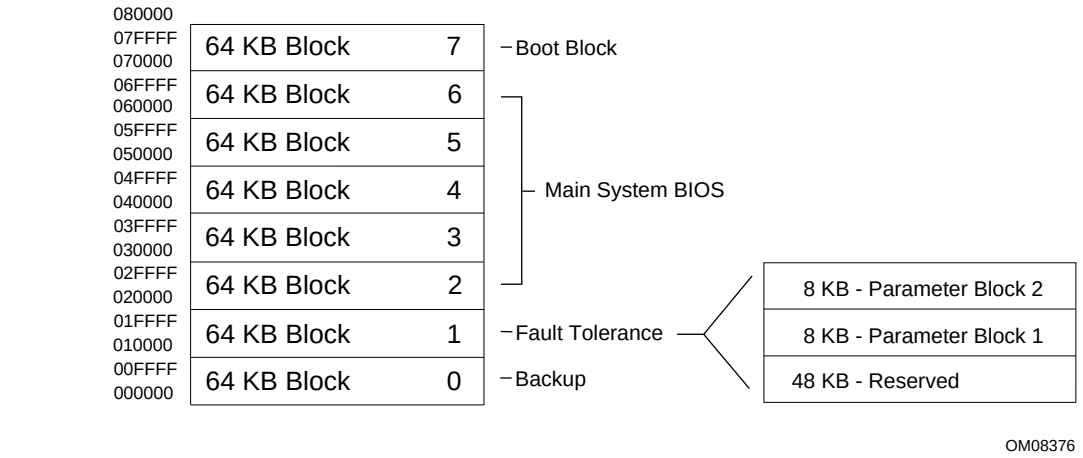


Figure 13. Memory Map of the Flash Memory Device

3.3 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA/66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, ARMD (ATA Removable Media Devices), and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66 features the following items are required:

- An ATA-66 peripheral device
- An ATA-66 compatible cable
- ATA-66 operating system device drivers

NOTE

ATA-66 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an Ultra ATA/66 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate for either drive is 33 MB/sec.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT† 4.0, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The board's compliance level with SMBIOS	Table 3, page 16

3.5 BIOS Upgrades

A new version of the BIOS can be upgraded from a 1.44 MB diskette (for updating from an LS-120 diskette drive) or a CD-ROM using the Intel® Flash Memory update utility that is available from Intel. The BIOS can also be updated from the operating system using the operating system's update utility that is available from Intel. These utilities support the following BIOS maintenance functions:

- Update the flash BIOS
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS
- BIOS boot block update

BIOS upgrades and these utilities are available from Intel through the Intel World Wide Web site.

NOTE

Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.5.1 Language Support

The BIOS Setup program and help messages can be supported in 32 languages. Five languages are available in the BIOS: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

3.5.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site. See Section 1.2 for more information about this site.

3.6 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from either a 1.44 MB diskette (for recovery from an LS-120 diskette drive configured as an ATAPI removable IDE device), or from a CD-ROM using the BIOS recovery mode. When recovering the BIOS be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support. You can monitor this procedure by listening to the speaker or looking at the recovery drive LED.
- Two beeps and the end of activity in the recovery drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery. In case of a BIOS recovery failure, verify that SPD memory is installed and retry the BIOS recovery procedure. If non-SPD memory is installed, replace with SPD memory and try the procedure again.

NOTE

BIOS recovery cannot be accomplished if non-SPD DIMMs are installed. The SPD data structure is required for the recovery process.

To create a BIOS recovery diskette or CD-ROM, a bootable LS-120 diskette or CD-ROM must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

If the computer is configured to boot from an LS-120 diskette (in the Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode	Section 2.9, page 58
The Boot menu in the BIOS Setup program	Section 4.7, page 89
Contacting Intel customer support	Section 1.2, page 16

3.7 Boot Options

In the BIOS Setup program, the user can choose to boot from an ATAPI removable media device, hard drives, CD-ROM, or the Intel UNDI (Universal Network Driver Interface) PXE-2.0 environment. The default settings for the boot devices are:

- IDE HDD
- ATAPI CD-ROM
- Intel UNDI PXE-2.0
- Disabled

3.7.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device.

The network (Intel UNDI, PXE-2.0 environment) can be selected as a boot device. This selection allows booting from an Intel UNDI, PXE-2.0 through the LAN connector with a remote boot ROM installed.

For information about…	Refer to
The El Torito specification	Table 3, page 16

3.7.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the keyboard and mouse are not present.

3.8 USB Legacy Support

NOTE

USB legacy support is for keyboards, mice, and hubs only. Other USB devices are not supported.

USB legacy support enables USB devices such as keyboards, mice, and hubs to be used even when no operating system USB drivers are in place. By default, USB legacy support is set to Enabled in the BIOS. USB legacy support is used in accessing the BIOS Setup program and installing an operating system that supports USB.

NOTE

Do not use USB devices with an operating system that does not support USB. USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.

This sequence describes how USB legacy support operates in the Enabled mode.

1. When you first power-up the computer, USB legacy support is disabled.
2. POST begins.
3. USB legacy support is then enabled by the BIOS. This allows you to use a USB keyboard to enter the BIOS Setup program or the maintenance mode.
4. When POST completes, it leaves USB legacy support enabled.
5. The operating system then loads. While the operating system is loading, USB keyboards and mice are recognized.
6. After the operating system loads the USB drivers, other types of USB devices are then recognized by the operating system.

3.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 46 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 46. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options *	Can change all options *	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

* If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 87

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 47 lists the BIOS Setup program menu functions.

Table 47. BIOS Setup Program Menu Functions

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and allows memory settings	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 58 tells how to put the board in configuration mode.

Table 48 lists the function keys available for menu screens.

Table 48. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen
<↑> or <↓>	Selects an item
<Tab>	Selects a field
<Enter>	Executes command or selects a submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The menu shown in Table 49 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9 on page 58 for configuration mode setting information.

Table 49. Maintenance Menu

Feature	Options	Description
▸ Clear All Passwords	Confirm: Yes/No	Selecting *Yes* clears the user and supervisor passwords.
▸ Clear BIS Credentials	Confirm: Yes/No	Selecting *Yes* clears the WfM BIS (Boot Integrity Service) credentials.
▸ Extended Configuration	(See Extended Configuration Submenu)	Selecting *User-Defined* allows setting system control and video memory cache modes.
CPU Information:		
CPU Microcode Update Revision	No options	Displays CPU's Microcode Update Revision.
CPU Stepping Signature	No options	Displays CPU's Stepping Signature.

4.2.1 Extended Configuration Submenu

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu represented by Table 50 is for setting system control and video memory cache mode. This submenu becomes available when User-Defined is selected under Extended Configuration.

Table 50. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	**Default (default)** User-Defined	Selecting user-defined allows you to select *Default* or *User-Defined*. Selecting *User-Defined* allows you to configure the items listed under Memory Control below. Note: If *User-Defined* is selected, the status will be displayed in the Advanced Menu as: “Extended Menu: Used.”
Memory Control:		
SDRAM Auto Configuration	• **Auto (default)** • User-Defined	Sets extended memory configuration options to auto or user-defined.
CAS# Latency	• **3 (default)** • 2 • Auto	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# delay	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge	• 3 • 2 • **Auto (default)**	Selects the length of time required before accessing a new row.

4.3 Main Menu

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 51 describes the Main Menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 51. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS
Processor Type	No options	Displays processor type
Processor Speed	No options	Displays processor speed
System Bus Frequency	No options	Displays the host bus speed
Cache RAM	No options	Displays the size of second-level cache
Total Memory	No options	Displays the total installed SDRAM memory
Memory Bank 0 Memory Bank 1	No options No options	Displays *SDRAM* or *Not Installed* indicating the presence or absence of memory in Memory Banks 0 and 1
Processor Serial Number	• Enable • **Disable (default)**	If enabled, displays the processor's serial number. This feature is supported by these processors only: 533EB, 600EB, 667, and 733
System Time	Hour, minute, and second	Specifies the current time
System Date	Month, day, and year	Specifies the current date

4.4 Advanced Menu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

Table 52 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

CAUTION

Setting items on this screen to incorrect values may cause your system to malfunction.

Table 52. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	Will read *Used* or *Not Used* depending upon whether *User-Defined* is set in the Extended Configuration sub-menu.
▸ Boot Configuration	No options	Configures Plug and Play, the Numlock key, and resets configuration data. When selected, displays the Boot Settings Configuration submenu.
▸ Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
▸ IDE Configuration	No options	Specifies type of connected IDE device.
▸ Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.

4.4.1 Boot Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The submenu represented by Table 53 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 53. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices. Not required with a Plug and Play operating system.
Reset Config Data	• **No (default)** • Yes	Clears the BIOS configuration data on the next boot.
Numlock	• Off • **On (default)**	Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.2 Peripheral Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The submenu represented in Table 54 is used for enabling the onboard audio, serial and parallel ports, LAN devices, and legacy USB support.

Table 54. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A (if available)	• Disable • Enable • **Auto (default)**	Enables or disables Serial Port A.
Parallel Port (if available)	• Disable • Enable • **Auto (default)**	Enables or disables the Parallel Port.
Mode	• Output only • **Bi-directional (default)** • EPP • ECP	Allows configuring the Parallel Port's operating mode.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN Device	• Disabled • **Enabled (default)**	Enables or disable the onboard LAN controller. Shows only if LAN is installed.
Legacy USB Support	• Disabled • **Enabled (default)** • Auto	Enables or disables USB legacy support. (See Section 3.8 on page 75 for more information.)

4.4.3 IDE Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The menu represented in Table 55 is used to configure IDE device options.

Table 55. IDE Configuration

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay. Selecting a predelay instructs the BIOS to wait a specified time before attempting to detect the hard-disk drive. This allows the BIOS to detect slow spin-up hard disk drives.
▸ Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
▸ Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
▸ Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
▸ Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4 IDE Configuration Sub-Submenus

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Event Log Configuration

The sub-submenus represented in Table 56 are used to configure IDE devices.

Table 56. IDE Configuration Sub-Submenus

Feature	Options	Description
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows the cylinders, heads, and sectors fields to be changed. *Auto* automatically fills in the values for the cylinders, heads, and sectors fields.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables the LBA mode control. (Shows when anything other than *Auto* is selected in the *Type* menu above.)
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting. Shows when anything other than *Auto* is selected in the *Type* menu above.
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Configures the PIO mode. Shows when anything other than *Auto* is selected in the *Type* menu above.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4 (Available in primary IDE only)	Specifies the Ultra DMA mode for the drive. Shows when anything other than *Auto* is selected in the *Type* menu above.

4.4.5 Event Log Configuration Submenu

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

Boot Configuration
Peripheral Configuration
IDE Configuration
Event Log Configuration

The submenu represented by Table 57 is used to configure the event logging features.

Table 57. Event Log Configuration Submenu

Feature	Options	Description
Event log	No options	Indicates if there is space available in the event log.
Event log validity	No options	Indicates if the contents of the event log are valid.
▸ View event log	No options	Pressing *Enter* displays the event log.
Clear all event logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
▸ Mark events as read	No options	Pressing *Enter* marks all events as read.

4.5 Security Menu

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 58 is for setting passwords and security features.

Table 58. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
User Password Is	No options	Reports if there is a user password set.
Supervisor Password Is	No options	Reports if there is a supervisor password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
If password entered previously:		
Feature	**Options**	**Description**
Clear User Password (Supervisor only)	• Yes • No	Allows removal of a previously entered password.
User Access Level (Supervisor only)	• Limited • No access • View Only • **Full (default)**	Specifies user's access privileges.
Unattended Start	• Enabled • **Disabled (default)**	Enables or disables wake on LAN technology feature. Locks keyboard.

4.6 Power Menu

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 59 is for setting the power management features.

Table 59. Power Menu

Feature	Options	Description
Power Management	• **Enable (default)** • Disable	Enable or disable the BIOS power management feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• **Enabled (default)** • Disabled	Enables the hard drive to be managed during standby and suspend.
Video Power Down	• Disable • Standby • **Suspend (default)** • Sleep	Disabled, disables the video power management feature. Other values enable video power management and specifies the mode in which to place the monitor when entering a low power state.
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI suspend state.
Video Repost	• **Disabled (default)** • Enabled	Allows user to select if system BIOS is to repost video when board wakes from an S3 sleep state. Visible only if S3 is selected in the ACPI Suspend State menu above.

4.7 Boot Menu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The menu represented in Table 60 is used to set the boot features and the boot sequence.

Table 60. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM logo instead of POST messages.
Quick Boot	• **Disabled (default)** • Enabled	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stays Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC/Power loss occurs. *Power On* restores power to the computer. *Stay Off* keeps the power off until the power switch is pressed. *Last State* restores the previous power state before power loss occurred.
On Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to a modem wakeup event when the power is off.
On LAN	• Stay Off • **Power On (default)**	Specifies how the computer responds to a LAN wakeup event when the power is off.
On PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PME wakeup event when the power is off.
First Boot Device Second Boot Device Third Boot Device Fourth Boot Device Fifth Boot Device (Note: The selections under Options are available for *all* boot devices, first through fourth. The default settings are listed under Description.)	• ARMD-FDD (1) • ARMD-HDD (2) • IDE-HDD (3) • **ATAPI CD-ROM (default)** • Intel UNDI, PXE-2.0 • Disabled	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. The defaults for the first through fourth boot devices are: • IDE-HDD • ATAPI CD-ROM • Intel UNDI, PXE-2.0 • Disabled
▸ IDE Drive Configuration	No Option	Configures IDE drives. When selected, displays the IDE configuration submenu.

(1) ARMD-HDD = ATAPI Removable Media Device - hard disk drive

(2) ARMD-FDD = ATAPI Removable Media Device - floppy disk drive

(3) HDD = Hard Disk Drive

4.7.1 IDE Drive Configuration Submenu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The submenu represented in Table 61 is used to set the order in which the IDE drives boot. Changing the boot-order of a given drive causes the boot-order for the other drives to change automatically to accommodate your selection.

Table 61. IDE Drive Configuration Submenu

Feature	Options	Description
Primary Master IDE	**1st IDE (default)** 2nd IDE 3rd IDE 4th IDE	Allows you to select the order in which the Primary Master IDE drive boots.
Primary Slave IDE	1st IDE **2nd IDE (default)** 3rd IDE 4th IDE	Allows you to select the order in which the Primary Slave IDE drive boots.
Secondary Master IDE	1st IDE 2nd IDE **3rd IDE (default)** 4th IDE	Allows you to select the order in which the Secondary Master IDE drive boots.
Secondary Slave IDE	1st IDE 2nd IDE 3rd IDE **4th IDE (default)**	Allows you to select the order in which the Secondary Slave IDE drive boots.

4.8 Exit Menu

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 62 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 62. Exit Menu

Feature	Description
▸ Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
▸ Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
▸ Load Setup Defaults	Loads the factory default values for all the Setup options.
▸ Load Custom Defaults	Loads the custom defaults for Setup options.
▸ Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
▸ Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 63 lists the error messages and provides a brief description of each.

Table 63. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate-A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive is not an ATAPI device. Run Setup to make sure device is selected correctly.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 63. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Is Locked	The system keyboard lock is engaged. The system must be unlocked to continue to boot.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added, there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an offboard card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 64 defines the Uncompressed INIT Code Checkpoints, Table 65 describes the Boot Block Recovery Code Check Points, and Table 66 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 64. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If the BIOS is in recovery mode or the main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 65. Boot Block Recovery Code Check Points

Code	Description of POST Operation
E0	Onboard floppy controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller, interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize ATAPI CD-ROM drive.
EA	Try to boot from ATAPI CD-ROM. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip†) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from ATAPI CD-ROM failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 66. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23, 24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate display memory R/W test.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 66. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640 K memory.
48	Patterns written in base memory. Going to find out amount of memory below 1 M memory.
49	Amount of memory below 1 M found and verified. Going to find out amount of memory above 1 M memory.
4B	Amount of memory above 1 M found and verified. Check for soft reset and going to clear memory below 1 M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1 M cleared. (SOFT RESET) Going to clear memory above 1 M.
4D	Memory above 1 M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64 K memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1 M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1 M to follow.
52	Memory testing/initialization above 1 M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 66. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done.
91	Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area.
9A	Return after setting timer. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID, and Num Lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 66. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 67 describes the bus initialization checkpoints.

Table 67. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 68 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 68. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned
1	func#1, static devices init on the bus concerned
2	func#2, output device init on the bus concerned
3	func#3, input device init on the bus concerned
4	func#4, IPL device init on the bus concerned
5	func#5, general device init on the bus concerned
6	func#6, error reporting for the bus concerned
7	func#7, add-on ROM init for all buses

Table 69 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 69. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	Onboard system devices
2	ISA devices (not supported)
3	EISA devices (not supported)
4	ISA PnP devices (not supported)
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the YA810E board. The speaker provides audible error code (beep code) information during the power-on self-test (POST).

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during power-on self-test (POST), the BIOS displays an error message describing the problem (see Table 70). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 70. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g., POST module not found, etc.)

5.6 Enhanced Diagnostics

The enhanced diagnostics feature consists of a hardware decoder and four LEDs located on the back panel. This feature requires no cabling or modifications to the chassis other than to the back panel I/O shield.

Figure 14 shows the location of the diagnostic LEDs. Table 71 lists the diagnostic codes displayed by the LEDs.

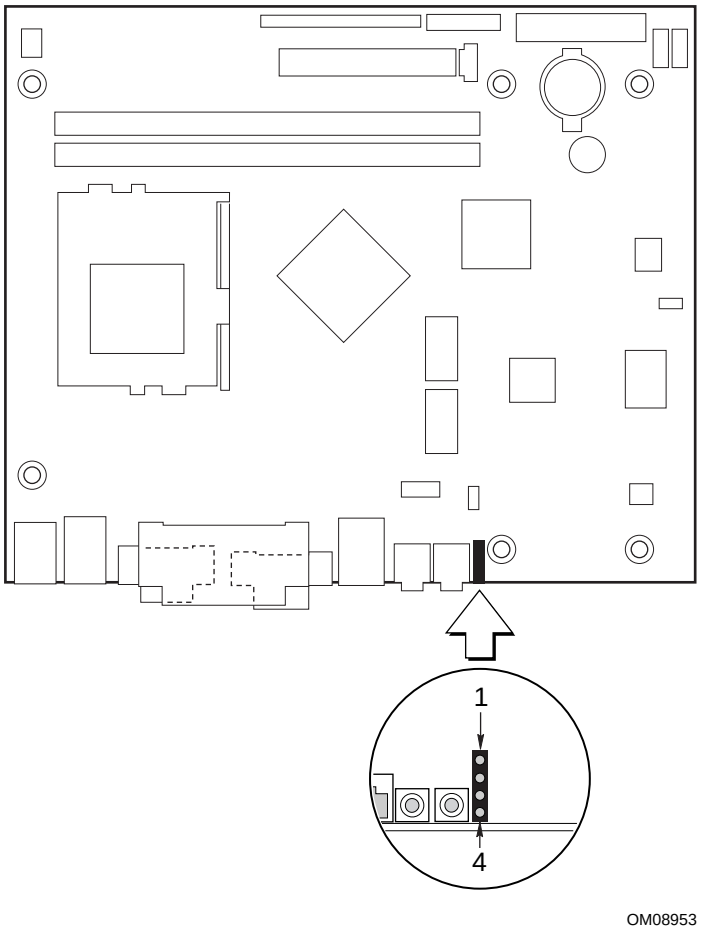
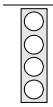
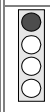
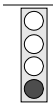
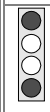
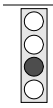
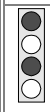
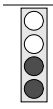
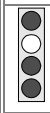
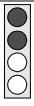
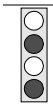
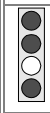
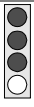
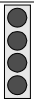


Figure 14. Enhanced Diagnostic LEDs

Table 71. Diagnostic LED Codes

Display	BIOS Operation	Display	BIOS Operation
 Amber Amber Amber Amber	Power-on, starting BIOS	 Green Amber Amber Amber	Undefined
 Amber Amber Amber Green	Recovery mode	 Green Amber Amber Green	Undefined
 Amber Amber Green Amber	Processor, cache, etc.	 Green Amber Green Amber	Undefined
 Amber Amber Green Green	Memory, auto-size, shadow, etc.	 Green Amber Green Green	Undefined
 Amber Green Amber Amber	PCI bus initialization	 Green Green Amber Amber	Undefined
 Amber Green Amber Green	Video	 Green Green Amber Green	Undefined
 Amber Green Green Amber	IDE bus initialization	 Green Green Green Amber	Reserved
 Amber Green Green Green	USB initialization	 Green Green Green Green	Booting operating system

Note: Undefined states are reserved for future use.