Advanced/ZE Memory Map, I/O Map, IRQs and DMA

I/O MAP

Address (hex)	*Size*	*Description*
0000 - 000F	16bytes	PIIX - DMA 1
0020 - 0021	2 bytes	PIIX - Interrupt Controller 1
0040 - 0043	4 bytes	PIIX - Timer 1
0048 - 004B	4 bytes	PIIX - Timer 2
0060	1 byte	Keyboard Controller Data Byte
0061	1 byte	PIIX - NMI, speaker control
0064	1 byte	Kbd Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX - Enable NMI
0070, bits 6:0	7 bits	82C306 - Real Time Clock, Address
0071	1 byte	82C306 - Real Time Clock, Data
0078	1 byte	Reserved - Brd. Config.
0079	1 byte	Reserved - Brd. Config.rd only
0080 - 008F	16bytes	PIIX - DMA Page Register
00A0 - 00A1	2 bytes	PIIX - Interrupt Controller 2
00C0 - 00DE	31bytes	PIIX - DMA 2
00F0	1 bytes	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0278 - 027B	4 bytes	Parallel Port 2
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0376	1 byte	Secondary IDE Chan Cmd
0377	1 byte	Secondary IDE Chan Stat
0378 - 037F	8 bytes	Parallel Port 1
03BC - 03BF	4 bytes	Parallel Port x
03E8 - 03EF	8 bytes	Serial Port 3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 bytes	Primary IDE Channel Cmnd
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change
03F7, bits 6:0	7 bits	Primary IDE Channel Status
03F8 - 03FF	8 bytes	On-Board Serial Port 1
LPT + 400h	8 bytes	ECP port, LPT + 400h
0CF8-0CFB*	4 bytes	PCI Config Addr Reg Enable
0CFC-0CFF*	4 bytes	PCI Conifig Data Reg
FF00-FF07	8 bytes	IDE Bus Master Reg

* Only accessible after PCI configuration space enabled.

Table C-1. Advanced/ZE I/O Address Map

I/O Port 78 is reserved for BIOS use. I/O Port 79 is a read only port, the bit definitions are shown below.

Bit #	*Description*	*Bit = 1*	*Bit = 0*
0	Internal CPU Clock Freq. (Switch 6)	3/2x	2x
1	No Connect		
2	No Connect		
3	External CPU clock (Switch 7)		
4	External CPU clock (Switch 8)		
5	Setup Disable (Switch 5)	Enable access	Disable access
6	Clear CMOS (Switch 4)	Keep values	Clear values
7	Password Clear (Switch 3)	Keep password	Clear

Table C-2. I/O Port for board configuration

PCI CONFIGURATION SPACE MAP

The 82430FX chipset uses Configuration Mechanism 1 to access PCI configuration space. The PCI Configuration Address register is a 32-bit register located at CF8h, the PCI Configuration Data register is a 32-bit register located at CFCh. These registers are only accessable by full DWORD accesses. The table below lists the PCI bus and device numbers used by the baseboard.

Bus Number (hex)	*Dev Number (hex)*	*Func. Number (hex)*	*Description*
00	00	00	Intel 82437FX (TSC)
00	07	00	Intel 82371FB (PIIX) PCI/ISA bridge
00	07	01	Intel 82371FB (PIIX) IDE Bus Master
00	0F		PCI Expansion Slot 1
00	0D		PCI Expansion Slot 2
00	0E		PCI Expansion Slot 3
00	10		PCI Expansion Slot 4

Table C-3. Advanced/ZE PCI Config. Space Map

MEMORY MAP

Address Range (Decimal)	*Address Range (hex)*	*Size*	*Description*
1024K-131072K	100000-8000000	130048K	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI System BIOS
952K-959K	EE000-EFFFF	8K	FLASH Boot Block (Available as UMB)
948K-951K	ED000-EDFFF	4K	ESCD (Plug'n'Play configuration area)
944K-947K	EC000-ECFFF	4K	OEM LOGO (available as UMB)
896K-943K	E0000-EBFFF	48K	BIOS RESERVED (currently available as UMB)
800K-895K	C8000-DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K-799K	A0000-C7FFF	160K	Available HI DOS Memory (normally reserved for video)
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K-638K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

Table D-1. Advanced/ZE Memory Map

The table above details the Advanced/ZE memory map. The ESCD area from ED000-EDFFF is not available for use as an Upper Memory Block (UMB) by memory managers. The area from E0000-EBFFF is currently not used by the BIOS and is available for use as UMB by memory managers. Parts of this area may be used by future versions of the BIOS to add increased functionality.

INTERRUPTS & DMA CHANNELS

IRQ	*System Resource*
NMI	Unused
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	Parallel Port 2
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available
10	User available
11	User available
12	On-board Mouse Port
13	Reserved, Math coprocessor
14	Primary IDE if enabled, else available to user
15	Secondary IDE if enabled, else available to user

Table E-1. Advanced/ZE Interrupts

DMA	*Data Width*	*System Resource*
0	8- or 16-bits	Open
1	8- or 16-bits	Open - Normally used for LAN
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

Table E-2. Advanced/ZE DMA Map