

# Intel® Desktop Board D850GB Specification Update

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The Intel® Desktop Board D850GB may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel® D850GB may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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### **REVISION HISTORY**

Date of Revision	Version	Description
December 2000	-001	This document is the first Specification Update for the Intel® Desktop Board D850GB. Added Errata 1, 2 and Document Changes 1-3.
January 2001	-002	Updated General Information, Note 3. Added Specification Change 1 and Document Change 4.
February 2001	-003	Removed BIOS/Errata cross reference table, Added Specification Clarifications 1-3, and Documentation Changes 5, 6.
March 2001	-004	Updated Erratum 1.
April 2001	-005	Updated General Information Section.
May 2001	-006	Removed Specification Change 1, Specification Clarifications 1, 2, and Document Changes 1-6, which were published in revision -002 of the Technical Product Specification. Added Errata 3, 4.
June 2000	-007	Added Specification Change 2 and Erratum 5.
July 2001	-008	Amended Erratum 5. Added Erratum 6.
August 2001	-009	Added Specification Change 3 and Specification Clarifications 4,5.
November 2001	-010	Added Specification Change 4 and Specification Clarification 6.
December 2001	-011	Added Erratum 7. Corrected Specification Change numbering.
January 2002	-012	Added Specification Clarifications 7, 8.
February 2002	-013	Added Erratum 8.
December 2002	-014	Removed Printed Board Assembly (PBA) information from the document, as this reference is no longer valid. Updated the Legal Disclaimer Section. Added Erratum 9.
November 2003	-015	Added Specification Clarification 9.



### **PREFACE**

This document is an update to the specifications contained in the *Intel*<sup>®</sup> *Desktop Board D850GB Technical Product Specification* (Order number A26080). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the Intel® Pentium® 4 Processor Specification Update (Order number 249199) for specification updates concerning the Intel Pentium 4 processor. Items contained in the Intel Pentium 4 Processor Specification Update that either do not apply to the desktop board D850GB or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel*<sup>®</sup> 82850 *Chipset*: 82850 *Memory Controller Hub (MCH) Specification Update* (Order Number 290691) for specification updates concerning the 82850 MCH Controller. Items contained in the 82850 *MCH Specification Update* that either do not apply to the desktop board D850GB or have been worked around are noted in this document. Otherwise, it should be assumed that any MCH errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the Intel® 82801 I/O Controller Hub (ICH) Specification Update (Order Number 290677) for specification updates concerning the 82801 I/O Controller Hub. Items contained in the Intel 82801 ICH Specification Update that either do not apply to the desktop board D850GB or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

#### Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Characterized errata may cause the desktop board D850GB's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all desktop boards.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Specification Update for the Intel® Desktop Board D850GB



### **GENERAL INFORMATION**

### **Basic Desktop Board D850GB Identification Information**

AA Revision	PBA Revision	<b>BIOS Revision</b>	Notes
A22917-306	A22920-306	GB85010A.86A.0040.P03	1-5
A22917-307	A22920-307	GB85010A.86A.0046.P05	1-5
A22917-308	A22920-308	GB85010A.86A.0048.P07	1-5
A22917-309	A22920-309	GB85010A.86A.0048.P07	1-5
A22917-310	A22920-310	GB85010A.86A.0056.P10	1-5
A23794-502	A23796-502	GB85010A.86A.0048.P07	1-5
A23794-503	A23796-503	GB85010A.86A.0048.P07	1-5
A23794-504	A23796-504	GB85010A.86A.0056.P10	1-5
A48535-902	A48536-902	GB85010A.86A.0054.P09	1-5
A48535-903	A48536-903	GB85010A.86A.0058.P12	1-5
A48535-904	A48536-904	GB85010A.86A.0063.P14	1-5
A48535-905	A48536-905	GB85010A.86A.0063.P14	1-5
A48535-906	A48536-906	GB85010A.86A.0063.P14	1-5
A48535-907	A48536-907	GB85010A.86A.0063.P14	1-5
A48527-902	A48528-902	GB85010A.86A.0054.P09	1-5
A48527-903	A48528-903	GB85010A.86A.0058.P12	1-5
A48527-904	A48528-904	GB85010A.86A.0063.P14	1-5
A48527-905	A48528-905	GB85010A.86A.0063.P14	1-5
A48527-906	A48528-906	GB85010A.86A.0063.P14	1-5
A48527-907	A48528-907	GB85010A.86A.0063.P14	1-5
A55888-900	A55889-900	GB85010A.86A.0054.P09	1-5
A55888-901	A55889-901	GB85010A.86A.0056.P10	1-5
A55888-902	A55889-902	GB85010A.86A.0058.P12	1-5
A55888-903	A55889-903	GB85010A.86A.0063.P14	1-5
A55888-904	A55889-904	GB85010A.86A.0063.P14	1-5
A55888-906	A55889-906	GB85010A.86A.0063.P14	1-5
A55888-907	A55889-907	GB85010A.86A.0063.P14	1-5

### NOTES:

1. The PBA number or AA number is found on a small label on the component side of the board.





2. The 82850 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82850 MCH	A2	SL4NG
82801BA ICH	B1' B4	SL4YG SL59Z
SST 49LF004 4Mbit FWH	NA	NA

- The following errata are contained in the Intel<sup>®</sup> Pentium<sup>®</sup> 4 Processor Specification Update (Order Number 249199) for the Pentium 4 processor and either do not apply to the desktop board D850GB or have been worked-around in this PBA and/or BIOS revision: None. All other errata associated with the processor apply to this PBA revision.
- 4. The following items are contained in the Intel<sup>®</sup> 82850 Memory Controller Hub (MCH) Specification Update (Order Number 290691) and either do not apply to the desktop board D850GB or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the MCH apply to this PBA revision.
- 5. The following items are contained in the Intel<sup>®</sup> 82801 I/O Controller Hub Specification Update (Order Number 290677) and either do not apply to the desktop board D850GB or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the ICH apply to this PBA revision.



### Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the desktop board D850GB. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

### **CODES USED IN SUMMARY TABLE**

Doc: Document change or update that will be implemented.

Fix: This erratum is intended to be fixed in a future revision of the desktop board,

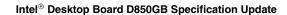
driver, or BIOS.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Shaded: This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
2	Doc	Support for faster Intel® Pentium® 4 processor
3	Doc	Support for faster Intel Pentium 4 Processors
4	Doc	Support for faster Intel Pentium 4 processors
NO.	PLANS	ERRATA
1	Fixed	Some SCSI host bus adapters may not boot to the hard disk drive with a bootable CD-ROM drive attached
2	Fixed	System may freeze when user password is enabled
3	Fixed	Certain audio Communication Network Riser (CNR) adapters are not recognized by the system BIOS or any operating system
4.	Fixed	Event log corruption in the system BIOS
5	Fixed	System BIOS will not properly configure multi-channel audio Communications Network Riser (CNR) cards
6	Fixed	BIOS recovery causes system hangs
7	Fixed	If the boot order is changed in the boot menu in BIOS Setup and custom defaults are saved, the saved boot order is not restored when the custom defaults are loaded.
8	Fix	System hang during POST may occur when using certain USB cameras
9	NoFix	System boot time may be excessive when using ECC memory
NO.	PLANS	SPECIFICATION CLARIFICATIONS
3	Doc	Change to description of Section 4.5, Security Menu
4	Doc	Change to description of Section 2.8, Connectors
5	Doc	Change to description of Section 2.8.3.2, Front Panel Connector
6	Doc	Change to description of Section 2.11.4, Fan Connector Current Capability
7	Doc	Change to description of Section 2.6, Interrupts





NO.	PLANS	SPECIFICATION CLARIFICATIONS (cont.)
8	Doc	Change to description of Section 2.7, PCI Interrupt Routing Map
9	Doc	Clarification of SMBus routing



### SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the Desktop Board D850GB Technical Product Specification (Order Number A26080). All Specification Changes will be incorporated into a future version of that specification.

#### 2. Support For Faster Intel® Pentium® 4 Processor

Section 1.4, Processor, will be changed in its entirety as follows:

#### 1.4 Processor



# **!** CAUTION

Use only the processors listed below. Use of unsupported processors can damage the D850GB board, the processor, and the power supply. See the Intel® Desktop Board 850GB Specification Update for the most up-to-date list of supported processors for the D850GB board.

The D850GB board supports a single Pentium® 4 processor with a system bus of 400 MHz. The D850GB board supports the processors listed in Table 4. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 4. **Supported Processors** 

Туре	Designation	System Bus	L2 Cache Size
Pentium® 4	1.3, 1.4, 1.5, and 1.7 GHz	400 MHz	256 KB
processor			



### NOTE

BIOS Revision GB85010A.86A.0056.P10 or later is required for the board to properly support 1.7 GHz processors.



### **!** CAUTION

Use only an ATX12V-compliant power supply with this board. ATX12V power supplies have two additional power leads that provide required supplemental power for the Intel Pentium 4 processor and the Intel 850 chipset. Always



connect both additional power supply leads of the ATX12V power supply, otherwise the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.2, page 16
Processor usage	Section 1.2, page 16
Power supply connectors	Section 2.8.2.3, page 56

#### 3. Support For Faster Intel® Pentium® 4 Processors

Section 1.4, Processor, will be changed in its entirety as follows:

#### 1.4 Processor



### **CAUTION**

Use only the processors listed below. Use of unsupported processors can damage the D850GB board, the processor, and the power supply. See the Intel® Desktop Board 850GB Specification Update for the most up-to-date list of supported processors for the D850GB board.

The D850GB board supports a single Pentium<sup>®</sup> 4 processor with a system bus of 400 MHz. The D850GB board supports the processors listed in Table 4. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 4. **Supported Processors** 

Туре	Designation	System Bus	L2 Cache Size
Pentium® 4 processor	1.3, 1.4, 1.5, 1.6, 1.7, and 1.8 GHz	400 MHz	256 KB



### NOTE

BIOS Revision GB85010A.86A.0056.P10 or later is required for the board to properly support 1.7 GHz processors.





Use only an ATX12V-compliant power supply with this board. ATX12V power supplies have two additional power leads that provide required supplemental power for the Intel<sup>®</sup> Pentium<sup>®</sup> 4 processor and the Intel<sup>®</sup> 850 chipset. Always connect both additional power supply leads of the ATX12V power supply, otherwise the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.2, page 16
Processor usage	Section 1.2, page 16
Power supply connectors	Section 2.8.2.3, page 56

#### 4. Support For Faster Intel® Pentium® 4 Processors

Section 1.4, Processor, will be changed in its entirety as follows:

#### 1.4 **Processor**



## **A** CAUTION

Use only the processors listed below. Use of unsupported processors can damage the D850GB board, the processor, and the power supply. See the Intel® Desktop Board 850GB Specification Update for the most up-to-date list of supported processors for the D850GB board.

The D850GB board supports a single Pentium 4 processor with a system bus of 400 MHz. The D850GB board supports the processors listed in Table 4. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 4. **Supported Processors** 

Туре	Designation	System Bus	L2 Cache Size	
Pentium® 4	1.3, 1.4, 1.5, 1.6, 1.7, 1.8	400 MHz	256 KB	
processor	GHz, 1.9, and 2.0			





### NOTE

BIOS Revision GB85010A.86A.0056.P10 or later is required for the board to properly support 1.7 GHz processors.



### **NOTE**

BIOS Revision GB85010A.86A.0063.P14 or later is required for the board to properly support 1.9 GHz or later processors.



# **A** CAUTION

Use only an ATX12V-compliant power supply with this board. ATX12V power supplies have two additional power leads that provide required supplemental power for the Intel® Pentium® 4 processor and the Intel® 850 chipset. Always connect both additional power supply leads of the ATX12V power supply, otherwise the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.2, page 16
Processor usage	Section 1.2, page 16
Power supply connectors	Section 2.8.2.3, page 56



### **ERRATA**

# 1. Some SCSI Host Bus Adapters May Not Boot to The Hard Disk Drive With a Bootable CD-ROM Drive Attached

**PROBLEM**: If a bootable CD-ROM is attached to the SCSI host bus adapter (HBA) and set as bootable in the setup menu of the SCSI HBA without bootable media installed, the system may not boot to the attached hard drive.

**IMPLICATION**: Users who wish to utilize a bootable SCSI CD-ROM in conjunction with a bootable hard drive on an add-in SCSI host bus adapter may not be able to boot to the hard drive if the SCSI adapter is set to recognize the CD-ROM as a bootable device.

WORKAROUND: Enable the CD-ROM as a bootable SCSI device only when using bootable media.

STATUS: This erratum was fixed in BIOS revision GB85010A.86A.0053.P08.

### 2. System May Freeze When User Password is Enabled

**PROBLEM:** If both User Password and Unattended Start are enabled in the BIOS Setup program with a PS/2\* keyboard and mouse attached, the system may freeze after start-up in Windows\* 2000.

**IMPLICATION:** With a PS/2 keyboard and mouse attached to the system and if the user has the User password and Unattended start option enabled in the BIOS setup menu, the user may experience a system lock up after booting into Windows 2000.

**WORKAROUND:** This behavior is not exhibited when a USB keyboard and mouse are utilized in lieu of the PS/2 keyboard and mouse.

STATUS: This erratum was fixed in BIOS revision GB85010A.86A.0047.P06

# 3. Certain Audio Communication Network Riser (CNR) Adapters Are Not Recognized by The System BIOS or Any Operating System

**PROBLEM:** CNR Audio add-in devices that can function as either a secondary audio codec in a multi-channel upgrade or as the primary audio codec, are configured as a secondary codec on desktop boards that do not have a primary audio codec. This results in the CNR audio add-in device not being recognized by the system BIOS or any operating system.

**IMPLICATION:** If a user requires a CNR audio device that will function as a primary audio codec or a CNR device that will function as a secondary audio codec in a multi-channel upgrade on a desktop board that does not have a primary audio codec, the CNR device will not be recognized by the system BIOS or the operating system.

WORKAROUND: None.

STATUS: This erratum was fixed in PBA revisions A22920-310 or later.



### 4. Event Log Corruption in The System BIOS

**PROBLEM:** Event log data in the system BIOS Advanced menu, Event Log Configuration sub-menu, View Event Log option is corrupt displaying an array of "-3/4" characters. This anomaly is present only in BIOS revisions GB85010A.86A.0053.P08 and GB85010A.86A.0054.P09.

**IMPLICATION:** Due to corruption of the View Event Log option in the system BIOS, system events will not be captured and stored.

WORKAROUND: None.

**STATUS:** This erratum was fixed in BIOS revision GB85010A.86A.0056.P10.

# 5. System BIOS Will Not Properly Configure Multi-Channel Audio Communications Network Riser (CNR) Cards

**PROBLEM:** During the system boot process, the system BIOS compares the multi-channel signature stored in BIOS with the multi-channel signature stored in the audio CNR EEPROM. If the signatures match, the system BIOS then programs the device ID in the PCI configuration space with the multi-channel model ID from the CNR EEPROM. The system BIOS for this desktop board incorrectly programs the device ID in the PCI configuration space. When the audio driver that supports multi-channel functionality is installed, the driver may not install correctly or may not install at all.

**IMPLICATION:** Users who install a multi-channel audio CNR card may experience difficulty installing the manufacturers audio drivers.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision GB85010A.86A.0060.P13.

### 6. BIOS Recovery Causes System Hangs

**PROBLEM:** When upgrading the BIOS in the recovery mode to a different revision than is currently installed, the Vital Product Data (VPD) file is not correctly updated, causing the system to hang.

**IMPLICATION:** Users who need to utilize the recovery mode to reinstall the BIOS will experience system hangs if recovering the BIOS to a different BIOS revision than that already installed.

**WORKAROUND:** If the recovery mode is needed to reinstall the system BIOS, first recover the BIOS with the same BIOS revision that was installed when the need for a BIOS recovery occurred. After which, use IFLASH.EXE or the Express BIOS Update Utility (EBU) to install the desired BIOS revision.

STATUS: This erratum was fixed in BIOS revision GB85010A.86A.0060.P13.

# 7. If The Boot Order is Changed in The Boot Menu in BIOS Setup And Custom Defaults Are Saved, The Saved Boot Order is Not Restored When The Custom Defaults Are Loaded.

**PROBLEM**: Changing the boot order in the Boot Menu of the BIOS setup menu and saving that change as custom defaults will result in an incorrect boot order after the custom defaults are loaded.



**IMPLICATION:** Customers that require a different boot order that is saved as custom defaults will experience a different boot order than was saved as custom defaults once the custom defaults are loaded.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision GB85010A.86A.0076.P17

# 8. System Hang During POST May Occur When Using Certain USB Cameras

**PROBLEM:** During the system boot, certain USB cameras may cause a hang during POST if the camera is on during the boot process.

**IMPLICATION:** Some USB cameras may cause a system hang if the camera is on during system boot due to the BIOS incorrectly identifying the camera as a bootable device.

**WORKAROUND:** Ensure that the USB camera is off during the system boot process.

**STATUS:** This erratum may be fixed in a future BIOS revision.

### 9. System Boot Time May be Excessive When Using ECC Memory

**PROBLEM:** A blank screen may occur for as long as one minute during POST while the system is booting, when ECC memory is utilized.

**IMPLICATION:** When BIOS detects ECC memory during the system boot process, BIOS will run memory scans multiple times resulting in a delayed POST (up to one minute) making the system seem unresponsive.

WORKAROUND: None.

**STATUS:** This erratum will not be fixed.



### **SPECIFICATION CLARIFICATIONS**

The Specification Clarifications listed in this section apply to the *Desktop Board D850GB Technical Product Specification* (Order Number A26080). All Specification Changes will be incorporated into a future version of that specification.

### 3. Change to Description of Section 4.5, Security Menu

Section 4.5, Security Menu, will be replaced in its entirety as follows:

### 4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
-------------	------	----------	----------	-------	------	------

The menu represented by Table 72 is for setting passwords and security features.

Table 72. Security Menu

If no password entered previously:				
Feature	Options	Description		
Supervisor Password Is	No options	Reports if there is a supervisor password set.		
User Password Is	No options	Reports if there is a user password set.		
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.		
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.		
Clear User Password (Note 1)	Yes (default)     No	Clears the user password.		

continued



Table 72. Security Menu (continued)

If no password entered previously:				
Feature	Options	Description		
User Access Level (Note 2)	<ul><li>Limited</li><li>No Access</li><li>View Only</li><li>Full (default)</li></ul>	Sets BIOS Setup Utility access rights for user level.		
Unattended Start (Notes 1,3-4)	Disabled (default)     Enabled	Enabled allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.		

#### Notes:

- This feature appears only if a user password has been set.
- This feature appears only if a supervisor password has been set.
- If both Legacy USB and Unattended Start are set to enabled in the BIOS setup menu, USB aware operating systems can unlock a PS/2\* style keyboard and mouse without requiring the user to enter a password.
- 4. When Unattended Start is enabled in the BIOS setup menu, a USB aware operating system may override user password protection if used in conjunction with a USB keyboard and mouse without requiring the user to enter a password.

#### 4. Change to Description of Section 2.8, Connectors

Section 2.8, Connectors will change in its entirety as follows:

#### 2.8 **Connectors**



## **!** CAUTION

Only the back panel connectors and the front panel USB connector of the D850GB board have overcurrent protection. All of the remaining internal connectors of the D850GB board are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.



This section describes the board's connectors. The connectors can be divided into the following groups:

- Back panel I/O connectors (see page 50)
  - PS/2\* keyboard and mouse
  - USB (two)
  - Parallel port
  - Serial port
  - LAN
  - Audio (Line out, Line in, and Mic in)
- Internal I/O connectors (see page 53)
  - Audio (ATAPI CD-ROM, legacy-style CD-ROM, and auxiliary line input)
  - Fans (four)
  - Power (three)
  - Wake on LAN\* technology
  - Wake on Ring
  - Add-in boards (one CNR connector, one AGP connector, and five PCI bus connectors)
  - IDE (two)
  - Diskette drive
  - SCSI LED
- External I/O connectors (see page 65)
  - Front panel USB
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)



### 5. Change to Description of Section 2.8.3.2, Front Panel Connector

Section 2.8.3.2, Front Panel Connector will change in its entirety as follows:

### 2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table lists the signal names of the front panel connector.

Table 46. Front Panel Connector (J9D2)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
9	+5 V	Out	Reserved	10	N/C		
11	Reserved	In	Reserved	12	Ground		Ground
13	Ground		Ground	14	(pin removed)		Not connected
15	Reserved	Out	Reserved	16	+5 V	Out	Power

# 6. Change to Description of Section 2.11.4, Fan Connector Current Capability

Section 2.11.4, Fan Connector Current Capability will change in its entirety as follows:

### 2.11.4 Fan Connector Current Capability

The D850GB board is designed to supply a maximum of 225 mA per fan connector.



### **CAUTION**

Use of a Processor Fan with greater than 220mA of current consumption will result in a fan startup failure.



### 7. Change to Description of Section 2.6, Interrupts

Section 2.6, Interrupts, will change in its entirety as follows:

### 2.6 Interrupts

The Interrupts can go through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the Intel<sup>®</sup> ICH2 component. The PIC is supported in Windows\* 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and support a total of 24 interrupts.

Table 15. Interrupts

Table 13. III	ierrupts
IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option) / User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for Intel ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16	AGP video (through PIRQA) (Note 2)
17	AC' 97 Audio/User Available (through PIRQB) (Note 2)
18	User available (through PIRQC) (Note 2)
19	Intel ICH2 USB Controller #1 (through PIRQD) (Note 2)

continued



Table 15. Interrupts (continued)

IRQ	System Resource
20	Intel® ICH2 LAN (optional) (through PIRQE) (Note 2)
21	User available (through PIRQF) (Note 2)
22	User available (through PIRQG) (Note 2)
23	Intel ICH2 USB Controller #2/ User Available (through PIRQH) (Note 2)

Note 1: Default, but can be changed to another IRQ.

Note 2: Available in APIC mode only.

### 8. Change to Description of Section 2.7, PCI Interrupt Routing Map

Section 2.7, PCI Interrupt Routing Map, will change in its entirety as follows:

### 2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.



The Intel® ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D850GB board and therefore share the same interrupt. Table 16 shows an example of how the PIRQ signals are routed on the D850GB board.

For example, using Table 16 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 4. In PCI bus connector 4, INTA is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 4 now shares interrupts with these onboard interrupt sources.

**PCI Interrupt Routing Map** Table 16.

·	Intel ICH2 PIRQ Signal Name				
<b>PCI Interrupt Source</b>	PIRQF	PIRQG	PIRQH	PIRQB	Other
AGP connector				INTB	INTA to PIRQA
Intel® ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
Intel ICH2 USB controller #2			INTC		
Intel ICH2 Audio / Modem				INTB	
Intel ICH2 LAN					INTA to PIRQE
PCI Bus Connector 1 (J4E1)	INTA	INTB	INTC	INTD	
PCI Bus Connector 2 (J4D1)	INTD	INTA	INTB	INTC	
PCI Bus Connector 3 (J4C1)	INTC	INTD	INTA	INTB	
PCI Bus Connector 4 (J4B1)	INTB	INTC	INTD	INTA	
PCI Bus Connector 5 (J4A1)	INTA	INTB	INTC	INTD	

### **■ NOTE**

In PIC mode, the Intel ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12,14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. In APIC mode, the allocation of PIRQ lines to IRQ signals is as shown in Table 16.



### 9. Clarification of SMBus Routing

Section 2.8.2.1 will change in its entirety as follows:

### 2.8.2.1 Expansion Slots

The board has the following expansion slots:

- One AGP connector at location J5E1 (ATX expansion slot 6). The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.
- Five PCI local bus slots (compliant with PCI rev 2.2 specification). The SMBus is routed to PCI bus connector 2 only at location J4D1 (ATX expansion slot 4). PCI add-in cards with SMBus support can access sensor data and other information residing on the desktop board.
- One CNR (optional), shared with PCI bus connector 5 at location J4A1 (ATX expansion slot 1).

### **◯** NOTE

The SMBus routing to the PCI bus connectors does not conform to the PCI Engineering Change Notice (ECN) "Addition of the SMBus to the PCI Connector ECN", dated October 5th, 2000. The ECN specifies that SMBus signals must be routed to all PCI bus connectors. On this board, SMBus signals are routed to PCI bus connector 2 only.

Add-in cards that implement PCI bus connector pins A40 and A41 for any purpose other than SMBCLK (SMBus clock) and SMBDAT (SMBus data) should not be installed in PCI bus connector 2.

# For information about Refer to Addition of the SMBus to the PCI Connector ECN http://www.pcis

Addition of the SMBus to the PCI Connector ECN	http://www.pcisig.com/data/s
	pecifications/smb ecn 0405
	<u>01.pdf</u>

### **◯** NOTE

This document references back-panel slot numbering with respect to processor location on the board. The AGP slot is not numbered. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. The CNR slot shares PCI slot 5. The ATX/MicroATX specifications identify expansion slot locations



with respect to the far edge of a full-sized ATX chassis. The ATX specification and the board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type (PCI vs. AGP), but refers to an actual slot location on a chassis. Figure 11 on page 59 illustrates the board's PCI slot numbering.