Intel® Desktop Board D815EGEW Specification Update

Release Date: February 2002

Order Number: A77134-003

The desktop board D815EGEW may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
November 2001	-001	This document is the first Specification Update for the Intel® Desktop Board D815EGEW. Added Erratum 1.
January 2002	-002	Updated General Information section. Added Specification Clarifications 1, 2. Added Documentation Changes 1, 2.
February 2002	-003	Added Erratum 2. Updated General Information.

PREFACE

This document is an update to the specifications contained in the *Desktop Board D815EGEW Technical Product Specification* (Order number A73971). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® III Processor Specification Update* (Order number 244453) for specification updates concerning the Pentium III processor. Items contained in the *Pentium III Processor Specification Update* that either do not apply to the desktop board D815EGEW or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® Celeron® Processor Specification Update* (Order number 243748) for specification updates concerning the Intel Celeron processor. Items contained in the *Intel Celeron Processor Specification Update* that either do not apply to the desktop board D815EGEW or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82815 Chipset: 82815 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) for specification updates concerning the 82815 GMCH Controller. Items contained in the *82815 GMCH Specification Update* that either do not apply to the desktop board D815EGEW or have been worked around are noted in this document. Otherwise, it should be assumed that any GMCH errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82801 I/O Controller Hub (ICH) Specification Update* (Order Number 290677) for specification updates concerning the 82801 I/O Controller Hub. Items contained in the *Intel 82801 ICH Specification Update* that either do not apply to the desktop board D815EGEW or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the desktop board D815EGEW behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for Desktop Board D815EGEW

GENERAL INFORMATION

Basic Desktop Board D815EGEW Identification Information

AA Revision	PBA Revision	BIOS Revision	Notes
A75560-100	A75561-100	EW81510A.86A.0039.P02	1-6
A75560-200	A75561-200	EW81510A.86A.0044.P03	1-6
A69600-103	A69601-103	EW81510A.86A.0039.P02	1-6
A69600-200	A69601-200	EW81510A.86A.0044.P03	1-6

NOTES:

1. The PBA number or AA number is found on a small label on the component side of the board.
2. The 82815 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82815 GMCH	A2T	SL5YN
82801BA ICH	B5	SL5WK
82802AB FWH	A1	SB48

3. The following errata are contained in the *Pentium® III Processor Specification Update* (Order Number 244453) for the Pentium III processor and either do not apply to the Desktop Board D815EGEW or have been worked-around in this PBA and/or BIOS revision: 1. All other errata associated with the processor apply to this PBA revision.
4. The following errata are contained in the *Intel® Celeron® Processor Specification Update* (Order Number 243748) for the Celeron processor and either do not apply to the Desktop Board D815EGEW or have been worked-around in this PBA and/or BIOS revision: None. All other errata associated with the processor apply to this PBA revision.
5. The following items are contained in the *Intel® 82815 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) and either do not apply to the Desktop Board D815EGEW or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the GMCH apply to this PBA revision.
6. The following items are contained in the *Intel® 82801 I/O Controller Hub Specification Update* (Order Number 290677) and either do not apply to the Desktop Board D815EGEW or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the ICH apply to this PBA revision.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the desktop board D815EGEW. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the desktop board or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	ERRATA
1	Fixed	Intel® Pentium® III processor Erratum E76
2	Fix	System hang during POST may occur when using certain USB cameras
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Change to description of Section 2.6, Interrupts
2	Doc	Change to description of Section 2.7, PCI Interrupt Routing Map
NO.	**PLANS**	**DOCUMENTATION CHANGES**
1	Doc	Change to description of The BIOS identification string in the Revision History
2	Doc	Change to description of Section 3.1, Introduction

ERRATA

1. Intel® Pentium® III Processor Erratum E76

PROBLEM: For a complete description of the Pentium® III processor erratum E76, see the Pentium III Specification Update, order number 244453 found at http://developer.intel.com/design/PentiumIII/specupdt/.

IMPLICATION: For a complete description of the Pentium III processor erratum E76, see the Pentium III Specification Update, order number 244453 found at http://developer.intel.com/design/PentiumIII/specupdt/.

WORKAROUND: Update the D815EEA2/D815EPEA2 desktop board with BIOS revision EA81520A.86A.0014.P09.

STATUS: This erratum was addressed in BIOS revision EW81510A.86A.0039.P02.

2. System Hang During POST May Occur When Using Certain USB Cameras

PROBLEM: During the system boot, certain USB cameras may cause a hang during POST if the camera is on during the boot process.

IMPLICATION: Some USB cameras may cause a system hang if the camera is on during system boot due to the BIOS incorrectly identifying the camera as a bootable device.

WORKAROUND: Ensure that the USB camera is off during the system boot process.

STATUS: This erratum may be fixed in a future BIOS revision.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Desktop Board D815EGEW Technical Product Specification* (Order Number A73971). All Specification Clarifications will be incorporated into a future version of that specification.

1. Change to Description of Section 2.6, Interrupts

Section 2.6, Interrupts, will change in its entirety as follows:

2.6 Interrupts

The Interrupts can go through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the Intel ICH2 component. The PIC is supported in Windows* 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and support a total of 24 interrupts.

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option) / User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for Intel ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

continued

Table 16. Interrupts (continued)

IRQ	System Resource
16	AGP video (through PIRQA) (Note 2)
17	AC' 97 Audio/User Available (through PIRQB) (Note 2)
18	User available (through PIRQC) (Note 2)
19	Intel® ICH2 USB Controller #1 (through PIRQD) (Note 2)
20	Intel ICH2 LAN (optional) (through PIRQE) (Note 2)
21	User available (through PIRQF) (Note 2)
22	User available (through PIRQG) (Note 2)
23	Intel ICH2 USB Controller #2/ User Available (through PIRQH) (Note 2)

Note 1: Default, but can be changed to another IRQ.

Note 2: Available in APIC mode only.

2. Change to Description of Section 2.7, PCI Interrupt Routing Map

Section 2.7, PCI Interrupt Routing Map, will change in its entirety as follows:

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The Intel ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D815EGEW board and therefore share the same interrupt. Table 17 shows an example of how the PIRQ signals are routed on the D815EGEW board.

For example, using Table 17 as a reference, assume that an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQH. The add-in card in PCI bus connector 3 now shares interrupts with these onboard interrupt sources.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name				
	PIRQF	**PIRQG**	**PIRQH**	**PIRQB**	**Other**
GMCH				INTB	INTA to PIRQA
Intel® ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
Intel ICH2 audio/modem				INTB	
Intel ICH2 LAN					INTA to PIRQE
PCI bus connector 1	INTA	INTB	INTC	INTD	
PCI bus connector 2	INTD	INTA	INTB	INTC	
PCI bus connector 3	INTC	INTD	INTA	INTB	
PCI bus connector 4	INTB	INTC	INTD	INTA	

NOTE

In PIC mode, the Intel ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12,14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. In APIC mode, the allocation of PIRQ lines to IRQ signals is as shown in Table 17.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Desktop Board D815EGEW Technical Product Specification* (Order Number A73971). All Documentation Changes will be incorporated into a future version of that specification.

1. Change to Description of The BIOS Identification String in the Revision History

The first paragraph of the Revision History will be changed in its entirety as follows:

This product specification applies to only standard D815EGEW boards with BIOS identifier EW81510A.86A.

2. Change to Description of Section 3.1, Introduction

Section 3.1, Introduction, will change in its entirety as follows:

3.1 Introduction

The D815EGEW boards uses an Intel/AMI BIOS, which is stored in flash memory and can be updated using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The D815EGEW board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as EW81510A.86A.

When the D815EGEW board's BIOS Setup configuration jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

For information about	Refer to
The D815EGEW board's compliance level with Plug and Play	Table 3, page 17