Advanced/MA Memory Map, I/O Map, IRQs, DMA

MEMORY MAP

Address Range (Decimal)	*Address Range (hex)*	*Size*	*Description*
1024K-131072K	100000-8000000	127M	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI System BIOS
952K-959K	EE000-EFFFF	8K	Main BIOS (available as UMB)
948K-951K	ED000-EDFFF	4K	ESCD (Plug 'N' Play configuration area)
944-947K	EC000-ECFFF	4K	OEM LOGO (available as UMB)
896K-943K	E0000-EBFFF	48K	BIOS RESERVED (Currently available as UMB)
800-895K	C8000-DFFFF	96K	Available HI DOS memory (open to ISA 7
640K-799K	A0000-C7FFF	160K	Video memory and BIOS
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K-638K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

The table above details the Advanced/MA memory map. The ECSD area from EA000-EDFFF is not available for use as an Upper Memory Block (UMB) by memory managers. The area from E0000-EBFFF is currently not used by the BIOS and is available for use as UMB by memory managers. Parts of this area may be used by future versions of the BIOS to add increased functionality.

I/O MAP

Address (hex)	*Size*	*Description*
0000 - 000F	16 bytes	PIIX - DMA 1
0020 - 0021	2 bytes	PIIX - Interrupt Controller 1
002E - 002F	2 bytes	Ultra I/O configuration registers
0040 - 0043	4 bytes	PIIX - Timer 1
0048 - 004B	4 bytes	PIIX - Timer 2
0060	1 byte	Keyboard Controller Data Byte
0061	1 byte	PIIX - NMI, speaker control
0064	1 byte	Kbd Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX - Enable NMI
0070, bits 6:0	7 bits	PIIX - Real Time Clock,
0071	1 byte	PIIX - Real Time Clock, Data
0078	1 byte	Reserved - Brd. Config.
0079	1 byte	Reserved - Brd. Config.
0080 - 008F	16 bytes	PIIX - DMA Page Register
00A0 - 00A1	2 bytes	PIIX - Interrupt Controller 2
00C0 - 00DE	31 bytes	PIIX - DMA 2
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0200 - 0207	8 bytes	Game Port
0220 - 022F	8 bytes	CS4232 audio
0278 - 027B	4 bytes	Parallel Port 2
02F8 - 02FF	8 bytes	On-Board Serial Port 2
0330 - 0331	1 bytes	MPU - 401 (MIDI)
0376	1 byte	Sec IDE Chan Cmd Port
0377	1 byte	Sec IDE Chan Stat Port
0378 - 037F	8 bytes	Parallel Port 1

Address (hex)	*Size*	*Description*
0388 - 038B	4 bytes	CS4232 audio
03B4 - 03B5	2 bytes	Mach64 CT
03BA	1 byte	Mach64 CT
03BC - 03BF	4 bytes	Parallel Port 3
03C0 - 03CA	12 bytes	Mach64 CT
03CC	1 byte	Mach64 CT
03CE - 03CF	2 bytes	Mach64 CT
03D4 - 03D5	2 bytes	Mach64 CT
03DA	1 byte	Mach64 CT
03E8 - 03EF	8 bytes	Serial Port 3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Pri IDE Chan Cmd Port
03F7 (Write)	1 byte	Floppy Chan 1 Cmd
03F7, bit 7	1 bit	Floppy Disk Chg Chan 1
03F7, bits 6:0	7 bits	Pri IDE Chan Status Port
03F8 - 03FF	8 bytes	On-Board Serial Port 1
LPT + 400h	8 bytes	ECP port, LPT + 400h
04D0 - 04D1	2 bytes	Edge/Level INTR Control
0608 - 060B	4 bytes	CS4232 audio
0CF8*	4 bytes	PCI Config Address Reg.
0CF9	1 byte	Turbo & Reset control
0CFC-0CFF*	4 bytes	PCI Config Data Reg
0FF0 - 0FF7	8 bytes	CS4232 audio ctrl
FF00 - FF07	8 bytes	IDE Bus Master Reg.
FFA0 - FFA7	8 bytes	IDE primary channel
FFA8 - FFAF	8 bytes	IDE secondary channel

Table D-1. Advanced/MA I/O Address Map (* Only accessible by DWORD accesses.)

I/O Port 78 is reserved for BIOS use. Port 79 is a read only port, the bit definitions are shown below in Table D-2.

Bit #	*Description*	*Bit = 1*	*Bit = 0*
0	Reserved	n/a	n/a
1	Soft Off capable power supply present	No	Yes
2	On-board Audio present	Yes	No
3	External CPU clock	Table B-2	Table B-2
4	External CPU clock	Table B-2	Table B-2
5	Setup Disable	Enable access	Disable access
6	Clear CMOS	Keep values	Clear values
7	Password Clear	Keep password	Clear password

Table D-2. Advanced/MA Port 79 Definition

PCI CONFIGURATION SPACE MAP

The 82430FX chipset uses Configuration Mechanism 1 to access PCI configuration space. The PCI Configuration Address is a 32-bit register located at CF8h, the PCI Configuration Data is a 32-bit register located at CFCh. These registers are only accessible by full DWORD accesses. The table below lists the PCI bus and device numbers used by the baseboard.

Bus Number (hex)	*Dev Number (hex)*	*Func. Number (hex)*	*Description*
00	00	00	Intel 82437FX (TSC)
00	07	00	Intel 82371FB (PIIX) PCI/ISA bridge
00	07	01	Intel 82371FB (PIIX) IDE Bus Master
00	08	00	ATI Mach64 CT graphics controller
00	11	00	PCI Expansion Slot
00	13	00	PCI Expansion Slot

INTERRUPTS & DMA CHANNELS

IRQ	*System Resource*
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard buffer full
2	Reserved, Cascade interrupt from slave PIC
3	Serial Port 2
4	Serial Port 1
5	On-board Audio
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	On-board Audio (MPU-401)
10	User available
11	User available
12	On-board Mouse Port (Avail if no PS/2 mouse)
13	Reserved, Math coprocessor
14	Primary on-board IDE (Avail if IDE disabled)
15	Secondary on-brd IDE (Avail if IDE disabled)

Table F-1. Advanced/MA Interrupts (default settings)

DMA	*Data Width*	*System Resource*
0	8- or 16-bits	On-board Audio
1	8- or 16-bits	On-board Audio
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port (for ECP/EPP Config.)
4		Reserved - Cascade channel
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

Table F-2. Advanced/MA DMA Map (default settings)

SOFT-OFF CONTROL

The Advanced/MA design supports Soft off control via the SMM code in the BIOS. The CS1 pin out of the National 306B Ultra I/O controller is connected to the Soft off control line in our power supply circuit. The registers in the Ultra I/O controller that sets the I/O address and control of the CS1 pin is NOT setup until the SMM code is activated. The code performs the following operations:

OUT 0Ch to I/O port 2Eh	OUT 11h to I/O port 2Eh	OUT 0Dh to I/O port 2Eh
OUT 75h to I/O port 2Fh	OUT 00h to I/O port 2Fh	OUT A0h to I/O port 2Fh

After setting the above registers, any read operation to I/O location 75H will trigger the Softoff circuit and turn the power supply off.