SUPER®

SUPER P6DBS
SUPER P6DBE
SUPER P6DBU
SUPER P6SBU
SUPER P6SBS
SUPER P6SBA

USER'S AND BIOS MANUAL

Revision 2.3

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Preface

About This Manual

This manual is written for system houses, PC technicians and knowledgeable PC end users. It provides information for the installation and use of SUPER P6DBS/P6DBE/P6DBU/P6SBU/P6SBS/P6SBA motherboard. SUPER P6DBS/P6DBE/P6DBU/P6SBU/P6SBS/P6SBA supports Pentium II 400/350/333/300/266/233 MHz.

The Pentium II processor with the Dual Independent Bus Architecture is housed in a new package technology called the Single Edge Contact (S.E.C.) cartridge. This new cartridge package and its associated "Slot 1" infrastructure will provide the headroom for future high-performance processors.

Manual Organization

Chapter 1, Introduction, describes the features, specifications and performance of the SUPER P6DBS/P6DBE/P6DBU/P6SBU/P6SBS/P6SBA system board, provides detailed information about the chipset, and offers warranty information.

Refer to Chapter 2, Installation, for instructions on how to install the Pentium II processor, the retention mechanism, and the heat sink support. This chapter provides you with the instructions for handling static-sensitive devices. Read this chapter when you want to install DIM modules and to mount the system board in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, IDE interfaces, parallel port, serial ports, as well as the cables for the power supply, reset cable, Keylock/Power LED, speaker and keyboard.

If you encounter any problem, please see Chapter 3, Troubleshooting, which describes troubleshooting procedures for video, memory, and the setup configuration stored in memory. For quick reference, a general FAQ [frequently asked questions] is provided. Instructions are also included for technical support procedure, for returning merchandise for service and for BIOS upgrades using our BBS#.

See Chapter 4 for configuration data and BIOS features.

Chapter 5 has information on running setup and includes default settings for Standard Setup, Advanced Setup, Chipset function, Power Management, PCI/ PnP Setup and Peripheral Setup.

Appendix A offers information on BIOS error beep codes and messages.

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P6DBU/P6SBU

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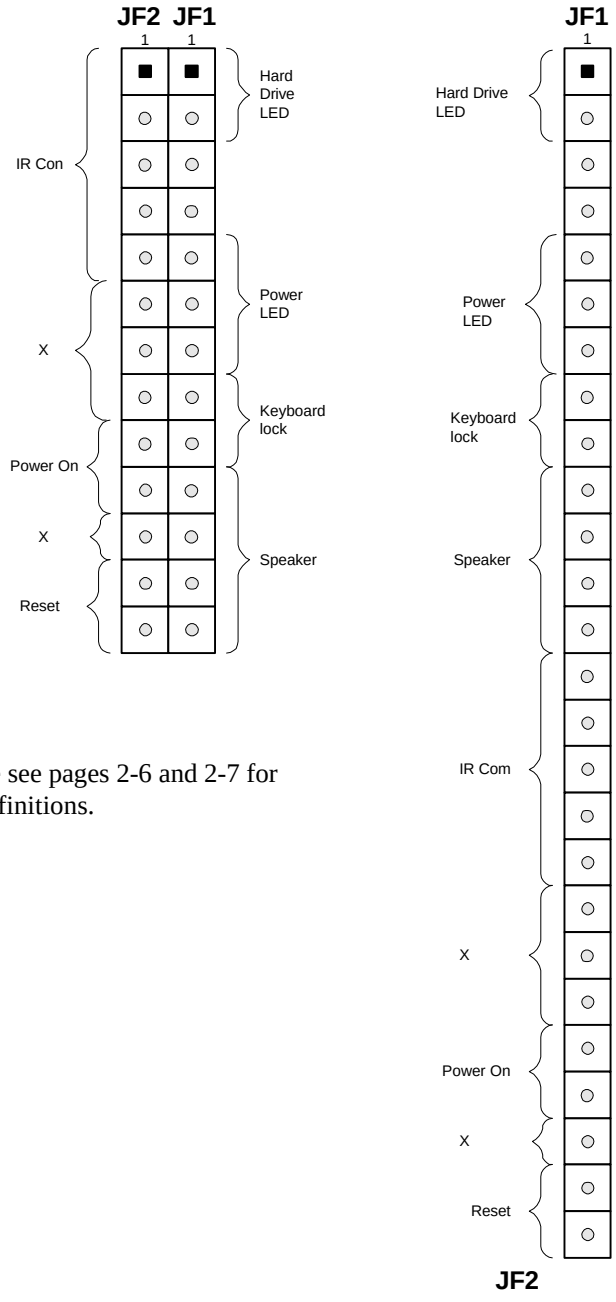
Front Control Panel Connector



Please see pages 2-6 and 2-7 for pin definitions.

Chapter 1
Introduction

1-1 Overview

SUPER P6DBS/P6DBE/P6DBU/P6SBU/P6SBS/P6SBA supports Pentium II 233/266/300/333 MHz processors and *Celeron 266/300 or higher at 66MHz bus speed or Pentium II 350/400 MHz processors at 100MHz bus speed. SUPER P6DBU, P6DBS, and P6DBE supports dual Pentium II processors. SUPER P6SBU/P6SBS/P6SBA supports a single Pentium II processor. All six motherboards are based on Intel's 440BX chipset which enables 66/100 MHz system bus speed, Accelerated Graphics Port (AGP), Wake-on-LAN™, SDRAM, concurrent PCI and Ultra DMA 33 MB/s burst data transfer rate.

While all of the motherboards are ATX form factor, P6DBU and P6DBE have 5 PCI and 2 ISA with one shared slot. SUPER P6DBS, P6SBU, P6SBS and P6SBA have 4 PCI and 3 ISA with one shared slot. All six motherboards have the AGP port, and can accommodate a total of 1 GB EDO at 66 MHz or 512 MB unbuffered SDRAM or 1 GB registered SDRAM memory with 4 168-pin DIMM sockets.

AGP reduces contention with the CPU and I/O devices by broadening the bandwidth of graphics to memory. It delivers a maximum of 532 MB/s 2x transfer mode which is quadruple the PCI speed!

Wake on LAN allows remote network management and configuration of the PC, even in off-hours when the PC is turned off. This reduces the complexity of managing the network.

Other features that maximize customer satisfaction and simplicity in managing the computer are PC 98-ready and support for Advanced Configuration and Power Interface (ACPI). With PC Health Monitoring, you can protect your system from problems before they even occur.

Included I/O on all motherboards are 2 EIDE ports, a floppy port, an ECP/EPP parallel port, a PS/2 mouse and PS/2 keyboard, 2 serial ports, an infrared port and 2 USB ports. SUPER P6DBUand P6SBU provide on-board Adaptec 7890 Ultra II SCSI controller with data transfer rate of up to 80 MB/s, and optional **RAIDport III (ARO-1130xA-2)****. SUPER P6DBS and P6SBS have

Note: Celeron is single processor only

***** See bottom of page 2***

integrated on-board Adaptec 7895 MultiChannel UW SCSI controller. The dual channels allow data transfer rate of 40 MB/s per channel. Additionally, these two motherboards have a RAID port on-board to support the **Adaptec ARO-1130xA RAIDport II card**** for increase I/O performance and fault tolerance.

********The ***x*** *in 1130 xA and 1130 xA-2 refers to the RAIDport workstation driver (1130 CA) or server driver (1130 SA) depending on software used. Please note: 1130 xA is compatible with NT Workstation, NT Server and Netware Server. The 1130 xA-2 is only compatible with NT Workstation at this time. Check the Adaptec web site for further information: www.adaptec.com.*

SUPER P6DBS

Figure 1-1. SUPER P6DBS Motherboard Picture

SUPER P6DBE

Figure 1-2. SUPER P6DBE Motherboard Picture

SUPER P6DBU

Figure 1-3. SUPER P6DBU Motherboard Picture

SUPER P6SBU

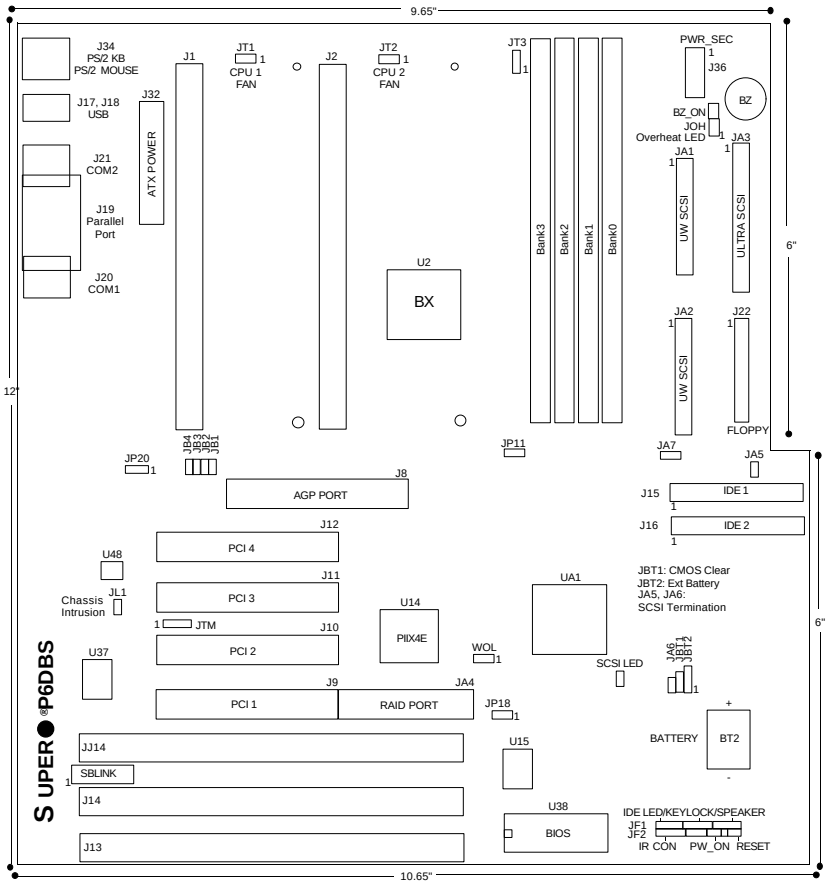
Figure 1-4. SUPER P6SBU Motherboard Picture

SUPER P6SBS

Figure 1-5. SUPER P6SBS Motherboard Picture

SUPER P6SBA

Figure 1-6. SUPER P6SBA Motherboard Picture



———— Manufacturer Settings ————

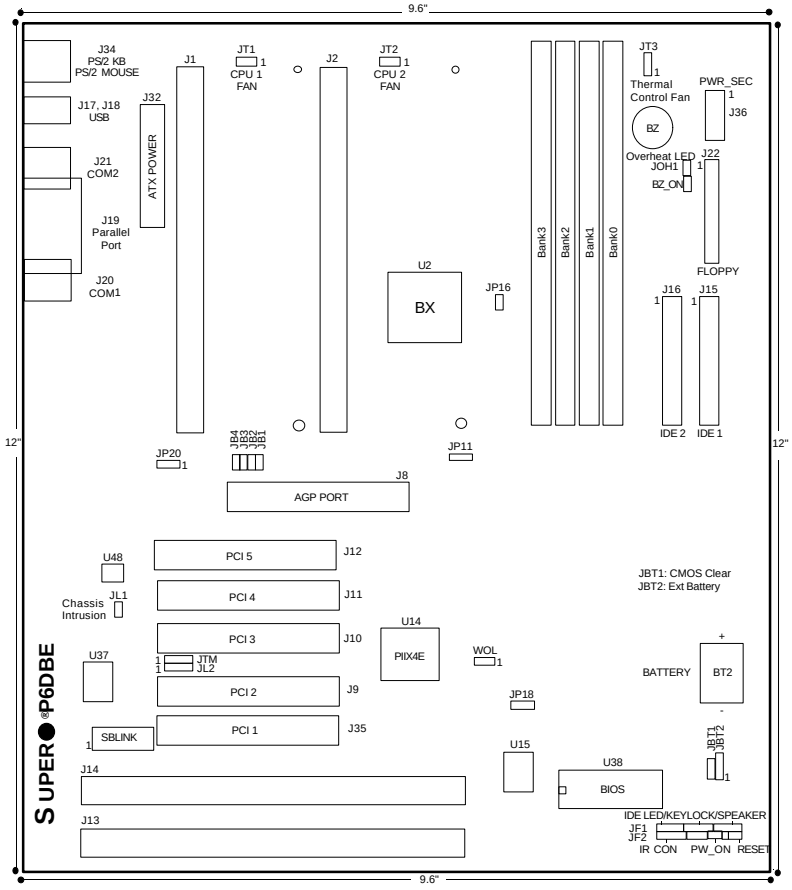
JBT1:	1-2 (default)
	2-3 CMOS Clear
	* To clear the CMOS completely, disconnect the power source.
JL1:	OFF (default)
	ON (intrusion)
JP11:	1-2 Auto
	2-3 66 MHz
	OFF 100 MHz
JP20:	1-2 PIIX CTL PD State
	2-3 BIOS CTL PD State (default)
WOL:	Wake-on-LAN

————————Pentium II CPU Speed————————

	JB1	JB2	JB3	JB4
x3	ON	OFF	ON	ON
x3.5	OFF	OFF	ON	ON
x4	ON	ON	OFF	ON
x4.5	OFF	ON	OFF	ON
x5	ON	OFF	OFF	ON
x5.5	OFF	OFF	OFF	ON
x6	ON	ON	ON	OFF

***Note: To Enable Overheat Buzzer place a jumper on BZ_On.**

Figure 1-7. SUPER P6DBS Motherboard Layout



——— Manufacturer Settings ———

JBT1: 1-2 (default)
2-3 CMOS Clear
To clear the CMOS completely, disconnect the power source.

JL1: OFF (default)
ON (intrusion)

JP11: 1-2 Auto
2-3 66 MHz
OFF 100 MHz

JP20: 1-2 PIIX CTL PD State
2-3 BIOS CTL PD State (default)

WOL: Wake-on-LAN

———————————————

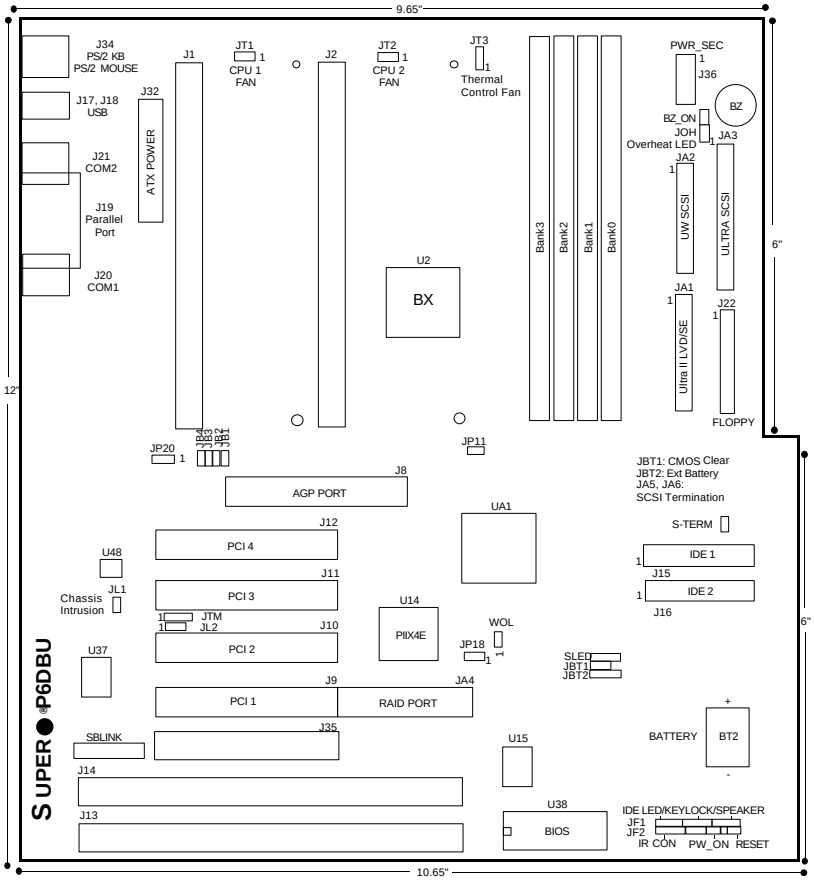
———Pentium II CPU Speed———

	JB1	JB2	JB3	JB4
x3	ON	OFF	ON	ON
x3.5	OFF	OFF	ON	ON
x4	ON	ON	OFF	ON
x4.5	OFF	ON	OFF	ON
x5	ON	OFF	OFF	ON
x5.5	OFF	OFF	OFF	ON
x6	ON	ON	ON	OFF

———————————————

***Note: To Enable Overheat Buzzer place a jumper on BZ_On.**

Figure 1-8. SUPER P6DBE Motherboard Layout



——————— Manufacturer Settings ———————

JBT1: 1-2 (default)
2-3 CMOS Clear
* To clear the CMOS completely, disconnect the power source.

JL1: OFF (default)
ON (intrusion)

JP11: 1-2 Auto
2-3 66 MHz
OFF 100 MHz

JP20: 1-2 PIIX CTL PD State
2-3 BIOS CTL PD State (default)

WOL: Wake-on-LAN

S-TERM: On: SCSI Termination Enable
Off: Termination Disable

————————————————————

————————Pentium II CPU Speed————————

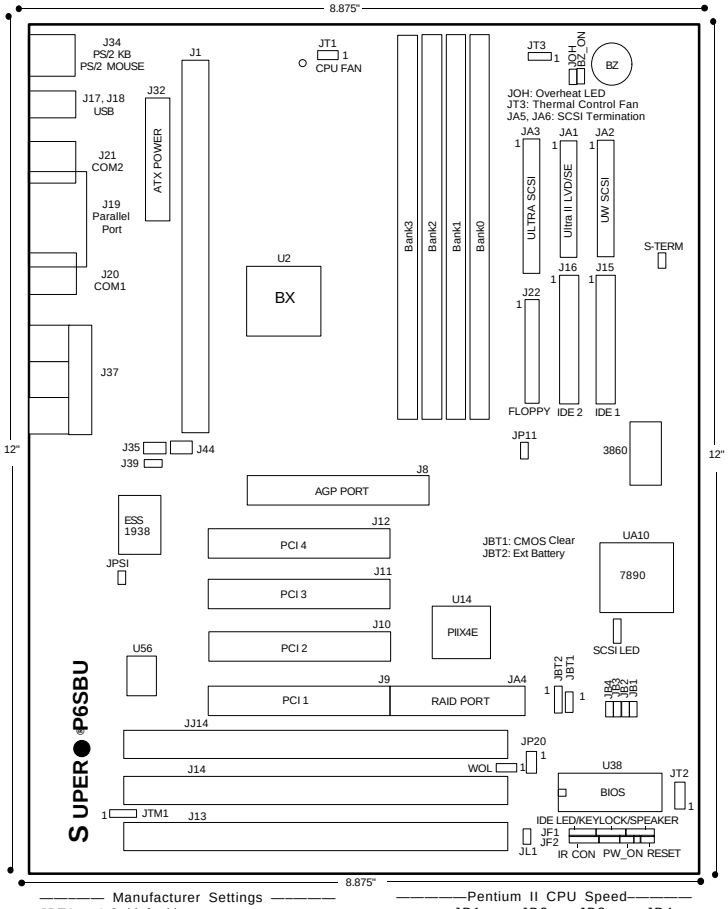
	JB1	JB2	JB3	JB4
x3	ON	OFF	ON	ON
x3.5	OFF	OFF	ON	ON
x4	ON	ON	OFF	ON
x4.5	OFF	ON	OFF	ON
x5	ON	OFF	OFF	ON
x5.5	OFF	OFF	OFF	ON
x6	ON	ON	ON	OFF

————————————————————————————

Note: JA3 is Optional

Note: To Enable Overheat Buzzer place a jumper on BZ_On.

Figure 1-9. SUPER P6DBU Motherboard Layout



———— Manufacturer Settings ————

JBT1: 1-2 (default)
2-3 CMOS Clear
To clear the CMOS completely, disconnect the power source.

JL1: OFF (default)
ON (intrusion)

JP11: 1-2 Auto
2-3 66 MHz
OFF 100 MHz

JP20: 1-2 PIIX CTL PD State
2-3 BIOS CTL PD State (default)

WOL: Wake-on-LAN

S-TERM: On: SCSI Termination Enable
Off: Termination Disable

————————————————

————Pentium II CPU Speed————

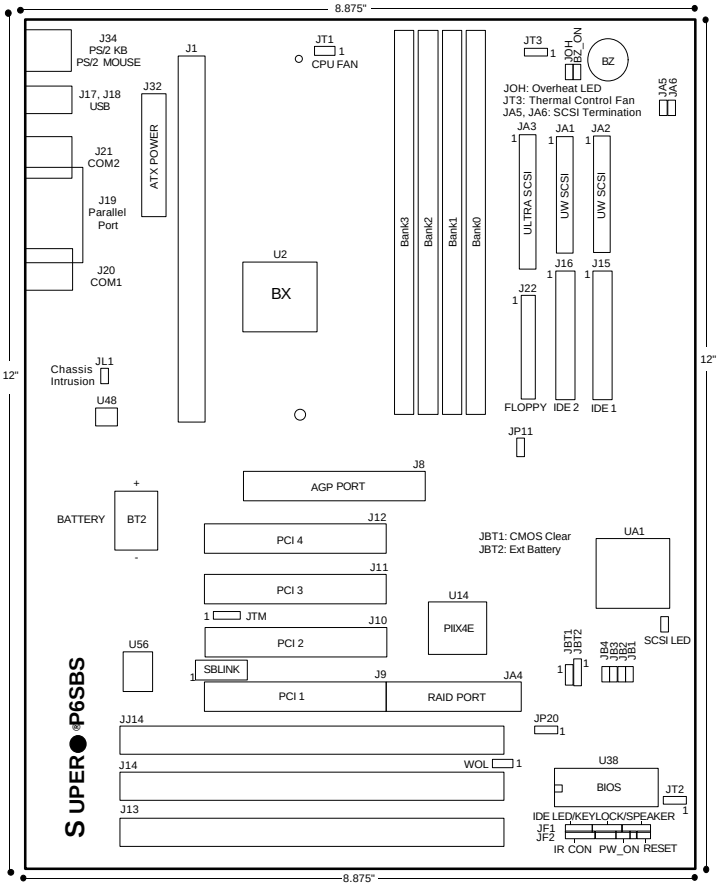
	JB1	JB2	JB3	JB4
x3	ON	OFF	ON	ON
x3.5	OFF	OFF	ON	ON
x4	ON	ON	OFF	ON
x4.5	OFF	ON	OFF	ON
x5	ON	OFF	OFF	ON
x5.5	OFF	OFF	OFF	ON
x6	ON	ON	ON	OFF

————————————————

Note: JA3 is Optional

Note: To Enable Overheat Buzzer place a jumper on BZ_On.

Figure 1-10. SUPER P6SBU Motherboard Layout



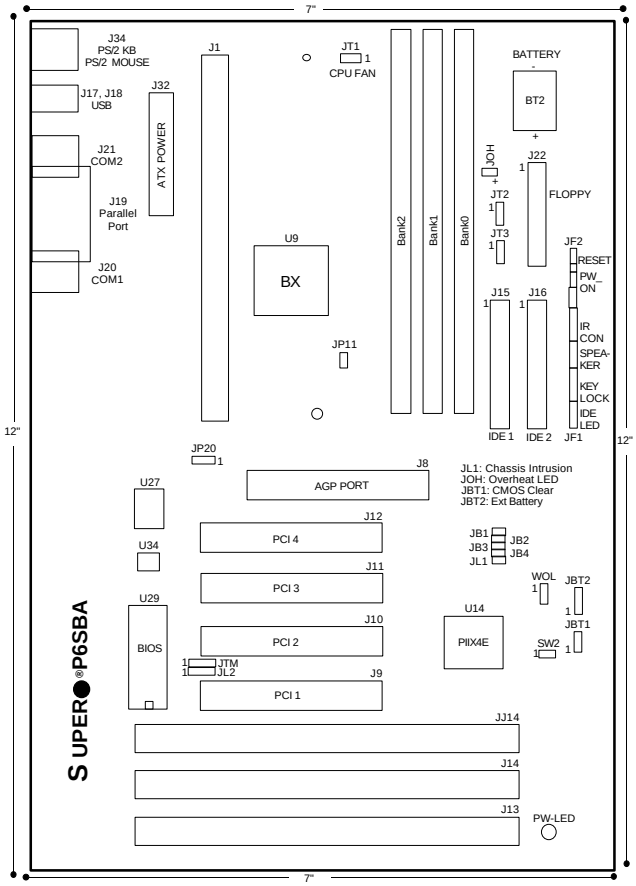
Manufacturer Settings	
JBT1:	1-2 (default)
	2-3 CMOS Clear
	To clear the CMOS completely, disconnect the power source.
JL1:	OFF (default)
	ON (intrusion)
JP11:	1-2 Auto
	2-3 66 MHz
	OFF 100 MHz
JP20:	1-2 PIIX CTL PD State
	2-3 BIOS CTL PD State (default)
WOL:	Wake-on-LAN

Pentium II CPU Speed

	JB1	JB2	JB3	JB4
x3	ON	OFF	ON	ON
x3.5	OFF	OFF	ON	ON
x4	ON	ON	OFF	ON
x4.5	OFF	ON	OFF	ON
x5	ON	OFF	OFF	ON
x5.5	OFF	OFF	OFF	ON
x6	ON	ON	ON	OFF

***Note: To Enable Overheat Buzzer place a jumper on BZ_On.**

Figure 1-11. SUPER P6SBS Motherboard Layout



——— Manufacturer Settings ———

JBT1: 1-2 (default)
2-3 CMOS Clear
To clear the CMOS completely, disconnect the power source.

JL1: OFF (default)
ON (intrusion)

JP11: 1-2 Auto
2-3 66 MHz
OFF 100 MHz

JP20: 1-2 PIIX CTL PD State
2-3 BIOS CTL PD State (default)

WOL: Wake-on-LAN

———Pentium II CPU Speed———

	JB1	JB2	JB3	JB4
x3	ON	OFF	ON	ON
x3.5	OFF	OFF	ON	ON
x4	ON	ON	OFF	ON
x4.5	OFF	ON	OFF	ON
x5	ON	OFF	OFF	ON
x5.5	OFF	OFF	OFF	ON
x6	ON	ON	ON	OFF

Figure 1-12. SUPER P6SBA Motherboard Layout

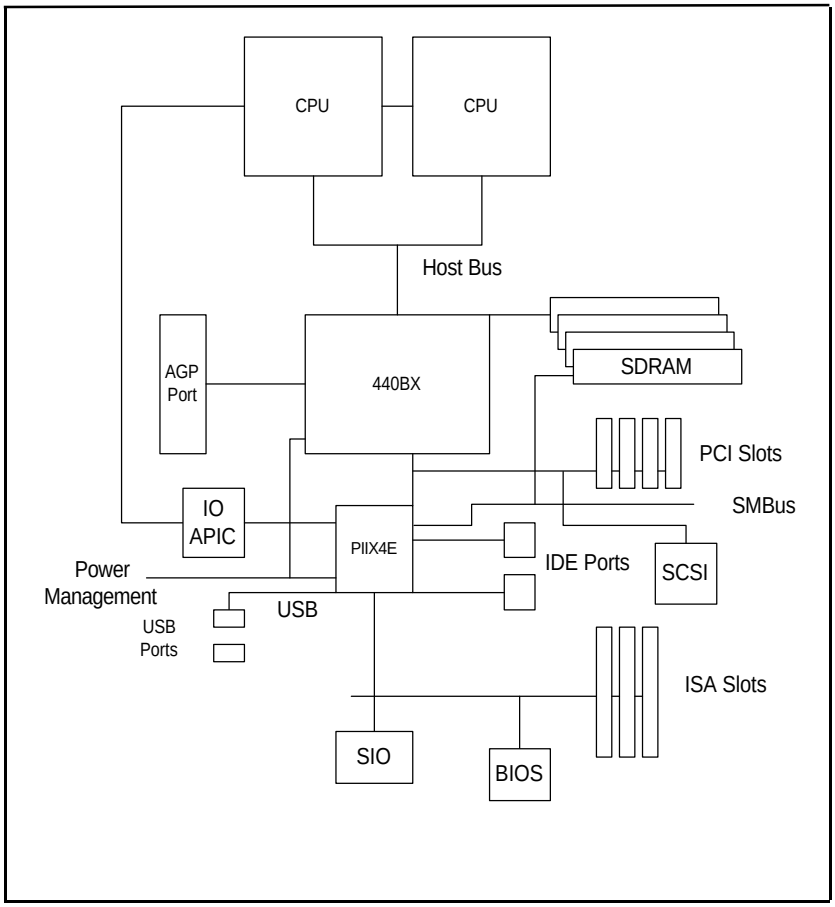


Figure 1-13. 440BX AGP SET:
System Block Diagram (Dual Processors)

Features for P6DBS, P6DBE, P6DBU, P6SBU, P6SBS, and P6SBA Motherboards*

*** Bolded text notes variation in features**.

The following list covers the general features of SUPER P6DBS, P6DBE, P6DBU, P6SBU, P6SBS, and P6SBA.

CPU

- Dual Pentium II processor 233/266/300/333 MHz at 66 MHz bus speed or 350/400 MHz at 100 MHz bus speed (**Note: SUPER P6SBU, P6SBS, and P6SBA support a Single Pentium II processor**.)

Memory

- 1 GB EDO at 66 MHz or 512 MB unbuffered 3.3V SDRAM or 1 GB registered SDRAM (**P6DBS/P6DBE/P6DBU/P6SBU/P6SBS only)**
- 768 MB EDO, 768 MB registered DIMM, 384 MB SDRAM **(P6SBA only**) (**Note: When CPU bus is running at 100 MHz, the SDRAM must be PC-100 compliant DIMMs**) (**Note: The maximum memory cacheability size depends on processor capability**)
- Error Checking and Correction and Error Checking support

Chipset

- Intel 440BX

Expansion Slots

P6DBS/P6SBU/P6SBS/P6SBA	P6DBU/P6DBE
• 4 PCI slots • 3 ISA slots [one PCI/ISA shared slot] • 1 AGP slot	• 5 PCI slots • 2 ISA slots [one PCI/ISA shared slot] • 1 AGP slot

BIOS

- 2 Mb AMI® Flash BIOS
- APM 1.2, DMI 2.01, Plug and Play (PnP)
- Adaptec 7890 SCSI BIOS 2.01 (**P6DBU/P6SBU only**)
- Adaptec 7895 SCSI BIOS (**P6DBS/P6SBS only**)

PC Health Monitoring

- Seven on-board voltage monitors for CPU core(s), CPU I/O, +3.3V, ±5V, and ±12V
- Three fans status monitors with firmware/software control on/off
- Environment temperature monitor and control
- CPU fan auto-off in sleep mode
- Chassis overheat alarm, LED, and control
- Chassis intrusion detection
- System resource alert
- Hardware BIOS virus protection

- Switching voltage regulator for the CPU core
- SUPERMICRO SUPER Doctor and Intel® LANDesk® Client Manager (LDCM) support

ACPI/PC 98 Features

- Microsoft OnNow
- Slow blinking LED for suspend-state indicator
- BIOS support for USB keyboard
- Real time clock wake-up alarm
- Main switch override mechanism
- External modem ring-on

On-Board I/O

- 68-pin 16-bit Ultra II LVD/SE SCSI connectors and 68-pin, 16 bit Ultra Wide SCSI Connector / 50-pin 8-bit Ultra SCSI connector (**P6DBU/P6SBU only**)
- 68-pin 16-bit Dual Ultra-Wide SCSI connectors and 50-pin 8-bit Ultra SCSI connector (**P6DBS/P6SBS only**)
- RAID port for Adaptec ARO-1130xA RAIDport II card (**P6DBS/P6SBS only**)
- RAID port for Adaptec ARO-1130xA-2 RAIDport III card (**P6DBU/P6SBU only**)
- 2 EIDE Bus Master interfaces support Ultra DMA/33 and Mode 4
- 1 floppy port interface
- 2 Fast UART 16550 serial ports
- EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port) parallel port
- PS/2 mouse and PS/2 keyboard
- Infrared port
- 2 USB (Universal Serial Bus) ports
- Solo-1 PCI *Audio*Drive® **(P6SBU only)**

CD Utilities

- Intel LANDesk Client Manager for Windows NT® and Windows® 95 (optional)
- PIIX4 Upgrade Utility for Windows 95
- BIOS Flash Upgrade Utility
- SUPER Doctor Utility
- SCSI Utility, manual and driver

Dimensions

- SUPER P6DBS - ATX (12" x 9.65") * See board diagram for full measurements
- SUPER P6DBE - ATX (12" x 9.6")
- SUPER P6DBU - ATX (12" x 9.65") * See board diagram for full measurements
- SUPER P6SBU - ATX (12" x 8.875")
- SUPER P6SBS - ATX (12" x 8.875")
- SUPER P6SBA - ATX (12" x 7")

1-2 Chipset Overview

The 440BX chipset, developed by Intel, is the ultimate processor platform targeted for 3D graphics and multimedia applications. Along with System-to-PCI bridge integrated with optimized DRAM controller and data path, the chipset introduces the Accelerated Graphics Port (AGP) interface. AGP is a high performance, component level interconnect targeted at 3D applications and is based on a set of performance enhancements to PCI. The I/O subsystem portion of the 440BX platform is based on the PIIX4E, a highly integrated version of Intel's PCI-to-ISA bridge family.

The PCI/AGP and system bus interface controller (82443BX) supports up to two Pentium II processors. It provides an optimized 72-bit DRAM interface (64-bit data plus ECC). This interface supports 3.3V DRAM technologies. The controller provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with the PCI Rev 2.1 Specification. The AGP interface is based on the AGP Specification Rev 1.0. It can support up to 133 MHz (532 MB/s) data transfer rates.

1-3 PC Health Monitoring

This section describes the PC health monitoring features of SUPER P6DBU, P6DBS, P6DBE, P6SBU, P6SBS, and P6SBA. They have an on-board System Hardware Monitor chip which can support PC health monitoring.

Seven On-Board Voltage Monitors for the CPU Core(s), CPU I/O, +3.3V, ±5V, and ±12V

The on-board voltage monitor will scan the seven monitored voltages continuously. Once a voltage becomes unstable, it will report a warning or an error message on the screen. Users can adjust the threshold of the monitored voltage to determine the sensitivity of the voltage monitor.

Three-Fan Status Monitors with Firmware/Software Control On/Off

The PC health monitor can check the RPM status of the cooling fans. The on-board 3-pin CPU fan is controlled by the ACPI BIOS and the ACPI enabled operating system. The thermal fans are controlled by the overheat detection logic.

Environment Temperature Control

The thermal control sensor will monitor the real-time CPU temperature. It will turn on the back-up fan whenever the CPU temperature goes over the user-defined threshold. The overheat circuitry runs independently from the CPU. It can still monitor the overheat condition even if the CPU is in sleep mode. Once it detects that the CPU temperature is too high, it will automatically turn on the back-up fan to prevent any overheat damage to the CPU. The on-board chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature is too high.

CPU Fan Auto-Off in Sleep Mode

The CPU fan will turn on when the power is on. It can be turned off when the CPU is in sleep mode. When the CPU is in sleep mode, it will not run at full power, thereby generating less heat. For power saving purposes, the user has the option to shut down the CPU fan.

CPU Overheat Alarm, LED and Control in P6DBS/P6DBE/ P6DBU/P6SBU/P6SBS

This feature is available when the user enables the CPU overheat warning function in the BIOS. The overheat alarm will activate when the CPU temperature exceeds the temperature configured by the user. When the overheat alarm is activated both the overheat fan and LED are triggered.

Chassis Intrusion Detection

The chassis intrusion circuitry can detect unauthorized intrusion to the system. The chassis intrusion connector is located on JL1. Attach a micro-switch to JL1. When the micro-switch is closed, it means that the chassis has been opened. The circuitry will then alert the user with a warning message when the system is turned on. This feature is available when the user is running Intel's LANDesk Client Manager, and SUPERMICRO's Super Doctor.

System Resource Alert

This feature is available when used with Intel's LANDesk Client Manager. The user can be notified of certain system events. For example, if the system is running low on virtual memory, the hard drive space is not enough to save the data, you are then alerted of the potential problems.

Hardware BIOS Virus Protection

The system BIOS is protected by hardware so that no virus can infect the BIOS area. The user can only change the BIOS content through the flash utility provided by SUPERMICRO. This feature can prevent viruses from infecting the BIOS area and loss of valuable data.

Switching Voltage Regulator for the CPU Core

The switching voltage regulator for the CPU core can support up to 20A current, with auto-sensing voltage ID ranging from 1.8v to 3.5v. This will allow the regulator to run cooler and make the system more stable.

Intel LANDesk® Client Manager (LDCM) Support

As the computer industry grows, PC systems have become more complex and harder to manage. Historically, only experts have been able to fully understand and control these complex systems. Today's users want manageable systems that interact automatically with the user. Client Manager enables both administrators and clients to:

- Review system inventory
- View DMI-compliant component information
- Back-up and restore system configuration files
- Troubleshoot
- Receive notification for system events
- Transfer files to and from client workstations
- Remotely reboot client workstations

1-4 Solo-1™ PCI *Audio*Drive® (Optional for P6SBU)

The Solo-1 PCI *Audio*Drive solution implements a single chip PCI audio solution, providing high-quality audio processing while maintaining full legacy DOS game compatibility. With a dynamic range over 80 dB, the Solo-1 complies with the Microsoft PC 97/PC 98 specifications and meets WHQL audio requirements.

The Solo-1 incorporates a microcontroller, ESFM™ music synthesizer, 3-D stereo effects processor, 16-bit stereo wave ADC and DAC, 16-bit stereo music DAC, MPU-401 UART mode serial port, dual game port, hardware master volume control, a serial port interface to external wavetable music

synthesizer, DMA control logic with FIFO, and PCI bus interface logic. There are three stereo inputs (LINE-IN, LINE-OUT, MIC IN) and a mono microphone input.

1-5 ACPI/PC 98 Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, including hardware, operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives, and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, phones, and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 98 and Windows NT 5.0.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears off and responds immediately to user or other requests.

Slow Blinking LED for Suspend-state Indicator

When the CPU goes into a suspend state, the power LED will start blinking to indicate that the CPU is in suspend mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

BIOS Support for USB Keyboard

If the USB keyboard is the only keyboard in the system, the USB keyboard will work like a normal keyboard during system boot-up.

Real Time Clock Wake-up Alarm

The PC is perceived to be off when not in use, but is still capable of responding to preset wake-up events. In the BIOS the user can set a timer to wake-up the system at a predetermined time.

Main Switch Override Mechanism

When an ATX power supply is used, the power button can function as a system suspend button. When the user presses on the power button, the system will enter a SoftOff state. The monitor will be suspended, and the hard drive will spin down. Pressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required circuitry on the system alive. In case the system malfunctions and you want to turn off the power, just press down on the power button for 4 seconds. The power will turn off and no power is provided to the motherboard.

External Modem Ring-on

Wake-up events can be triggered by a device such as the external modem ringing when the system is in SoftOff state.

1-6 Wake-On-LAN (WOL)

Wake-on-LAN is defined as the ability of a management application to remotely power up a computer which is powered off. Remote PC setup, updates, and asset tracking can occur after hours and on weekends so daily LAN traffic is kept to a minimum and users are not interrupted.

The motherboards have a 3-pin header (WOL) used to connect to the 3-pin header on the Network Interface Card (NIC) which has WOL capability. Note that Wake-On-Lan can only be used with an ATX power connector onboard.

1-7 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for high CPU clock rates like 233, 266, 300, 333, 350 or 400 MHz Pentium II processor.

SUPER P6DBS/P6DBE/P6DBU/P6SBU/P6SBS/P6SBA accommodates ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some power supplies are not adequate.

It is highly recommended that you use a high quality power supply which meets ATX power supply specification 2.01. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to separate noise from the computer. You can also install a power surge protector to help avoid problems caused by power surges.

1-8 Super I/O

The disk drive adapter functions of Super I/O chip include a floppy disk drive controller compatible with the industry standard 82077/765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the Super I/O greatly reduced the number of components required for interfacing with floppy disk drives. The Super I/O supports four 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s.

The Super I/O provides two high speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2 Kbps and also advanced speed with baud rates of 230 K, 460 K, or 921 Kbps which support higher speed modems.

The Super I/O supports one PC-compatible printer port (SPP), Bi-directional Printer Port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Also available, through the printer port interface pins, are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support of legacy and ACPI power management through SMI or SCI function pin. It also has auto power management to reduce power consumption.

The Super I/O complies with **Microsoft PC97 Hardware Design Guide**. IRQs, DMAs, and I/O space resources are flexible to adjust to meet ISA PnP requirement. Moreover, it meets the specification of PC97's requirement in the power management: ACPI and DPM (Device Power Management).

1-9 AIC -7895 MultiChannel™ single-chip UltraSCSI

SUPER P6DBS/P6SBS has an on-board SCSI controller which is 100% compatible with all major operating and hardware platforms. PCI 2.1 and SCAM Level 1 compliance are assured. Two independent UltraSCSI channels provide a per channel data transfer rate of 40 MB/s. Connectors include two 68-pin 16-bit Ultra Wide SCSI connectors (JA1/JA2) and a 50-pin 8-bit Ultra SCSI connector (JA3). You can connect up to 15 devices (seven 8-bit internal and eight 16-bit internal or external SCSI devices, or 15 Wide internal and external SCSI devices).

When Fast SCSI devices are connected, the total length of all cables (internal and external) must not exceed 3 meters (9.8 ft) to ensure reliable operation. If no Fast SCSI devices are connected, the total length of all cables must not exceed 6 meters (19.7 ft).

AIC-7895 consolidates the functions of two SCSI chips, eliminating the need for a PCI bridge. Reducing PCI bus loading enables system capabilities to be expanded with additional PCI devices.

The AIC-7895 functions with **Adaptec RAIDport II (ARO-1130xA)** to deliver RAID functionality.

1-10 AIC -7890 Ultra II SCSI

Note: If you are using a low voltage differential Hard Drive, it is recommended you use LVD/SE Ultra II SCSI cable. LVD/SE cable offers increased length, and can accommodate more devices.

SUPER P6DBU/P6SBU has an on-board SCSI controller which is 100% compatible with all major operating and hardware platforms. The AIC-7890 controller provides advanced PCI-to-SCSI Ultra2 SCSI host adapter features in a 272-pin Ball Grid Array (BGA) package, as well as containing an integrated dual mode (LVD/SE) transceiver. The AIC-7890 Ultra2 SCSI chip connects to a 32-bit PCI bus. It is PCI 2.1 compliant, and fully supports the power management requirements specified in Microsoft's PC 97 guidelines and it provides SCAM level 2 support. The AIC-7890 functions with **Adaptec RAIDport III (ARO-1130xA-2)** to deliver RAID functionality.

The AIC-7890 Ultra2 SCSI controller, used together with the AIC-3860 transceiver, allows Ultra2 and single-ended devices to operate together on the same SCSI bus without inpacting Ultra2 performance and cable lengths. The AIC-7890 controller can support external High Voltage Differential (HVD) transceivers only for Ultra data rates.

1-11 Warranty, Technical Support, and Service

The manufacturer will repair or exchange any unit or parts free of charge due to manufacturing defects for two years (24 months) from the original invoice date of purchase.

Warranty Terms and Conditions

Super Micro Computer, Inc. warrants its products to be free from defects in material and workmanship. The warranty period is two years (24 months) beginning from the original purchase date. Super Micro shall, at our option and cost, repair or replace the defective product if the product is returned within the applicable warranty period and if the product is found by Super Micro to be defective within the terms of this warranty. Before presenting any motherboard for warranty service, the customer must first remove the CPU(s), memory, or other peripherals.

This warranty shall not apply to any failure or defect caused by misuse, abnormal or unusually heavy use, neglect, abuse, alteration, improper installation, unauthorized repair or modification, improper testing, accident or causes external to the product such as, but not limited to, excessive heat or humidity, power failure, power surges, or acts of God/Nature. Super Micro makes no warranty with respect to (i) expendable components, (ii) any software products supplied by us, (iii) any experimental or developmental products, and (iv) products not manufactured by us; all of which components, software and products are provided "AS-IS."

This warranty is in lieu of any other warranty expressed or implied. In no event will Super Micro be held liable for incidental or consequential damages, such as loss of revenue or loss of business arising from the purchase of Super Micro products.

Returns

If you must return products for any reason, refer to Chapter 3 in this manual, “Returning Merchandise for Service.”

Chapter 2
Installation

2-1 Static-Sensitive Devices

Static-sensitive electric discharge can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge.

Precautions

- Use a grounded wrist strap designed for static discharge.
- Touch a grounded metal object before you remove the board from the anti-static bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules, or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the system board and peripherals back into their anti-static bags when not in use.
- Be sure your computer system's chassis allows excellent conductive contacts between its power supply, case, mounting fasteners, and the system board for grounding purposes.

Unpacking

The system board is shipped in anti-static packaging to avoid static damage. When unpacking the board, be sure the person handling the board is static-protected.

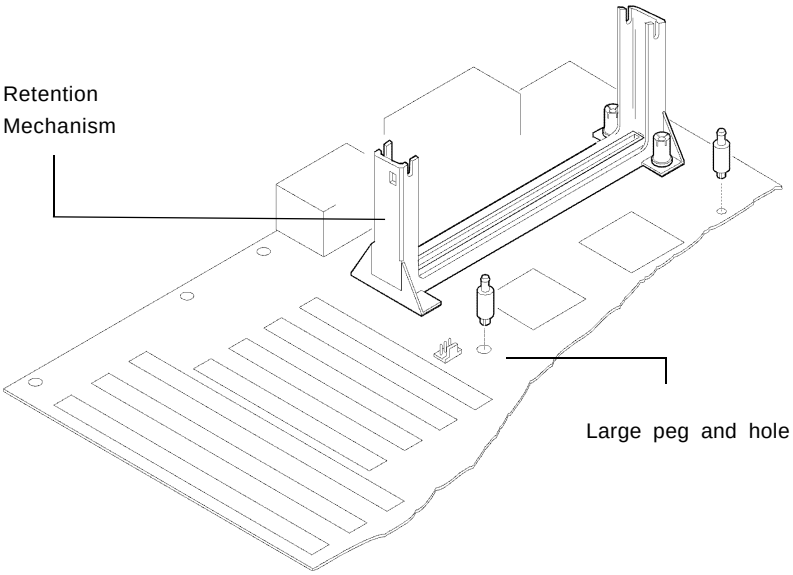
2-2 Pentium II Processor Installation

When handling the Pentium II processor, avoid placing direct pressure on the label area of the fan.

1. Check the Intel boxed processor kit for the following items: the processor with the fan heatsink attached, two black plastic pegs, two black plastic supports, and one power cable.

2. Install the retention mechanism attach mount under the motherboard. Do this before mounting the motherboard into the chassis. Do not screw too tightly. Mount the two black plastic pegs onto the motherboard (Figure 2.1). These pegs will be used to attach the fan heatsink supports. Notice that one hole and the base of one peg are larger than the other hole and peg base. Push each peg into its hole firmly until you hear it "click" into place.

Figure 2-1. Mounting the Pegs



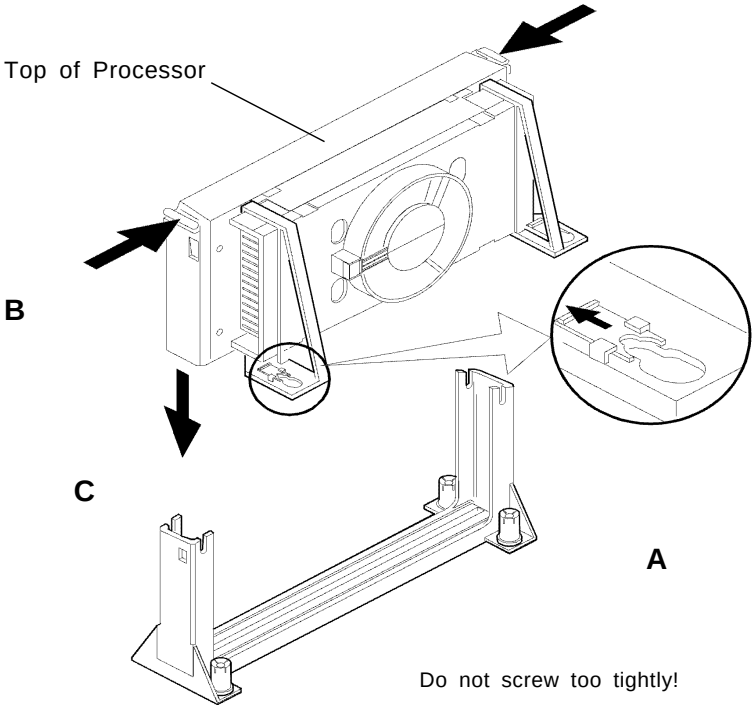
3. Slide a black plastic support onto each end of the fan heatsink, making sure that the hole and clip are on the outside edge of the support. If the supports are reversed, the holes will not line up with the pegs on the motherboard. Slide each support toward the center of the processor until the support is seated in the outside groove in the fan housing.

4. Slide the clip (A) on each support toward the processor, exposing the hole that will fit over the peg on the motherboard. Push the latches (B) on the processor toward the center of the processor until they click into place.

5. Hold the processor so that the fan shroud is facing toward the pegs on the motherboard. Slide the processor (C in Figure 2-2) into the retention mechanism and slide the supports onto the pegs. Ensure that the pegs on the motherboard slide into the holes in the heatsink support and that the

alignment notch in the SEC cartridge fits over the plug in Slot 1. Push the processor down firmly, with even pressure on both sides of the top, until it is seated.

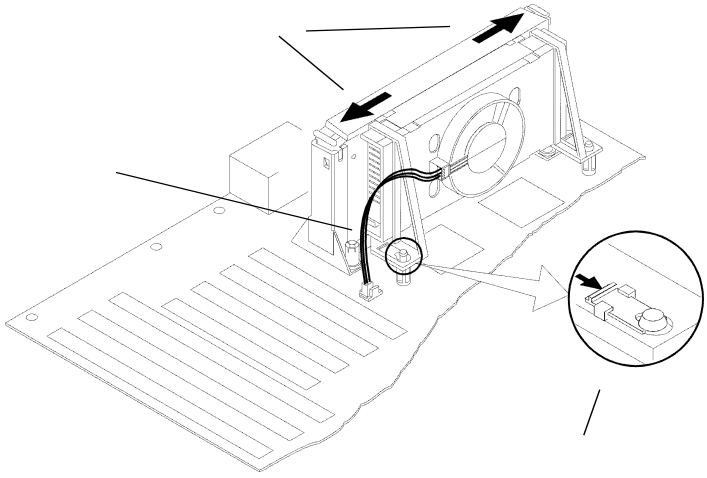
Figure 2-2. Retention Mechanism



6. Slide the clips on the supports (A) forward until they click into place to hold the pegs securely. Apply slight pressure on the peg and push the peg toward the clip while pushing the clip forward. Push the latches on the processor (B) outward until they click into place in the retention mechanism. The latches must be secured for proper electrical connection of the processor.

7. Attach the small end of the power cable (C in Figure 2-3) to the three-pin connector on the processor, then attach the large end to the three-pin connector on the motherboard.

Figure 2-3. Attaching the Fan Power Cable



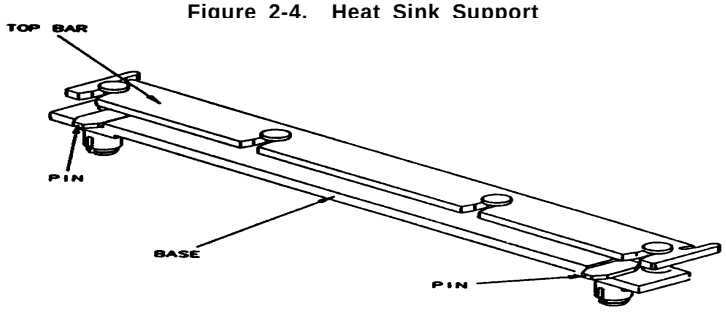
OEM Pentium II and Heat Sink Support

The heat sink support consists of a top bar, a base bar, four posts on the top bar and two posts on the base bar. The two posts on the base snap into the motherboard. Install the two pins into the base bar. Insert the Pentium II with the heat sink on it into Slot 1. Install the top support bar. The four top posts should be close to Slot 1. The bottom most row of fins in the heat sink should fit between the top support bar and the bottom support bar as shown in Figure 2-4.

Removing the Pentium II Processor

To remove the Pentium II processor from the motherboard, follow the reverse of the installation process. Note: **Do not reuse the pegs**.

Figure 2-4. Heat Sink Support



When removing the Pentium II processor, avoid pressing down on the motherboard or components. Instead, press down on the plastic connectors.

2-3 Installation of the Universal Retention Mechanism (URM)*

Please Note! Screws and washers attach from the bottom of the board and must be installed before mounting the board to the chassis. *(See figures 2-5 and 2-6)*

1. When Installing the URM be sure ***Left*** (L) and ***Right*** (R) sides are placed accordingly.

2. Lift arms upright and slide processor into socket, noting that notches need to line up.

*These directions may not apply to second source URMs

2-4 Special Instructions for the Celeron Processor

Please Note! The Celeron Processor requires special caps to hold it in place (caps are bundled with the motherboard). *(See figures 2-5 and 2-6)*

1. Lift URM's arms to upright position.

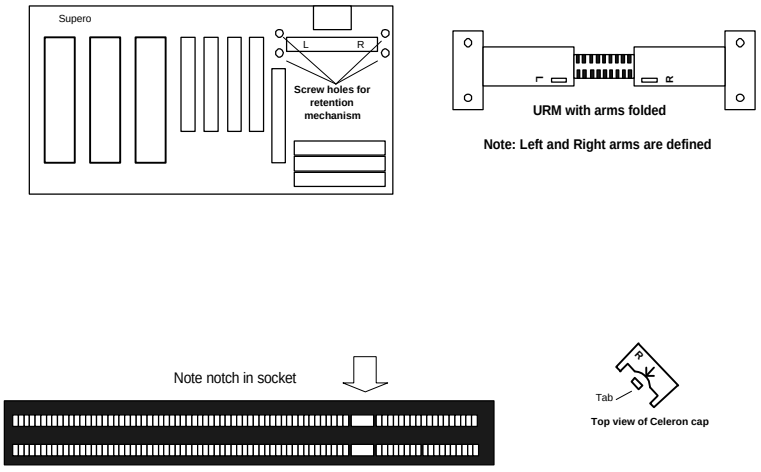
2. Slide Celeron into the socket, noting that notches need to line up.

3. Slide the special Celeron caps over the ends of the retention arms. Make sure the arrows face outward and that the ***Left*** (L) and ***Right*** (R) cap are on the appropriate sides of the URM. Caps should snap into place.

4. To remove caps, pull out on the tab (arrows points to tab), then pull up.

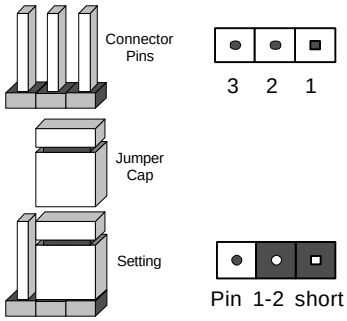
Figure 2-5. Installing the Celeron Processor

Figure 2-6. URM and Celeron Installation



2-5 Explanation and Diagram of Jumper/ Connector

To modify the operation of the motherboard, jumpers can be used to choose settings. Jumpers create shorts between two pins and change the function of the connector. Pin 1 is identified with a square.



2-6 Changing the CPU Speed

To change the CPU speed for a Pentium II processor, change the jumpers shown on Table 2-1. The example on the right will show you which CPU Core/Bus Ratio to use. The general rule is to divide the CPU speed by the bus speed (100 MHz). If you have a 400 MHz CPU, dividing it by 100 will give you a CPU Core/BUS Ratio of 4.0. After determining the CPU Core/Bus Ratio, refer to Table 2-1 for settings of JB1, JB2, JB3 and JB4.

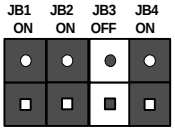
Table 2-1
Pentium II Speed Selection

CPU Core/ Bus Ratio	JB1	JB2	JB3	JB4
3.0	ON	OFF	ON	ON
3.5	OFF	OFF	ON	ON
4.0	ON	ON	OFF	ON
4.5	OFF	ON	OFF	ON
5.0	ON	OFF	OFF	ON
5.5	OFF	OFF	OFF	ON
6.0	ON	ON	ON	OFF

400 MHz = 100 MHz x 4.0

CPU Speed = Bus Freq. x Ratio

Example of 4.0
CPU Core/Bus Ratio



Note: SUPER P6DBU/P6SBU must be running at 100 MHz bus speed to support Pentium II 350/400 MHz processors.

2-7 Mounting the Motherboard in the Chassis

All the motherboards have standard mounting holes to fit different types of chassis. Chassis may come with a variety of mounting fasteners, made of metal or plastic. Although a chassis may have both metal and plastic fasteners, metal fasteners are the most highly recommended because they ground the system board to the chassis. Therefore, use as many metal fasteners as possible for better grounding.

2-8 Connecting Cables

Power Supply Connector

After you have securely mounted the motherboard to the chassis, you are ready to connect the cables. Attach power supply cables to J32 for an ATX power supply. See Table 2-2 for pin definitions of an ATX power supply.

Table 2-2
ATX Power Supply Connector
Pin Definitions for J32

Pin Number	Definition	Pin Number	Definition
1	3.3V	11	3.3V
2	3.3V3	12	-12V
3	Ground	13	Ground
4	5V	14	PS-ON
5	Ground	15	Ground
6	5V	16	Ground
7	Ground	17	Ground
8	PW-OK	18	-5V
9	5VSB	19	5V
10	12V	20	5V

Secondary Power Connector

The Secondary Power Connector is recommended when a heavy load of peripherals have been connected to the motherboard. ***Note: Be sure to use a 1 X 6 pin connector and check the power supply layout before attaching it.*** The Secondary Power Connector is located on J36. See Table 2-3 for pin definitions.

Table 2-3
Secondary Power Connector
J36

Pin Number	Definition
1	Ground
2	Ground
3	Ground
4	+3.3V
5	+3.3V
6	+5V (keyed)

*P6DBE/P6DBS/P6DBU only

Infrared Connector

The infrared connector is located on pins 1-8 of JF2. See Table 2-4 for pin definitions.

Table 2-4
Infrared Pin
Definitions
for JF2

Pin Number	Definition
1	+5V
2	Key
3	IRRX
4	Ground
5	IRTX
6	NC
7	NC
8	NC

PW_ON Connector

The PW_ON connector is located on pins 9 and 10 of JF2. Momentarily contacting both pins will power on/off the system. The user can also configure this button to function as a suspend button. (See BIOS setup information on page 5-13). To turn off the power when set to suspend mode, hold down the power button for at least 4 seconds. See Table 2-5 for pin definitions.

Table 2-5
PW-ON Connector
Pin Definitions
for JF2

Pin Number	Definition
9	PW_ON
10	Ground

Reset Connector

The reset connector is located on pins 12 and 13 of JF2. This connector attaches to the hardware Reset switch on the computer case. See Table 2-6 for pin definitions.

Table 2-6
Reset Pin
Definitions
for JF2

Pin Number	Definition
12	Ground
13	Reset

Hard Drive LED

The hard drive LED is located on pins 1 to 4 of JF1. Attach the hard drive LED cable onto pins 1 and 2. See Table 2-7 for pin definitions.

Table 2-7
Hard Drive LED Pin
Definitions
for JF1

Pin Number	Definition
1	+5V
2	HD Active
3	HD Active
4	+5V

Keylock/Power LED Connector

The keylock/power LED connector is located on pins 5 to 9 of JF1. See Table 2-8 for pin definitions. Pins 5 and 7 are for the power LED. Pins 8 and 9 are for the keylock.

Table 2-8
Keylock/Power LED Pin Definition
for JF1

Pin Number	Function	Definition
5	VCC +5V	Red wire, LED power
6	VCC +5V	Red wire, LED power
7	Ground	LED control
8		Keyboard inhibit
9	Ground	Black wire

Speaker Connector

The speaker connector is located on pins 10 to 13 of JF1. See Table 2-9 for pin definitions.

Table 2-9
Speaker Connector Pin Definitions for JF1

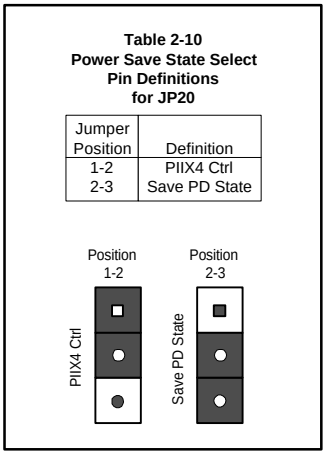
Pin Number	Function	Definition
10	+	Red wire, Speaker data
11	Key	No connection
12		Key
13		Speaker data

Power Save State Select

Refer to Table 2-10 to set JP20. Power Save State Select is used when you want the system to be in power off state the first time you apply power to the system or when the system comes back from AC power failure. In this state, the power will not come on unless you hit the power switch on the motherboard. PIIX4 control is used if you want the system to be in power on state the first time you apply power to the system or when the system comes back from AC power failure.

Table 2-10
Power Save State Select Pin Definitions for JP20

Jumper Position	Definition
1-2	PIIX4 Ctrl
2-3	Save PD State



ATX PS/2 Keyboard and PS/2 Mouse Ports

The ATX PS/2 keyboard and the PS/2 mouse are located on J34. See Table 2-11 for pin definitions.

Table 2-11
ATX PS/2 Keyboard and PS/2 Mouse Ports Pin Definitions for J34

Pin Number	Definition
1	Data
2	NC
3	Ground
4	VCC
5	Clock
6	NC

Universal Serial Bus

The two Universal Serial Bus connectors are located on J17 and J18. See Table 2-12 for pin definitions.

Table 2-12
Universal Serial Bus Pin Definitions

J17		J18	
Pin Number	Definition	Pin Number	Definition
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	Ground	4	Ground
5	N/A	5	Key

ATX Serial Ports

ATX serial port COM1 is located on J20 and serial port COM2 is located on J21. See Table 2-13 for pin definitions.

Table 2-13
ATX Serial Ports Pin Definitions

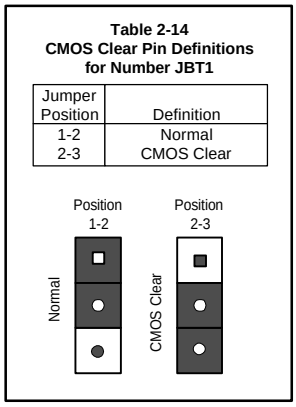
J20		J21	
Pin Number	Definition	Pin Number	Definition
1	DCD	6	CTS
2	DSR	7	DTR
3	Serial In	8	RI
4	RTS	9	Ground
5	Serial Out	10	NC

CMOS Clear

Refer to Table 2-14 for instructions on how to clear the CMOS. **For ATX power supply, you need to completely shut down the system, then use JBT1 to clear the CMOS.** Do not use the PW_ON connector to clear the CMOS. A second way of resetting the CMOS contents is by pressing the <ins> key, then turning on the system power. Release the key when the power comes on.

Table 2-14
CMOS Clear Pin Definitions for Number JBT1

Jumper Position	Definition
1-2	Normal
2-3	CMOS Clear



External Battery

Connect an external battery to JBT2. Refer to Table 2-15 for pin definitions.

Table 2-15
External Battery Pin Definitions for JBT2

Pin Number	Definition
1	+3V
2	NC
3	NC
4	Ground

Wake-on-LAN

The Wake-on-LAN connector is located on WOL. Refer to Table 2-16 for pin definitions.

Table 2-16
Wake-on-LAN Pin Definition located at WOL

Pin Number	Definition
1	+5V Standby
2	Ground
3	Wake up

Fan Connectors*

The thermal/overheat fan is located on JT3. The CPU fans are located on JT1 and JT2. Refer to Table 2-17 for pin definitions.

Table 2-17
Fan Connectors Pin Definitions for JT1, JT2, JT3

Pin Number	Definition
1	Ground (black)
2	+12V (red)
3	Tachometer

* Caution: These fan connectors are DC direct.

Chassis Intrusion

The Chassis Intrusion Detector is located on JL1. See chapter one, board layouts, and PC Health Monitor page 1-18 for more information. See Table 2-18 for pin definitions.

Table 2-18
Chassis Intrusion Detector Settings on JL1

Pin Number	Definition
1	Intrusion Input
2	Ground

Open = Default, Close = Intrusion

2-9 Installing the DIM Modules

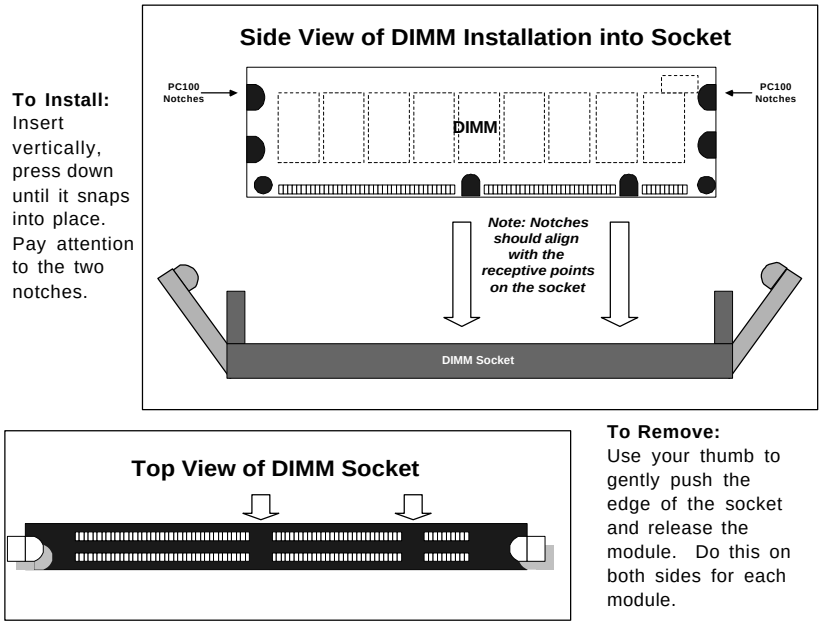
CAUTION

Exercise extreme care when installing or removing the DIM modules to prevent any possible damages.

DIM Module Installation

1. Insert DIM modules in Bank 0 through Bank 3 as required for the desired system memory.
2. Insert each DIM module vertically into its socket. Pay attention to the two notches to prevent inserting the DIMM at a wrong position. The component side of the DIM module must face the CPU socket. The prior statement is applicable for DIMMs with components on one side only.
3. Gently press the DIM module until it snaps upright into place in the socket.

4. For best results, install DIMM starting from bank 0 (the DIMM socket farthest from BX chip)



To Install: Insert vertically, press down until it snaps into place. Pay attention to the two notches.

To Remove: Use your thumb to gently push the edge of the socket and release the module. Do this on both sides for each module.

Figure 2-7. Installing the DIMM

2-10 Connecting Parallel, Floppy and Hard Disk Drives

Use the following information to connect the floppy and hard disk drive cables.

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have the twisted wires always connects to drive B.
- An IDE hard disk drive requires a data ribbon cable with 40 wires, and a SCSI hard disk drive requires a SCSI ribbon cable with 50 wires. A wide SCSI hard disk drive requires a SCSI ribbon cable with 68 wires.
- A single IDE hard disk drive cable has two connectors to provide for two drives. To select an IDE disk drive as C, you would normally set the drive select jumper on the drive to DS1 (or Master). To select an IDE disk drive as D, you would normally set the drive select jumper on the drive to DS2 (or Slave). Consult the documentation that came with your disk drive for details on actual jumper locations and settings.
- A single SCSI ribbon cable typically has three connectors to provide for

two hard disk drives and the SCSI adapter. (Note: most SCSI hard drives are single-ended SCSI devices.) The SCSI ID is determined by jumpers or a switch on the SCSI device. The last internal (and external) SCSI device cabled to the SCSI adapter must be terminated.

Table 2-19
Parallel Port Pin Definitions for Connector J19

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACK	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT	26	NC

Parallel Port Connector

The parallel port is located on J19. See Table 2-19 for pin definitions.

Floppy Connector

The floppy connector is located on J22. See Table 2-20 for pin definitions.

Table 2-20
Floppy Connector Pin Definitions for J22

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette

Table 2-21
IDE Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

IDE Interfaces

There are no jumpers to configure the on-board IDE interfaces J15 and J16. Refer to Table 2-21 for the pin definitions.

SCSI Connectors

There are no jumpers to configure the on-board Single End SCSI interface. Refer to Table 2-22 for pin definitions. Refer to Table 2-23 for the pin definitions for Wide SCSI pin definitions.

Table 2-22
68-pin Single End SCSI Connector Pin

Pin Number	Function	Pin Number	Function
1	GND	35	-DB (12)
2	GND	36	-DB (13)
3	GND	37	-DB (14)
4	GND	38	-DB (15)
5	GND	39	Parity H
6	GND	40	-DB (0)
7	GND	41	-DB (1)
8	GND	42	-DB (2)
9	GND	43	-DB (3)
10	GND	44	-DB (4)
11	GND	45	-DB (5)
12	GND	46	-DB (6)
13	GND	47	-DB (7)
14	GND	48	Parity L
15	GND	49	GND
16	GND	50	Termpwrd
17	Termpwrd	51	Termpwrd
18	Termpwrd	52	Termpwrd
19	GND	53	NC
20	GND	54	GND
21	GND	55	-ATTN
22	GND	56	GND
23	GND	57	-BSY
24	GND	58	-ACK
25	GND	59	-RST
26	GND	60	-MSG
27	GND	61	-SEL
28	GND	62	-CD
29	GND	63	-REQ
30	GND	64	-IO
31	GND	65	-DB (8)
32	GND	66	-DB (9)
33	GND	67	-DB (10)
34	GND	68	-DB (11)

Table 2-23
50-pin Wide SCSI Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	GND	26	-DB (0)
2	GND	27	-DB (1)
3	GND	28	-DB (2)
4	GND	29	-DB (3)
5	GND	30	-DB (4)
6	GND	31	-DB (5)
7	GND	32	-DB (6)
8	GND	33	-DB (7)
9	GND	34	-DB (P)
10	GND	35	GND
11	GND	36	GND
12	Reserved	37	Reserved
13	Open	38	Termpwr
14	Reserved	39	Reserved
15	GND	40	GND
16	GND	41	-ATN
17	GND	42	GND
18	GND	43	-BSY
19	GND	44	-ACK
20	GND	45	-RST
21	GND	46	-MSG
22	GND	47	-SEL
23	GND	48	-C/D
24	GND	49	-REQ
25	GND	50	-I/O

Table 2-24
SCSI LVD 68-pin Connector

Connector Contact Number	Signal Names	Connector Contact Number	Signal Names
1	+DB(12)	35	-DB(12)
2	+DB(13)	36	-DB(13)
3	+DB(14)	37	-DB(14)
4	+DB(15)	38	-DB(15)
5	+DB(P1)	39	-DB(P1)
6	+DB(0)	40	-DB(0)
7	+DB(1)	41	-DB(1)
8	+DB(2)	42	-DB(2)
9	+DB(3)	43	-DB(3)
10	+DB(4)	44	-DB(4)
11	+DB(5)	45	-DB(5)
12	+DB(6)	46	-DB(6)
13	+DB(7)	47	-DB(7)
14	+DB(P)	48	-DB(P)
15	GROUND	49	GROUND
16	DIFFSENS	50	GROUND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RESERVED	53	RESERVED
20	GROUND	54	GROUND
21	+ATN	55	-ATN
22	GROUND	56	GROUND
23	+BSY	57	-BSY
24	+ACK	58	-ACK
25	+RST	59	-RST
26	+MSG	60	-MSG
27	+SEL	61	-SEL
28	+C/D	62	-C/D
29	+REQ	63	-REQ
30	+I/O	64	-I/O
31	+DB(8)	65	-DB(8)
32	+DB(9)	66	-DB(9)
33	+DB(10)	67	-DB(10)
34	+DB(11)	68	-DB(11)

SCSI LVD 68-pin Connector

Refer to Table 2-24 for the pin definitions.

Table 2-25
AGP Port Pin Definitions for J8

Pin #	B	A	Pin #	B	A
1	Spare	12V	34	Vddq3.3	Vddq3.3
2	5.0V	Spare	35	AD21	AD22
3	5.0V	Reserved*	36	AD19	AD20
4	USB+	USB-	37	GND	GND
5	GND	GND	38	AD17	AD18
6	INTB#	INTA#	39	C/BE2#	AD16
7	CLK	RST#	40	Vddq3.3	Vddq3.3
8	REQ#	GNT#	41	IRDY#	Frame#
9	VCC3.3	VCC3.3	42		
10	ST0	ST1	43	GND	GND
11	ST2	Reserved	44		
12	RBF#	PIPE#	45	VCC3.3	VCC3.3
13	GND	GND	46	DEVSEL#	TRDY#
14	Spare	Spare	47	Vddq3.3	STOP#
15	SBA0	SBA1	48	PERR#	Spare
16	VCC3.3	VCC3.3	49	GND	GND
17	SBA2	SBA3	50	SERR#	PAR
18	SB_STB	Reserved	51	C/BE1#	AD15
19	GND	GND	52	Vddq3.3	Vddq3.3
20	SBA4	SBA5	53	AD14	AD13
21	SBA6	SBA7	54	AD12	AD11
22	KEY	KEY	55	GND	GND
23	KEY	KEY	56	AD10	AD9
24	KEY	KEY	57	AD8	C/BE0#
25	KEY	KEY	58	Vddq3.3	Vddq3.3
26	AD31	AD30	59	AD_STB0	Reserved
27	AD29	AD28	60	AD7	AD6
28	VCC3.3	VCC3.3	61	GND	GND
29	AD27	AD26	62	AD5	AD4
30	AD25	AD24	63	AD3	AD2
31	GND	GND	64	Vddq3.3	Vddq3.3
32	AD_STB1	Reserved	65	AD1	AD0
33	AD23	C/BE3#	66	SMB0	SMB1

AGP Port

There are no jumpers to configure the AGP port J8. Refer to Table 2-25 for the pin definitions.

Chapter 3
Troubleshooting

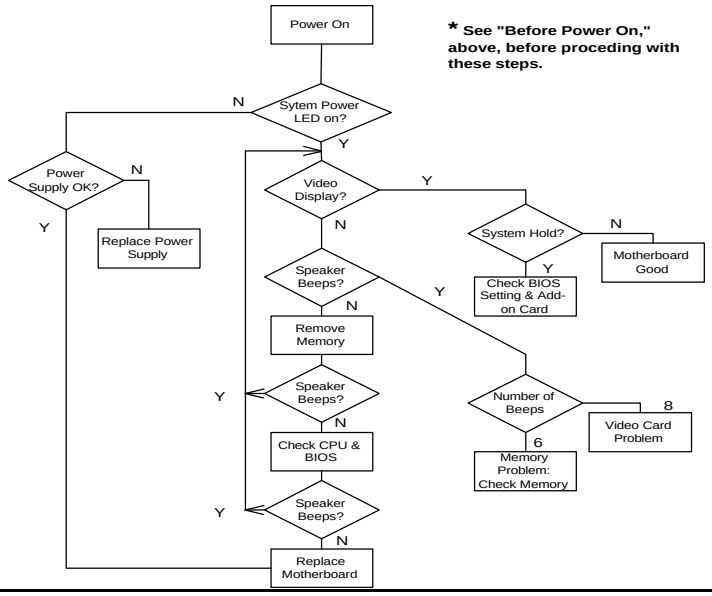
3-1 Troubleshooting Procedures

Use the following procedures and chart to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

Before Power On

1. Make sure there is no short circuit between motherboard and chassis.
2. Disconnect all ribbon/wire cables from the motherboard.
3. Remove all the add-in cards except the video graphics card. (Be sure the video/graphic card is inserted properly.)
4. Install a CPU, a chassis speaker and power LED to this motherboard. (Check all the jumper settings as well)
5. Install one bank of memory module.
6. Check power supply voltage monitor 115 V / 230 V switch.

Figure 3-1. Troubleshooting Flowchart



No Power

1. Make sure the default jumper is on and CPU is correctly setup.
2. Turn power switch on and off to test system.
3. If power is still not on, turn off system power to move jumper setting on JP20 from 2-3 to 1-2.
4. If moving jumper setting has not helped: Clear CMOS.
5. Check power supply voltage monitor. (Check power supply 115 V / 230 V switch)

No Video

Use the following steps for troubleshooting your system configuration.

1. If the power is on but you have no video, remove all the add-in cards and cables.
2. Check for shorted connections, especially under the motherboard.
3. Check the jumpers settings, clock speed, and voltage settings.
4. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details about beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended for port 80h codes. Refer to Appendix B.

Memory Error

If you encounter memory error, follow the procedures below.

1. Check to determine if DIM modules are improperly installed.
2. Make sure that different types of DIMMs have not been installed in different banks (e.g., a mixture of 2MB x 36 and 1 MB x 36 DIMMs in Banks 0).
3. Determine if different speeds of DIMMs have been installed, and the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for DIMMs in the system.
4. Check for bad DIM modules or chips.
5. Try to install the minimum memory first (single bank).

Losing the System's Setup Configuration

1. Check the jumper JBT1 setting. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose CMOS setup. Refer to Chapter 1 of this manual for details.
2. If the above step does not fix the Setup Configuration problem, contact your vendor for repair.

3-2 Technical Support Procedures

1. Please go through the 'Troubleshooting Procedures' and 'Frequently Asked Question' (FAQ) sections in this chapter of the manual or check our web site FAQ (http:// www.supermicro.com) before contacting Technical Support.
2. Take note that as a motherboard manufacturer Super Micro does not sell directly to end-users, so it is best to check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.
3. BIOS upgrades can be downloaded from the SUPER BBS# (408) 895-2022, 24 hours a day, using 1200-28800 baud, 8 data bits, 1 stop bit and no parity. BIOS upgrades can also be downloaded from our web site at http://www.supermicro.com.

Note: Not all BIOS can be flashed depending on the modifications to the boot block code.

4. If you still cannot resolve the problem, include the following information when you e-mail Super Micro for technical support:
   - BIOS release date/version
   - System board serial number
   - Product model name
   - Invoice number and date
   - System configuration

   Due to the volume of e-mails we recieve and the time it takes to replicate problems, a response to your question may not be immediately available. Please understand that we do not have the resources to serve every end-user, however we will try our best to help all our customers.
5. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department.

3-3 Frequently Asked Questions

Question: What are the differences between the various memories that the 440BX motherboard can support?

Answer: The 440BX integrates a main memory DRAM controller that supports a 64-bit or 72-bit (64 bit memory data plus 8 ECC bits.) DRAM from 8 MB to 512 MB for SDRAM and from 8 MB to 1 GB for EDO or registered DIMM. The DRAM types supported are either Extended Data Out (EDO), Synchronous DRAM (SDRAM) or Registered DIM modules. ***Note: EDO DIM Modules are not recommended for running 100 MHz bus speed**.

1. Mixing ECC and non-ECC will result in non-ECC operation.

EC/ECC is supported properly in the 440BX, only if all the memory are 72 bit wide. A system with a mixture of 64 and 72-bit wide memory will disable ECC mode.

2. EDO memory and SDRAM cannot be mixed.

3. Registered SDRAM and unbuffered SDRAM cannot be mixed.

4. Mixing PC/100 DIMM and PC/66 DIMM will result in an unexpected memory count or system errors.

5. User should populate the DIMM starting with the DIMM socket located the furthest from the BX chip (U2 on P6DBS/P6DBE/P6SBS, U4 on P6DBU/P6SBU or U9 on P6SBA).

6. If EDO memory is used, the CPU bus should be set at 66 MHz Bus speed only.

Question: How do I update my BIOS?

Answer: Update BIOS files are located on our web site at http://www.supermicro.com. Please check the current BIOS revision and make sure it is newer than your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer. Unzip the BIOS update file and you will find three files: readme.txt (flash instructions), sm2flash.com (BIOS flash utility), and the BIOS image file (xxxxxx.rom). Copy these files onto a bootable floppy and reboot your system. It is not necessary to set BIOS boot block protection jumpers on the motherboard.

At the DOS prompt, enter the command "sm2flash." This will start the flash utility and give you an opportunity to save your current BIOS image. Flash the boot block and enter the name of the update BIOS image file. NOTE: It is important to save your current BIOS and rename it "super.rom" in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select "Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS, please clear the CMOS then load Optimal Values in the BIOS.

Question: **After flashing the BIOS my system does not have video. How can I correct this?**

Answer: If the system does not have video after flashing your new BIOS, it indicates the flashing procedure failed. To remedy this, first clear the CMOS per instructions in this manual and retry BIOS flashing procedure. If you still do not have video, please use the following BIOS recovery procedure. Turn your system off and place the floppy disk with the saved BIOS image file (see above FAQ) in drive A. Press and hold "CTRL" and "Home" at the same time, then turn on power with these keys pressed until your floppy drive starts reading. Your screen will remain blank until the BIOS program is done. If system reboots correctly, then recovery is done.

Question: **I have memory problems. What is the correct memory to use and which BIOS setting should I choose?**

Answer: The correct memory to use on the SUPER P6DBS/P6DBE/P6DBU/P6SBU/P6SBS/P6SBA is 168-pin DIMM 3.3v non-buffered SPD (Serial Present Detection) SDRAM, SDRAM and EDO memory. SPD SDRAM is preferred but is not necessary. IMPORTANT: Please do not mix memory types; the results are unpredictable. If your memory count is exactly half of the correct value, please go to the BIOS in Chipset Setup and set "SDRAM AUTOSIZING SUPPORT" to *Enabled*. Change between available options until one setting correctly displays your memory.

Question: **Which Operating System (OS) supports AGP?**

Answer: At present Windows 98 and Windows NT 5.0 are the only OS that will have built-in support for AGP. Some AGP video adapters can run Windows 95 OSR2.1 with special drivers. Please contact your graphics adapter vendor for more details.

Question: **Do I need the CD that came with your motherboard?**

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications included on the CD are PCI IDE Bus Master drivers for Windows 95 and Windows NT, 440BX chipset drivers for Windows 95, and Super Doctor Monitoring software.

Question: **How do I install an on-board SCSI device controller for my P6DBS/P6SBS motherboard.**

Answer: First install 3 NT installation disks and then follow the on-screen instructions to complete the procedure. "Safe mode" is best for this installation.

Question: **Why can't I turn off the power using the momentary power on/off switch?**

Answer: The instant power off function is controlled by the BIOS. When this feature is enabled in the BIOS, the motherboard will have instant off capabilities as long as the BIOS has control of the system. When this feature is disabled or when the BIOS is not in control, such as during memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down. This feature is required to implement ACPI features on the motherboard.

Question: **I see some of my PCI devices sharing IRQs, but the system seems to be fine, is this correct or not?**

Answer: Some PCI Bus Mastering devices can share IRQs without performance penalties. These devices are designed to work correctly while sharing IRQs.

Question: **When I connect my Ultra II LVD Hard Drive on the JA1 SCSI connection, the drive was not recognized by BIOS or it failed to boot. Do I need a special cable?**

Answer: Yes, for Ultra II LVD Drive, you need a special 68-pin cable with active termination at the end of the cable, since Ultra II LVD Hard Drive does not have termination on the drive.

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton, and mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse, or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Chapter 4
AMI BIOS

4-1 Introduction

This chapter describes the AMIBIOS for the Intel 440BX Pentium II 400/350/333/300/266/233 MHz processors. The AMI ROM BIOS is stored in the Flash EEPROM and is easily upgraded using a floppy disk-based program.

System BIOS

The BIOS is the basic input output system used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. The WinBIOS is a high-quality example of a system BIOS.

Configuration Data

AT-compatible systems, also called ISA (Industry Standard Architecture) must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

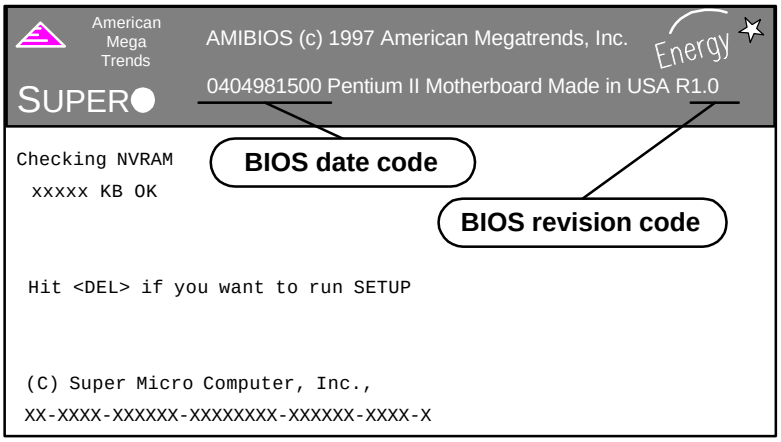
How Data Is Configured

AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM.

POST Memory Test

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown on the next page.

An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message.



4-2 BIOS Features

- supports Plug and Play V1.0A and DMI 2.1
- supports Intel PCI 2.1 (Peripheral Component Interconnect) local bus specification
- supports Advanced Power Management (APM) specification v 1.1
- supports xACP2
- supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- can be used as a boot device
- is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The PC Health Monitoring chips monitor:

- CPU temperature
- additional temperature sensors
- chassis intrusion detector

- five positive voltage inputs
- two negative voltage inputs
- three fan speed monitoring inputs

BIOS Configuration Summary Screen

AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

```
    AMIBIOS System Configuration (C) 1985-1997 American Megatrends Inc.,

Main Processor      : Pentium(tm) II      Base Memory Size    : 640 KB
Math Processor      : Built-In            Ext. Memory Size    : 64512 KB
Floppy Drive A:     : 1.44 MB, 3 1/2      Display Type        : VGA/EGA
Floppy Drive B:     : None                Serial Port(s)      : 3F8, 2F8
AMI-BIOS Date       : 7/15/95             Parallel Port(s)    : 378
Processor Clock     : 350MHz              External Cache      : 512 KB

PCI Devices
PCI Onboard PCI Bridge                    PCI Onboard Bridge Device
PCI Onboard USB Controller                PCI Onboard IDE
PCI Onboard SCSI, IRQ 10                  PCI Onboard SCSI, IRQ 10
PCI Slot 4 VGA, IRQ 11
```

*Note: The picture above reflects a board equipt with SCSI, but may be taken as a general example.

AMIBIOS Setup

See the following page for examples of the AMIBIOS Setup screen, featuring options and settings. Figure 4-1 shows the ***Standard*** option highlighted. To highlight other options, use the arrow keys, or use the tab key to move to other option boxes. Figure 4-2 shows the settings for the Standard setup. Settings can be viewed by highlighting a desired option and pressing <Enter>. Use the arrow keys to choose a setting. Note: Optimal settings for all options can be set automatically. Go to the ***Optimal*** icon in the default box and press <Enter>. Use the arrow keys to highlight *yes,* then press <Enter>.

Figure 4-1. Standard Option Highlighted

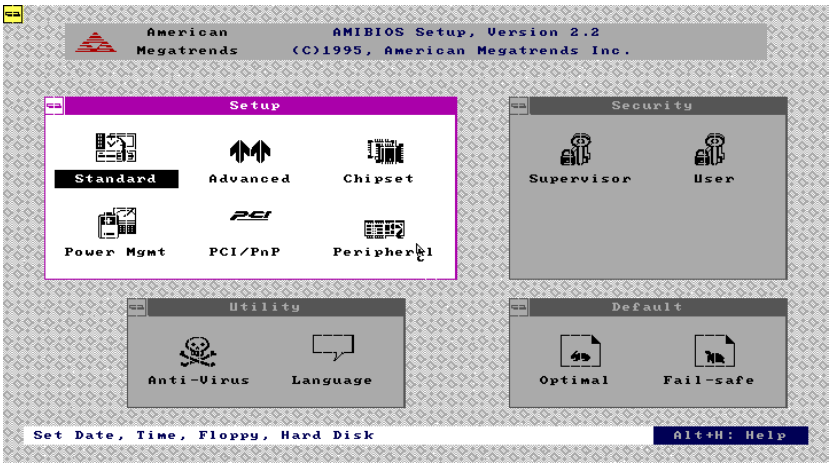
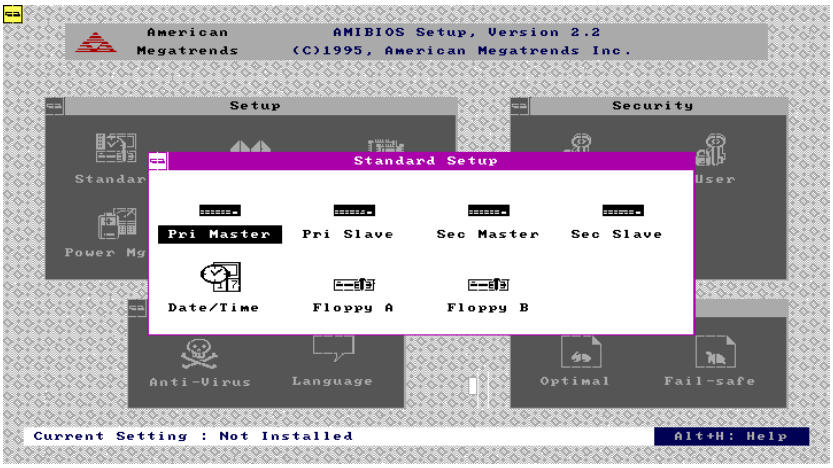


Figure 4-2. Settings for Standard Option



Chapter 5
Running Setup*

Optimal and Fail-Safe default settings are bolded in text unless otherwise noted.

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the options.

5-1 Setup

5-1-1 Standard Setup

Pri Master
Pri Slave
Sec Master
Sec Slave
Select these options to configure the drive named in the option. Select *Auto Detect IDE* to let AMIBIOS automatically configure the drive. A screen with a list of drive parameters appears. Click on *OK* to configure the drive.

Type	How to Configure
SCSI	Select *Type*. Select *Not Installed* on the drive parameter screen. The SCSI drivers provided by the SCSI manufacturer should allow you to configure the SCSI drive.
IDE	Select *Type*. Select *Auto* to let AMIBIOS determine the parameters. Click on OK when AMIBIOS displays the drive parameters. Select *LBA Mode*. Select *On* if the drive has a capacity greater than 540 MB. Select the *Block Mode*. Select *On* to allow block mode data transfers. Select the *32-bit mode*. Select *On* to allow 32-bit data transfers. Select *PIO mode*. Select *On* to allow AMIBIOS to determine the PIO Mode. It

	is best to select *Auto* to allow AMIBIOS to determine the PIO mode. If you select a PIO mode that is not supported by the IDE drive, the drive will not work properly. If you are absolutely certain that you know the drive's PIO mode, select PIO mode 0-4, as appropriate
CD ROM	Select *Type*. Select *CDROM*. Click on OK when AMIBIOS displays the drive parameters.

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drive may have even more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Date and Time Configuration

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values through the keyboard.

Floppy A
Floppy B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are *Not Installed, 360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch* or *2.88 MB 3½ inch*. ***Note: The Optimal and Fail-Safe settings for Floppy Drive A are 1.44 MB 3 1/2 inch and for Floppy Drive B are Not Installed***.

5-1-2 Advanced Setup

Quick Boot

The Settings are ***Disabled*** or *Enabled*. Set to *Enabled* to permit AMIBIOS to boot quickly when the computer is powered on. This option replaces the old Above 1 MB Memory Test Advanced Setup option. The settings are:

Setting	Description
Disabled	AMIBIOS tests all system memory. AMIBIOS waits up to 40 seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a <Del> key press and runs AMIBIOS Setup if the key has been pressed.
Enabled	AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. In *Enabled,* keyboard will be bypassed.

Note: You cannot run AMIBIOS Setup at system boot, because there is no delay for the Hit <Del> to run Setup message.

Pri Master ARMD Emulated as
Pri Slave ARMD Emulated as
Sec Master ARMD Emulated as
Sec Slave ARMD Emulated as
Options for Pri Master ARMD Emulated as, Pri Slave ARMD Emulated as, Sec Master ARMD Emulated as and Sec Slave ARMD Emulated as are ***Auto***, *Floppy* or *Hard disk*.

1st Boot Device
2nd Boot Device
3rd Boot Device
The options for 1st Boot Device are *Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD,* ***Floppy****, ARMD-FDD, ARMD-HDD, ATAPI CD ROM, SCSI, Network* or *I_20*. The options for 2nd Boot Device are *Disabled,* ***1st IDE-HDD****, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or ATAPI CD ROM*. The options for 3rd Boot Device are *Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or* ***ATAPI CD ROM***.

1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD and 4th IDE-HDD are the four hard disks that can be installed by the BIOS. 1st IDE-HDD is the first hard disk installed by the BIOS, 2nd IDE-HDD is the second hard disk, and so on. For example, if the system has a hard disk connected to Primary Slave and another hard disk to Secondary Master, then 1st IDE-HDD will be referred to as the hard disk connected to Primary Slave and 2nd IDE-HDD will be referred to as the hard disk connected to the Secondary Master. 3rd IDE-HDD and 4th IDE-HDD are not present. Note that the order of the initialization of the devices connected to the primary and secondary channels are Primary Master first, Primary Slave second, Secondary Master third, and Secondary Slave fourth.

The BIOS will attempt to read the boot record from 1st, 2nd, 3rd and 4th boot device in the selected order until it is successful in reading the booting record. The BIOS will not attempt to boot from any device which is not selected as the boot device.

Try Other Boot Device
This option controls the action of the BIOS if all the selected boot devices failed to boot. The settings for this option are ***Yes*** or *No*. If *Yes* is selected and all the selected boot devices failed to boot, the BIOS will try to boot from the other boot devices (in a predefined sequence) which are present but not selected as boot devices in the setup (and hence not yet

been tried for booting). If selected as *No* and all selected boot devices failed to boot, the BIOS will try not to boot from the other boot devices which may be present but not selected as boot devices in setup.

Initial Display Mode

This option determines the display screen with which the POST is going to start the display. The settings for this option are ***BIOS*** or *Silent*. If selected as *BIOS,* the POST will start with the normal sign-on message screen. If *Silent* is selected, the POST will start with the silent screen.

Display Mode at Add-on ROM Init

This option determines the display mode during add-on ROM (except Video add-on ROM) initialization. The settings for this option are ***Force BIOS*** or *Keep Current*. If selected as *Force BIOS,* the POST will force the display to be changed to BIOS mode before giving control to any add-on ROM. If no add-on ROM is found, then the current display mode will remain unchanged even if this setup question is selected as *Force BIOS.* If selected as *Keep Current,* then the current display mode will remain unchanged.

Floppy Access Control

The settings for this option are ***Read-Write*** or *Read-Only*.

Hard Disk Access Control

The settings for this option are ***Read-Write*** or *Read-Only*.

S.M.A.R.T. for Hard Disks

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a technology developed to manage the reliability of the hard disk by predicting future device failures. The hard disk needs to be S.M.A.R.T. capable. The settings for this option are ***Disabled*** or *Enabled*. ****Note: S.M.A.R.T. cannot predict all future device failures. S.M.A.R.T. should be used as a warning tool, not as a tool to predict the device reliability***.

Boot Up Num-Lock

Settings for this option are ***On*** or *Off*. When this option is set to *On*, the BIOS turns off the Num Lock key when the system is powered on. This will enable the end user to use the arrow keys on both the numeric keypad and the keyboard.

PS/2 Mouse Support
Settings for this option are ***Enabled*** or *Disabled*. When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse.

Primary Display
This option specifies the type of display adapter card installed in the system. The settings are *Absent,* ***VGA/EGA***, *CGA40x25*, *CGA80x25* or *Mono*.

Password Check
This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if WinBIOS Setup is executed.

Boot to OS/2
If DRAM size is over 64 MB, set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are ***No*** or *Yes*.

CPU Microcode Updation
Set this option to *Enabled* to permit the CPU to be updated on line. The settings for this option are ***Enabled*** or *Disabled*.

Internal Cache
This option is for enabling or disabling the internal cache memory. The settings for this option are *Disabled* or ***WriteBack***.

System BIOS Cacheable
When set to *Enabled*, the contents of the F0000h system memory segment can be read from or written to cache memory. The contents of this memory segment are always copied from the BIOS ROM to system RAM for faster execution. The settings are *Enabled* or *Disabled*. ***Note: The Optimal default setting is Enabled and the Fail-Safe default setting is Disabled. Set this option to Enabled to permit the contents of F0000h RAM memory segment to be written to and read from cache memory.***

CPU ECC
The settings for this option are ***Enabled*** or *Disabled*. This option enables Pentium II L2 cache ECC function.

MPS Revision
The settings for this option are 1.1 or **1.4**.

C000, 16K Shadow
C400, 16K Shadow
These options specify how the 32 KB of video ROM at C0000h is treated. The settings are: *Disabled*, *Enabled or* ***Cached***. When set to *Disabled,* the contents of the video ROM are not copied to RAM. When set to *Enabled,* the contents of the video ROM area from C0000h-C7FFFh are copied (shadowed) from ROM to RAM for faster execution. When set to *Cached*, the contents of the video ROM area from C0000h-C7FFFh are copied from ROM to RAM, and can be written to or read from cache memory.

C800, 16K Shadow
CC00, 16K Shadow
D000, 16K Shadow
D400, 16K Shadow
D800, 16K Shadow
DC00, 16K Shadow
These options enable shadowing of the contents of the ROM area named in the option. The ROM area not used by ISA adapter cards is allocated to PCI adapter cards. The settings are: ***Disabled*****,** *Enabled or Cached*. When set to *Disabled,* the contents of the video ROM are not copied to RAM. When set to *Enabled,* the contents of the video ROM area from C0000h-C7FFFh are copied (shadowed) from ROM to RAM for faster execution. When set to *Cached,* the contents of the video ROM area from C0000h-C7FFFh are copied from ROM to RAM and can be written to or read from cache memory.

5-1-3 Chipset Setup

USB Function
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the USB (Universal Serial Bus) functions.

USB KB/Mouse Legacy Support
The settings for this option are *Keyboard, Auto, Keyboard+Mouse* or ***Disabled***. Set this option to *Enabled* to enable the USB keyboard and mouse.

SERR# (System Error)

The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable the SERR# signal on the bus. BX asserts this signal to indicate a system error condition. SERR# is asserted under the following conditions:

- In an ECC configuration, the 82443BX asserts SERR#, for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored.
- The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated PCI cycle
- The 82443BX can also assert SERR# when a PCI parity error occurs during the address or data phase
- The 82443BX can assert SERR# when it detects a PCI address or data parity error on AGP
- The 82443BX can assert SERR# upon detection of access to an invalid entry in the Graphics Aperature Translation Table
- The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture and outside of main DRAM range (i.e. in the 640k - 1M range or above TOM)
- The 82443BX can assert SERR# upon detecting an invalid AGP master access outside of AGP aperture.
- The 82443BX asserts SERR# for one clock when it detects a target abort during 82443BX initiated AGP cycle

PERR#

This option signals data parity errors of the PCI bus. The settings are *Enabled* or ***Disabled***. Set to *Enabled* to enable the PERR# signal.

WSC# Handshake (Write Snoop Complete)

This signal is asserted active to indicate that all the snoop activity on the CPU bus on the behalf of the last PCI-DRAM write transaction is complete and that it is safe to send the APIC interrupt message. The settings for this option are ***Enabled*** or *Disabled*. Set to *Enabled* to enable handshaking for the WSC# signal.

USWC Write Post

The settings for this option are ***Enabled*** or *Disabled*. This option sets the status of USWC (Uncacheable, Speculative, Write-Combining) posted writes and is used to combine several partial writes to the frame buffer into a single write in order to reduce the data bus traffic. Set to *Enabled* to enable USWC posted writes to I/O. Set to *Disabled* to disable USWC posted writes to I/O.

BX/GX Master Latency Timer (CLKs)
This option specifies the master latency timings (in PCI clocks) for devices in the computer. It defines the number of PCI clocks a PCI master can own on the bus after PCI central arbiter removes the grant signal. The settings are *Disabled*, *32*, ***64***, *96*, *128*, *160*, *192* or *224*.

Multi-Trans Timer (Clks)
This option specifies the multi-trans latency timings (in PCI clocks) for devices in the computer. It reduces overhead switching between different masters. The settings are *Disabled*, ***32***, *64*, *96*, *128*, *160*, *192* or *224*.

PCI1 to PCI0 Access
PCI1 refers to AGP in BX and LX chipsets. PCI0 is the normal PCI bus. ***Note: Normally AGP master should not access to a PCI target***. The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable access between two different PCI buses (PCI1 and PCI0).

Memory Autosizing Support
The dynamic detection and sizing of SDRAM and EDO is performed by the BIOS in a system populated with memory which has no SPD information. When set to *Enable*, memory does not have the SPD information. The settings for this option are ***Auto*** or *Enable*.

DRAM Integrity Mode
The settings for this option are ***None***, *EC* or *ECC Hardware*. ***Note: For ECC memory only. See the table below to set the type of system memory checking.*** (Note: New BIOS versions automatically detect setting and do not need to be set by user.)

Setting	Description
None	No error checking or error reporting is done.
EC	Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset. Corrected bits of data from memory are not written back to DRAM system memory.
ECC Hardware	Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset and are written back to DRAM system memory. If a soft (correctable) error occurs, writing the fixed

data back to DRAM system memory will resolve the problem. Most DRAM errors are soft errors. If a hard (uncorrectable) error occurs, writing the fixed data back to DRAM system memory does not solve the problem. In this case, the second time the error occurs in the same location, a Parity Error is reported, indicating an uncorrectable error. If ECC is selected, AMIBIOS automatically enables the System Management Interface (SMI). If you do not want to enable power management, set the **Power Management/APM** option to *Disabled* and set all Power Management Setup timeout options to *Disabled*. To enable power management, set **Power Management/APM** to *Enabled* and set the power management timeout options as desired.

DRAM Refresh Rate

This option specifies the interval between Refresh signals to DRAM system memory. The settings for this option are ***15.6 us*** (micro-seconds), *31.2 us*, *62.4 us*, *124.8 us* or *249.6 us*.

Memory Hole

This option specifies the location of an area of memory that cannot be addressed on the ISA bus. The settings are ***Disabled***, *15 MB-16 MB*, or *512 KB-640 KB*.

SDRAM CAS# Latency

This option regulates the column address strobe. The settings are 2 SCLKs, 3 SCLKs or ***Auto***.

SDRAM RAS# to CAS# Delay

This option specifies the length of the delay inserted between the RAS and CAS signals of the DRAM system memory access cycle if SDRAM is installed. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs* or *3 SCLKs*. ***Note: The Optimal default setting is Auto and the Fail-Safe default setting is 3 SCLKs***.

SDRAM RAS# Precharge

This option specifies the length of the RAS precharge part of the DRAM system memory access cycle when Synchronous DRAM system memory is installed in the computer. The settings are *Auto* (AMIBIOS automatically

determines the optimal delay), *2 SCLKs or 3 SCLKs*. ***Note: The Optimal default setting is Auto and the Fail-Safe default setting is 3 SCLKs.***

Power Down SDRAM
BX supports SDRAM power down mode to minimize SDRAM power usage. The settings for this option are *Enabled* or ***Disabled***. The *Enabled* setting enables the SDRAM Power Down feature.

ACPI Control Register
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the ACPI (Advanced Configuration and Power Interface) control register.

Gated Clock
Signal GCLKEN enables internal dynamic clock gating in the 82443BX when a AGPset "IDLE" state occurs. This happens when the 82443BX detects an idle state on all its buses. The settings for this option are ***Enabled*** or *Disabled*. The *Enabled* setting enables the gated clock.

Graphics Aperture Size
This option specifies the amount of system memory that can be used by the Accelerated Graphics Port (AGP). The settings are *4 MB*, *8 MB*, *16 MB*, *32 MB*, ***64 MB***, *128 MB*, or *256 MB*.

Search for MDA (Monochrome Adapter) Range (B0000h-B7FFFh) Resources
Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In an AGP system, accesses in the normal VGA range are forwarded to the AGP bus. Since the monochrome adapter may be on the PCI (or ISA) bus, the 82443BX must decode cycles in the MDA range and forward them to PCI. The settings for this option are ***Yes*** or *No*. Set this option to *Yes* to let AMIBIOS search for MDA resources.

AGP Multi-Trans Timer (AGP Clks)
This option sets the AGP multi-trans timer. The settings are in units of AGP clocks: ***32***, *64*, *96*, *128*, *160*, *192*, or *224*.

AGP Low-Priority Timer
This option controls the minimum tenure on the AGP for low priority data transaction for both read and write. The settings are *Disabled, **32**, 64, 96, 128, 160, 192 or 224*.

AGP SERR (Advanced Graphic Port System Error)
BX asserts this signal to indicate a AGP system error condition. The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable the AGP SERR# signal.

AGP Parity Error Response
The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable the AGP (Accelerated Graphics Port) to respond to parity errors.

8bit I/O Recovery Time
This option specifies the length of a delay inserted between consecutive 8-bit I/O operations. The settings are ***Disabled***, *1 SYSCLK*, *2 SYSCLKs*, *3 SYSCLKs*, *4 SYSCLKs*, *5 SYSCLKs*, *6 SYSCLKs*, *7 SYSCLKs* or *8 SYSCLKs*.

16bit I/O Recovery Time
This option specifies the length of a delay inserted between consecutive 16-bit I/O operations. The settings are ***Disabled***, *1 SYSCLK*, *2 SYSCLKs*, *3 SYSCLKs*, *4 SYSCLKs*, *5 SYSCLKs*, *6 SYSCLKs*, *7 SYSCLKs* or *8 SYSCLKs*.

PIIX4 SERR#
This signal is asserted to indicate a PIIX4 System Error condition. The settings for this option are *Enabled* or ***Disabled***. The *Enabled* option enables the SERR# signal for the Intel PIIX4 chip.

USB Passive Release
BX releases USB bus when it is idle to maximize the USB bus usage. The settings for this option are ***Enabled*** or *Disabled*. Set this option to *Enabled* to enable passive release for USB.

PIIX4 Passive Release
This option functions similarly to USB Passive Release. The settings for this option are ***Enabled*** or *Disabled*. Set to *Enabled* to enable passive release for the Intel PIIX4 chip.

PIIX4 Delayed Transaction
BX is capable of PIIX4 transaction to improve PIIX4 interrupt efficiency. The settings for this option are ***Enabled*** or *Disabled*. Set this option to *Enabled* to enable delayed transactions for the Intel PIIX4 chip.

Type F DMA Buffer Control1
Type F DMA Buffer Control2
These options specify the DMA channel where Type F buffer control is implemented. The settings are ***Disabled***, *Channel-0*, *Channel-1*, *Channel-2*, *Channel-3*, *Channel-4*, *Channel-5*, *Channel-6* or *Channel-7*.

DMA0 Type
DMA1 Type
DMA2 Type
DMA3 Type
DMA5 Type
DMA6 Type
DMA7 Type
These options specify the bus that the specified DMA channel can be used on. The settings are *PC/PCI*, *Distributed*, or ***Normal ISA***.

Memory Buffer Strength
The settings for this option are ***Strong*** or *Auto*.

Manufacturer's Setting
Note: The user should always set this option to mode 0. All other modes are for factory testing only.

5-1-4 Power Management

Power Management
The settings for this feature are: ***APM***, *ACPI* or *Disabled*. Set to *APM* to enable the power conservation feature specified by Intel and Microsoft INT 15h Advance Power Management BIOS functions. Set to *ACPI* if your operating system supports Microsoft's Advanced Configuration and Power Interface (ACPI) standard.

Power Button Function
This option specifies how the power button mounted externally on the computer chassis is used. The settings are: *Suspend* or ***On/Off***. When set to *On/Off*, pushing the power button turns the computer on or off. When set to *Suspend*, pushing the power button places the computer in Suspend mode or Full On power mode.

Green PC Monitor Power State
This option specifies the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power savings state after the

specified period of display inactivity has expired. The settings are *Standby*, *Suspend* or *Off*. ***Note: The Optimal default setting for this option is Suspend and the Fail-Safe setting is Standby***.

Video Power Down Mode
This option specifies the power conserving state that the VGA video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. ***Note: The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled***.

Hard Disk Power Down Mode
This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are *Disabled*, *Standby*, or *Suspend*. ***Note: The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled***.

Hard Disk Timeout (Minutes)
This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters power-conserving state specified in the Hard Disk Power Down Mode option. The settings are ***Disabled*** and *1 Min through 15 Min in 1 minute intervals*.

Power Saving Type
The settings for this option are ***Sleep***, *Stop Clock or Deep Sleep*.

Standby/Suspend Timer Unit
This allows you to set the standby timeout and suspend timeout timer unit. The settings are *32 secs*, *4 msecs*, ***4 min*** or *4 secs*.

Standby Timeout
This option specifies the length of a period of system inactivity while in full power on state. When this length of time expires, the computer enters standby power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Suspend Timeout (Minutes)
This option specifies the length of a period of system inactivity while in standby state. When this length of time expires, the computer enters suspend power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Slow Clock Ratio
The value of the slow clock ratio indicates the percentage of time the STPCLK# signal is asserted while in the thermal throttle mode. The settings are *Disabled, 0-12.5%*, 12.5-*25%*, 25-*37.5%*, *37.5-50%*, ***50-62.5%***, *62.5-75%*, or *75-87.5%*.

Display Activity
This option specifies if AMIBIOS is to monitor display activity for power conservation purposes. When this option is set to *Monitor* and there is no display activity for the length of time specified in the Standby Timeout (Minute) option, the computer enters a power savings state. The settings are *Monitor* or ***Ignore***.

Device 6 (Serial port 1)
Device 7 (Serial port 2)
Device 8 (Parallel port)
Device 5 (Floppy disk)
Device 0 (Primary Master IDE)
Device 1 (Primary Slave IDE)
Device 2 (Secondary Master IDE)
Device 3 (Secondary Slave IDE)
When set to *Monitor*, these options enable event monitoring on the specified hardware interrupt request line. If set to Monitor and the computer is in a power saving state, AMIBIOS watches for activity on the specifies IRQ line. The computer enters the Full On state if any activity occurs. AMIBIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ line. ***Note: The Optimal default setting for each option is Ignore with the exception of Devices 0 (Primary Master IDE) and 6 (Serial Port 1) which should be set to Monitor. The Fail-Safe default for each option is Monitor.***

LAN Wake-Up
RTC Wake-UP
Options for LAN Wake-Up and RTC Wake-Up are ***Disabled*** or *Enabled*. When enabled, the **Hour** and **Minute** functions become available.

5-1-5 PCI/PnP Setup

Plug and Play-Aware OS
The settings for this option are ***No*** or *Yes*. Set this option to *Yes* if the operating system in the computer is aware of and follows the Plug and Play specification. AMIBIOS only detects and enables PnP ISA adapter

cards that are required for system boot. Currently, only Windows 95 is PnP-Aware. Set this option to *No* if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly. Otherwise, PnP-aware adapter cards installed in the computer will not be configured properly.

PCI Latency Timer (PCI Clocks)

This option specifies the latency timings in PCI clocks for all PCI devices. The settings are *32*, ***64***, *96*, *128*, *160*, *192*, *224*, or *248*.

PCI VGA Palette Snoop

The settings for this option are ***Disabled*** or *Enabled.* When set to *Enabled,* multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example: if there are two VGA devices in the computer (one PCI and one ISA) and this option is disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers. If enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA palette registers. This will permit the palette registers of both devices to be identical. This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping.

PCI IDE Busmaster

The settings for this option are ***Disabled*** or *Enabled*. Set to *Enabled* to specify the IDE Controller on the PCI bus has bus mastering capabilities. Under Windows 95, you should set this option to *Disabled* and install the Bus Mastering driver.

Offboard PCI IDE Card

This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. The PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed must be specified. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are ***Auto*** (AMIBIOS automatically determines where the offboard PCI IDE controller adapter card is installed), *Slot 1*, *Slot 2*, *Slot 3*, *Slot 4, Slot 5* or *Slot 6*.

This option forces IRQ14 and IRQ15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant ISA IDE controller adapter cards. If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

Offboard PCI IDE Primary IRQ
Offboard PCI IDE Secondary IRQ
These options specify the PCI interrupt used by the primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are ***Disabled***, *Hardwired*, *INTA*, *INTB*, *INTC*, or *INTD*.

PCI Slot1 IRQ Priority
PCI Slot2 IRQ Priority
PCI Slot3 IRQ Priority
PCI Slot4 IRQ Priority
These options specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are ***Auto***, *(IRQ) 3, 4, 5, 7, 9, 10,* or *11, in priority order***.**

DMA Channel 0
DMA Channel 1
DMA Channel 3
DMA Channel 5
DMA Channel 6
DMA Channel 7
These DMA channels control the data transfers between the I/O devices and the system memory. The chipset allows the BIOS to choose which channels to do the job. The settings are ***PnP*** or *ISA/EISA.*

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
These options specify which bus the specified IRQ line is used on and allow you to reserve IRQs for legacy ISA adapter cards. If more IRQs

must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an *ISA/EISA* setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP.

IRQ14 and 15 will not be available if the onboard PCI IDE is enabled. If all IRQs are set to *ISA/EISA* and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ 9 will still be available for PCI and PnP devices. This is because at least one IRQ must be available for PCI and PnP devices. The settings are ***PCI/PnP*** or *ISA/EISA.*

Reserved Memory Size
This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are ***Disabled***, *16K*, *32K* or *64K*.

Reserved Memory Address
This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are *C0000*, *C4000*, ***C8000***, *CC000*, *D0000*, *D4000*, *D8000* or *DC000*.

Default Primary Video
This feature supports multiple displays. The settings are ***AGP*** or *PCI*.

5-1-6 Peripheral Setup

On-board SCSI
The settings for this option are ***Enabled*** or *Disabled*. When set to *Enable* this option enables the Adaptec 7895 BIOS on the P6DBS/P6SBS motherboards or the Adaptec 7890 on the P6DBU/P6SBU motherboards.

Remote Power On
Microsoft's Memphis OS supports this feature which can wake-up the system from SoftOff state through devices (such as an external modem) that are connected to COM1 or COM2. The settings are ***Disabled*** or *Enabled*.

CPU Current Temperature
The current CPU temperature is displayed in this option.

CPU Overheat Warning
The settings for this option are *Enabled* or ***Disabled***. When set to *Enabled* this option allows the user to set an overheat warning temperature.

CPU Overheat Warning Temperature
Use this option to set the CPU overheat warning temperature. The settings are *25 °C through 75 °C in 1 °C intervals*. ***Note: The Optimal and Fail-Safe default settings are 55 °C***.

H/W Monitor In0 (CPU 1)
H/W Monitor In1 (CPU 2)
H/W Monitor In2 (+3.3V)
H/W Monitor In3 (+5V)
H/W Monitor In4 (+12V)
H/W Monitor In5 (-12V)
H/W Monitor In6 (-5V)
CPU1 Fan
CPU2 Fan
Thermal Control Fan
The above features are for PC Health Monitoring. The motherboards with W83781D have seven on-board voltage monitors for the CPU core, CPU I/O, +3.3V, +5V, -5V, +12V, and -12V, and three fan status monitors.

On-Board FDC
This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are *Auto* (AMIBIOS automatically determines if the floppy controller should be enabled), *Disabled*, or ***Enabled***.

On-Board Serial Port 1
This option specifies the base I/O port address of serial port 1. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, ***3F8h/COM1***, *2F8h/COM2*, *3E8h/COM3* or *2E8h/COM4*.

On-Board Serial Port 2
This option specifies the base I/O port address of serial port 2. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h/COM1*, ***2F8h/COM2***, *3E8h/COM3* or *2E8h/COM4*.

Serial Port 2 Mode
The settings for this option are ***Normal***, *IrDA* or *ASK IR*. When set to *IrDA,* the IR Duplex Mode becomes available and can be set to either Half or Full. When set to *ASK IR,* the IrDA Protocol becomes available and can be set to 1.6 us or 3/16.

On-Board Parallel Port
This option specifies the base I/O port address of the parallel port on the motherboard. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, ***378***, *278* or *3BC*.

Parallel Port Mode
This option specifies the parallel port mode. The settings are *Normal*, *Bi-Dir*, *EPP* or *ECP*. When set to *Normal,* the normal parallel port mode is used. Use *Bi-Dir* to support bidirectional transfers. Use *EPP* (Enhanced Parallel Port) to provide asymmetric bidirectional data transfer driven by the host device. Use *ECP* (Extended Capabilities Port) to achieve data transfer rates of up to 2.5 Mbps. ECP uses the DMA protocol and provides symmetric bidirectional communication. ***Note: The Optimal default setting for this option is ECP and the Fail-Safe setting is Normal***.

EPP Version
The settings are *1.7* or *1.9*. ***Note: The Optimal and Fail-Safe default settings are N/A***.

Parallel Port IRQ
This option specifies the IRQ to be used by the parallel port. The settings are ***Auto***, *5* or *7*.

Parallel Port DMA Channel
This option is only available if the setting of the parallel port mode option is *ECP*. The settings are *0*, *1*, *2*, *3*, *5*, *6* or *7*. ***Note: This option is N/A***.

On-Board IDE
This option specifies the onboard IDE controller channels to be used. The settings are *Disabled, Primary*, *Secondary* or ***Both***.

5-2 Security Setup

5-2-1 Supervisor User

The system can be configured so that all users must enter a password every time the system boots or when the WINBIOS setup is executed. You can set either a Supervisor password or a User password. If you do not want to use a password, just press <Enter> when the password prompt appears.

The password check option is enabled in the Advanced Setup by choosing either *Always* or *Setup*. The password is stored in CMOS RAM. You can enter a password by typing the password on the keyboard, selecting each letter via the mouse, or selecting each letter via the pen stylus. Pen access must be customized for each specific hardware platform.

When you select Supervisor or User, AMIBIOS prompts for a password. You must set the Supervisor password before you can set the User password. Enter a 1-6 character password. The password does not appear on the screen when typed. Retype the new password as prompted and press <Enter>. Make sure you write it down. If you forget it, you must drain CMOS RAM and reconfigure.

5-3 Utility Setup

5-3-1 Anti-Virus

When this icon is selected, AMIBIOS issues a warning when any program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive. The settings are *Enabled* or ***Disabled***.

5-3-2 Language

Note: The Optimal and Fail-Safe default settings for this option are English.

5-4 Default Setting

Every option in WinBIOS Setup contains two default settings: a Fail-Safe default, and an Optimal default.

5-4-1 Optimal Default

The Optimal default settings provide optimum performance settings for all devices and system features.

5-4-2 Fail-Safe Default

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Appendix A
BIOS Error Beep Codes & Messages

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error was detected in the base memory (the first 64 KB block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64 KB of memory.
4	Timer Not Operational	A memory failure was detected in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU on the system board generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error means that the BIOS cannot switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the motherboard generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. ***Please Note:*** This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS memory has failed.

Refer to the table on page A-3 for solutions to the error beep codes.

If it beeps...	**then ...**
1, 2, 3 times	reseat the DIMM memory. If the system still beeps, replace the memory.
6 times	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
4, 5, 7, or 10 times	the motherboard must be replaced.

Error Message	Information
8042 Gate -- A20 Error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
C: Drive Error	Hard disk drive C: does not respond. Run the Hard Disk Utility to correct this problem. Also, check the C: hard disk type in Standard Setup to make sure that the hard disk type is correct.
C: Drive Failure	Hard disk drive C: does not respond. Replace the hard disk drive.
Cache Memory Bad	Cache memory is defective. Replace it. Do Not Enable Cache!
CH-2 Timer Error	Most ISA computers include two times. There is an error in time 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run WINBIOS Setup or AMIBIOS Setup.
CMOS System Option Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run WINBIOS Setup or AMIBIOS Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run WINBIOS Setup or AMIBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run WINBIOS Setup or AMIBIOS Setup.

Error Message	Information
CMOS Time and Date Not Set	Run Standard Setup to set the date and time in CMOS RAM.
D: Drive Error	Hard disk drive D: does not respond. Run the Hard Disk Utility. Also check the D: hard disk type in Standard Setup to make sure that the hard disk drive type is correct.
D: Drive Failure	Hard disk drive D: does not respond. Replace the hard disk.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the computer. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	Some compters require a video switch on the motherboard be set to either color or monochrome. Turn the computer off, set the switch, then power on.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the computer is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the computer is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.

Error Message	Information
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the computer. Use another boot disk.
Keyboard Is Locked... Unlock It	The keyboard lock on the computer is engaged. The computer must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard. Set the *Keyboard* options in Standard Setup to *Not Installed* to skip the keyboard post routines.
KB/Interface Error	There is an error in the keyboard connector.
No ROM BASIC	Cannot find a bootable sector on either disk drive A: or hard disk drive C:. The BIOS calls INT 18h which generates this message. Use a bootable disk.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
On Board Parity Error	Parity error in motherboard memory. The format is: ON BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
Parity Error????	Parity error in system memory at an unknown address. Run AMIDiag to find and correct memory problems.

Appendix B

AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMI BIOS.

Check Point	Description
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next.
03	NMI is Disabled. Next, checking for a soft reset or a power-on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the post code unit next.
07	Next, initializing the CPU init and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before keyboard BAT command is issued.
0C	The keyboard controller I/B is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0F	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.

Check Point	Description
10	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh test line is toggling. Checking the 15 second on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG Switch is on.
27	Any initialization before setting video mode will be done next.

Check Point	Description
28	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30	The display memory read/write test passed. Look for retrace checking next.
31	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.

Check Point	Description
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error messages.
3A	The new cursor position has been read and saved. Displaying the Hit <DEL> message next.
40	Preparing the descriptor tables next.
42	The descriptor tables are prepared. Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been completed. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4B	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.

Check Point	Description
4C	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4D	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4F	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next.
59	The Hit <DEL> message is cleared. The <WAIT> message is displayed. Starting the DMA and interrupt controller test next.

Check Point	Description
60	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
7F	Extended NMI source enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	The command byte was written and global data initialization has been completed. Checking for a locked key next.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86	The password was checked. Performing any required programming before WINBIOS Setup next.

Check Point	Description
87	The programming before WINBIOS Setup has been completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89	The programming after WINBIOS Setup has been completed. Displaying the power-on screen message next.
8B	The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the WINBIOS Setup options next.
8D	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8F	The hard disk controller has been reset. Configuring the floppy drive controller next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has been completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.

Check Point	Description
99	Any initialization required after the option ROM test has been completed. Configuring the timer data area and printer base address next.
9A	Set the timer and printer base addresses. Setting the RS-232 base address next.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	The soft error display has completed. Setting the keyboard typematic rate next.
A4	The keyboard typematic rate is set. Programming the memory wait states next.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.

Check Point	Description
A9	Returned from adaptor ROM at E000h control. Next, performing any initialization required after the E000 option ROM had control.
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary. POST next.
B0	The system configuration is displayed.
AC	Uncompressing the DMI data and initializing DMI.
B1	Copying any code to specific areas.
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization cade checksum will be verified.
D1h	Initializing the DMA controller. Performing the keyboard controller BAT test. Starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl><Home>was pressed and verifying the system BIOS checksum.

If either <Ctrl><Home>was pressed or the system BIOS checksum is bad, next the system will go to checkpoint code E0h.

Otherwise, going to checkpoint code D7h.