

# Classic/PCI Low Profile Jumpers & Connectors

## PLEASE NOTE

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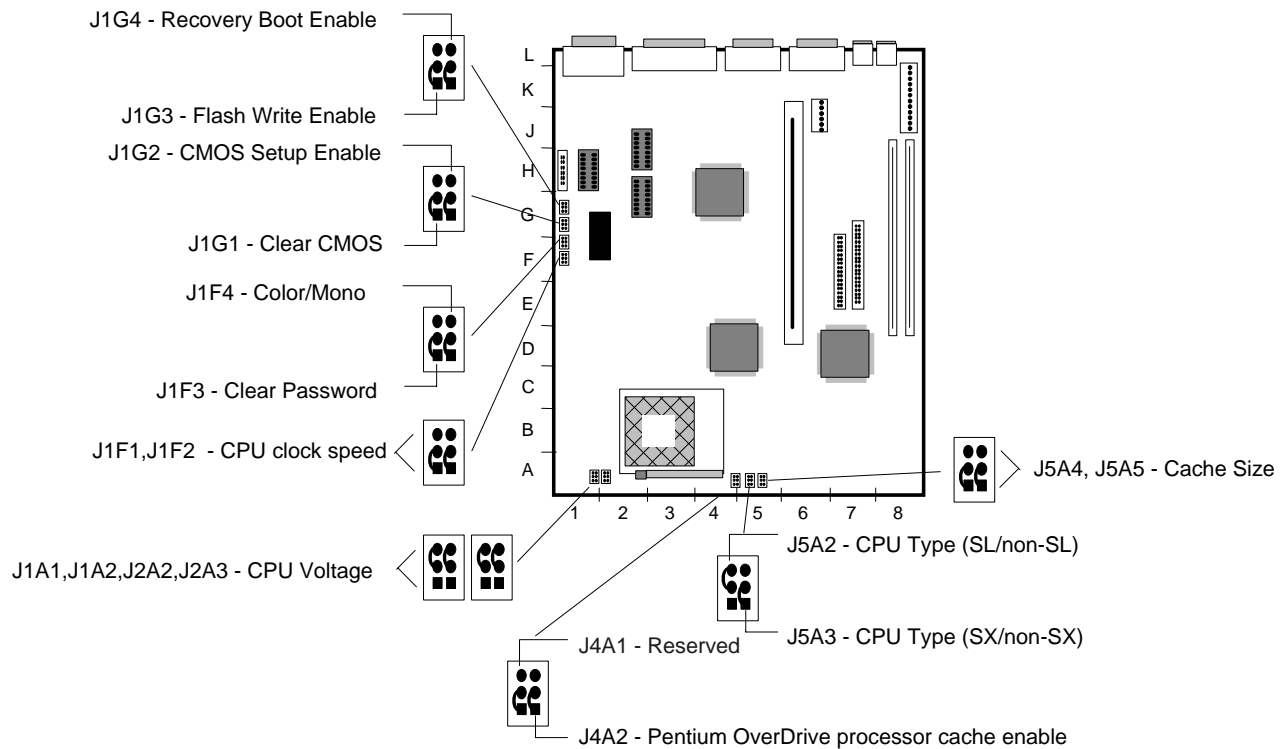


Figure B-1. Jumper locations and default settings (■ notes Pin 1 locations)

### **RECOVERY BOOT ENABLE – J1G4**

Allows recovery if the system FLASH update process results in corrupted EPROM

- 1-2 = Normal Boot (default)
- 2-3 = Recovery Boot

### **FLASH WRITE ENABLE – J1G3**

Allows reprogramming of Flash EPROM to be enabled or disabled

- 1-2 = Flash Write Enabled (default)
- 2-3 = Flash Write Protected

### **CMOS SETUP ENABLE – J1G2**

Allows access to CMOS Setup Utility to be disabled.

- 1-2 = Access to Setup allowed (default)
- 2-3 = Access to Setup prevented

### **CLEAR CMOS – J1G1**

Allows CMOS settings to be reset to default.

- 1-2 = Normal (default)
- 2-3 = Clear CMOS to default settings

### **CLEAR PASSWORD – J1F3**

Allows system password to be cleared.

- 1-2 = Password Enabled (default)
- 2-3 = Clear Password

**CPU CLOCK SPEED -- J1F1, J1F2**

There are two jumpers to select 25/33 MHz processor clocks. Both jumpers must have the same configuration for the CPU clock speed to be properly set. The default setting is determined by the processor shipped on the motherboard. Motherboards shipped without processors will be configured for a 33 MHz clock (1-2).

1-2 = 33 MHz

2-3 = 25 MHz

**CPU VOLTAGE (3.3V OR 5V) – J1A1, J1A2, J2A2, J2A3**

These four jumpers need to be moved to allow the use of the IntelDX4 microprocessor which operates at 3.3 volts. When all of the jumpers are moved into the 3.3 volt position (1-2) the on-board voltage regulator converts 5v to 3.3v for the IntelDX4 processor. This supplies 3.3v only to the processor socket. Default position is 2-3 for 5 volt operation.

1-2 = 3.3 volt

2-3 = 5 volt (default)

**WARNING: Do NOT move these jumpers while the power is on! The CPU could be damaged.**

**RESERVED – J4A1**

This jumper is reserved and should not be altered.

**PENTIUM OVERDRIVE PROCESSOR CACHE ENABLE -- J5A1**

This jumper normally is set to position 1-2. When installing a Pentium OverDrive processor, this jumper must be changed to 2-3 to properly set up the L1 cache for write-back mode.

1-2 = non Pentium OverDrive processors (default)

2-3 = Pentium OverDrive processor cache enabled

**CPU TYPE (SL/NON-SL) – J5A2**

This jumper is set to position 1-2 for non-SL enhanced processors and set to 2-3 for SL-enhanced processors. Note: All motherboards and systems shipped with processors have SL-enhanced processors installed.

1-2 = non SL-enhanced processors

2-3 = SL-enhanced processors (default)

**CPU TYPE (SX/NON-SX) – J5A3**

This jumper is set to position 2-3 for i486 SX processors and set to 1-2 for all other Intel processors. Note: The default setting is determined by the processor shipped. Motherboards shipped without processors will be configured for non SX processors (1-2).

1-2 = non SX processors (default)

2-3 = i486 SX processors

**CACHE SIZE – J5A4, J5A5**

Two jumpers to select cache options of 128 KB/256 KB. Both jumpers must have the same configuration for the cache to be properly set. If secondary (L2) cache is not installed, these jumper settings have no effect.

1-2 = 256 KB (default)

2-3 = 128 KB

# Connectors

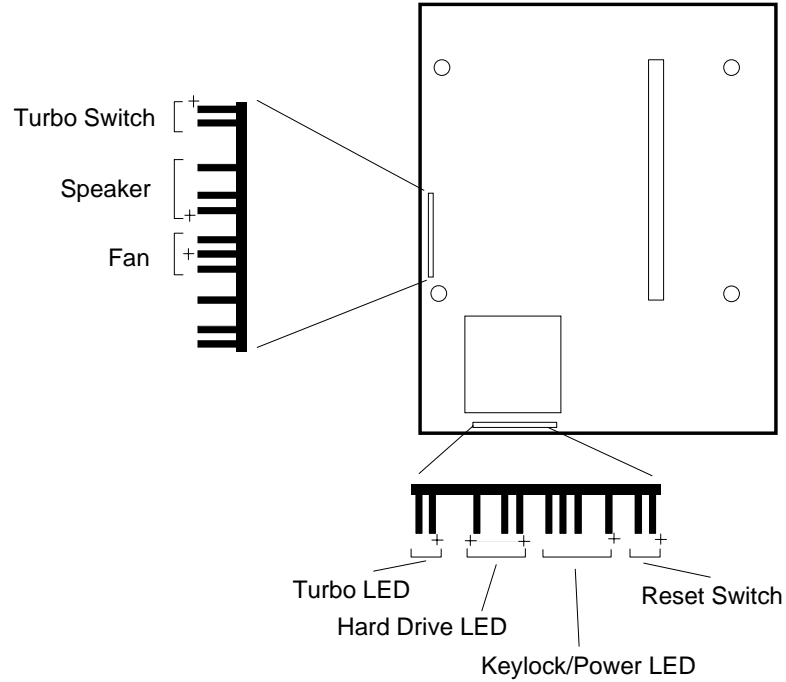


Figure C-1. Front panel connections

## TURBO SWITCH

Pin	Signal Name
1	TURBO
2	Ground
3	No Connect

## TURBO LED

Pin	Signal Name
1	TURBO LED
2	PULL_UP_330

## SPEAKER CONNECTOR

Pin	Signal Name
1	SPKR_DAT
2	Key
3	SPKRVCC
4	+5V Vcc

## HARD DRIVE LED

Pin	Signal Name
1	PULL_UP_330
2	Key
3	HD ACTIVE-
4	PULL_UP_330

## AUXILIARY FAN

Pin	Signal Name
1	Ground
2	+12V
3	Ground

## KEYLOCK/POWER LED

Pin	Signal Name
1	Ground
2	KEYLOCK
3	Ground
4	Key
5	PWR LED

## RESET CONNECTOR

Pin	Signal Name
1	Ground
2	RESET

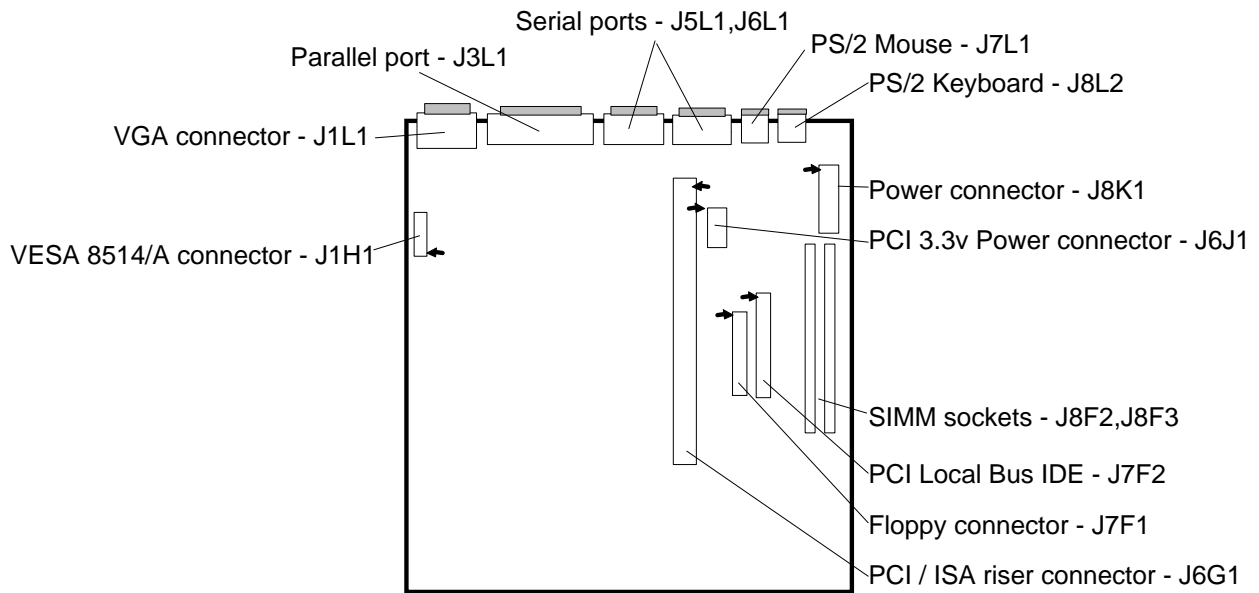


Figure C-2. Baseboard I/O connectors (→ notes Pin 1 locations)

**VESA 8514/A CONNECTOR (J1H1)**

Pin	Signal Name
1,3,5,15,17,19,21,26	Ground
2,4,6,8,10,12,14,16	Data 0:7
7	Data Enable
9	Sync Enable
11	PCLK Enable
18	PCLK
20	BLANK*
13,23	No connect
22	HSYNC
24	VSYNC

**PARALLEL PORT (J3L1)**

Pin	Signal Name	Direction
1	Strobe*	Output
2	Data Bit 0	Bi-Directional
3	Data Bit 1	Bi-Directional
4	Data Bit 2	Bi-Directional
5	Data Bit 3	Bi-Directional
6	Data Bit 4	Bi-Directional
7	Data Bit 5	Bi-Directional
8	Data Bit 6	Bi-Directional
9	Data Bit 7	Bi-Directional
10	ACK*	Input
11	BUSY	Input
12	PE (Paper End)	Input
13	SLCT	Input
14	Auto Feed XT*	Output
15	ERROR*	Input
16	INIT*	Output
17	SLCT IN	Output
18 - 25	Ground	n/a

**VGA CONNECTOR (J1L1)**

Pin	Signal Name
1	Red
2	Green
3	Blue
4	No Connect
5	Ground
6	Ground
7	Ground
8	Ground
9	No Connect
10	Ground
11	No Connect
12	No Connect
13	Horiz. Sync
14	Vertical Sync
15	No Connect

**SERIAL PORTS (J6L1=COM1, J5L1=COM2)**

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	SIN* (Serial Input)
3	SOUT* (Serial Output)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

**PS/2 MOUSE PORT (J7L1)**

Pin	Signal Name
1	Data
2	No Connect
3	Ground
4	Vcc
5	Clock
6	No Connect

**PS/2 KEYBOARD (J8L1)**

Pin	Signal Name
1	Data
2	No Connect
3	Ground
4	Vcc
5	Clock
6	No Connect

**PRIMARY POWER (J8K1)**

Pin	Name	Function
1	PWRGD	Power Good
2	+5 V	+ 5 volts Vcc
3	+12 V	+ 12 volts
4	-12 V	- 12 volts
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	-5 V	-5 volts
10	+5 V	+ 5 volts Vcc
11	+5 V	+ 5 volts Vcc
12	+5 V	+ 5 volts Vcc

**PCI (3.3V) POWER (J6J1)**

Pin	Name	Function
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	+3.3 V	+ 3.3 volts
5	+3.3V	+ 3.3 volts
6	+3.3 V	+ 3.3 volts

**PCI IDE CONNECTOR (J7F2)**

Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ3	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACK3-	29	30	Ground
IRQ14	31	32	IOCS16-
Addr 1	33	34	Ground
Addr 0	35	36	Addr 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground

**FLOPPY CONNECTOR (J7F1)**

Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Key	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable A-
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable B-
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data-
Ground	23	24	Write Gate-
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	Side 1 Select-
Ground	33	34	Diskette

**PCI /ISA RISER CONNECTOR (J6G1)**

Signal Name	Pin Number	Pin Number	Signal Name
IOCHK-	A1	B1	GND
SD7	A2	B2	RSTDRV
SD6	A3	B3	Vcc
SD5	A4	B4	IRQ9
SD4	A5	B5	-5V
SD3	A6	B6	DRQ2
SD2	A7	B7	-12V
SD1	A8	B8	0WS-
SD0	A9	B9	+12V
IOCHRDY	A10	B10	GND
AEN	A11	B11	SMEMW-
SA19	A12	B12	SMEMR-
SA18	A13	B13	IOW-
SA17	A14	B14	IOR-
SA16	A15	B15	DACK3-
SA15	A16	B16	DRQ3
SA14	A17	B17	DACK1-
SA13	A18	B18	DRQ1
SA12	A19	B19	REFRESH-
SA11	A20	B20	SYSCLK
SA10	A21	B21	IRQ7
SA9	A22	B22	IRQ6
SA8	A23	B23	IRQ5
SA7	A24	B24	IRQ4
SA6	A25	B25	IRQ3
SA5	A26	B26	DACK2-
SA4	A27	B27	TC
SA3	A28	B28	BALE
SA2	A29	B29	Vcc
SA1	A30	B30	OSC
SA0	A31	B31	GND
SBHE-	C1	D1	MEMCS16-
LA23	C2	D2	IOCS16-
LA22	C3	D3	IRQ10
LA21	C4	D4	IRQ11
LA20	C5	D5	IRQ12
LA19	C6	D6	IRQ15
LA18	C7	D7	IRQ14
LA17	C8	D8	DACK0-
MEMR-	C9	D9	DRQ0
MEMW-	C10	D10	DACK5-
SD8	C11	D11	DRQ5
SD9	C12	D12	DACK6-
SD10	C13	D13	DRQ6
SD11	C14	D14	DACK7-
SD12	C15	D15	DRQ7
SD13	C16	D16	Vcc
SD14	C17	D17	MASTER-
SD15	C18	D18	GND

Signal Name	Pin Number	Pin Number	Signal Name
GND	E1	F1	GND
GND	E2	F2	GND
PCIINT1-	E3	F3	PCIINT3-
PCIINT2-	E4	F4	PCIINT4-
Vcc	E5	F5	Vcc
Key	E6	F6	Key
Vcc	E7	F7	Vcc
PCIRST-	E8	F8	PCLKF
GNT0-	E9	F9	GND
REQ0-	E10	F10	GNT1-
GND	E11	F11	GND
PCLKE	E12	F12	REQ1-
GND	E13	F13	AD31
AD30	E14	F14	AD29
3.3V	E15	F15	3.3V
Key	E16	F16	Key
3.3V	E17	F17	3.3V
AD28	E18	F18	AD27
AD26	E19	F19	AD25
AD24	E20	F20	CBE3-
AD22	E21	F21	AD23
AD20	E22	F22	AD21
AD18	E23	F23	AD19
3.3V	E24	F24	3.3V
Key	E25	F25	Key
3.3V	E26	F26	3.3V
AD16	E27	F27	AD17
FRAME-	E28	F28	IRDY-
CBE2-	E29	F29	DEVSEL-
TRDY-	E30	F30	PLOCK-
STOP-	E31	F31	PERR-
SDONE	G1	H1	SERR-
SBO-	G2	H2	AD15
CBE1-	G3	H3	AD14
PAR	G4	H4	AD12
GND	G5	H5	GND
Key	G6	H6	Key
GND	G7	H7	GND
AD13	G8	H8	AD10
AD11	G9	H9	AD8
AD9	G10	H10	AD7
CBE0-	G11	H11	AD5
AD6	G12	H12	AD3
AD4	G13	H13	AD1
AD2	G14	H14	AD0
Key	G15	H15	Key
Vcc	G16	H16	Vcc
Vcc	G17	H17	Vcc
GND	G18	H18	GND
GND	G19	H19	GND