



# **Advanced/RH Motherboard Technical Product Specification**

Order Number 281809-007

March 1997

The Advanced/RH motherboard may contain design defects or errors known as errata. Characterized errata that may cause the Advanced/RH motherboard's behavior to deviate from published specifications are documented in the Advanced/RH Motherboard Specification Update.



# Revision History

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Revision	Revision History	Date
-001	Preliminary release of the Advanced/RH Technical Product Specification.	02/96
-002	Production release of the Advanced/RH Technical Product Specification.	04/96
-003	Incorporates Specification Update information through 4/15/96.	05/96
-004	Incorporates Specification Update information through 9/11/96.	10/96
-005	Incorporates minor changes.	02/97
-006	Incorporates Specification Update information through 2/12/97.	03/97
-007	Incorporates minor changes.	03/97

This product specification applies only to standard Advanced/RH motherboards with BIOS identifier 1.00.0x.CV2.

Changes to this specification will be published in the Advanced/RH Motherboard Specification Update before being incorporated into a revision of this document.

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# 1 Motherboard Description

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## 1.1 Overview

The Advanced/RH motherboard supports the following microprocessors:

- Pentium® processors operating at 75, 90, 100, 120, 133, 150, 166, and 200 MHz.
- Pentium processors with MMX™ technology operating at 166 and 200 MHz.

The motherboard features:

- LPX form factor
- Socket 7 Pentium OverDrive® processor socket

Main Memory

- Six 72-pin SIMM<sup>†</sup> sockets
- Support for up to 192 MB of Extended Data Out (EDO) or fast page memory
- Support for non-parity, parity, or ECC DRAM

Second Level Cache Memory

- 256 KB Pipeline Burst SRAM soldered to the motherboard
- CELP (Card Edge Low Profile) socket for 256 KB or 512 KB COAS<sup>t</sup> (Cache On A Stick) modules (available only if there is no cache soldered to the motherboard)

Chipset and PCI/IDE Interface

- Intel 82430HX PCISet
- Integrated PCI bus mastering controller
- Two fast IDE interfaces with support for up to four IDE drives or devices

I/O Features

- PC87306B Super I/O controller
- Integrates standard I/O functions: floppy drive interface, one multi-mode parallel port, two FIFO serial ports, real-time clock, keyboard and mouse controller, IrDA<sup>†</sup>-compatible interface

Expansion Slots

- Riser board options support a total of five slots (ISA/PCI)
- Two or three PCI-slot riser boards supported (jumper change required)

Audio Subsystem

- Creative Labs Vibra16 audio codec
- Telephony and CD-ROM upgrade headers, and back panel audio jacks

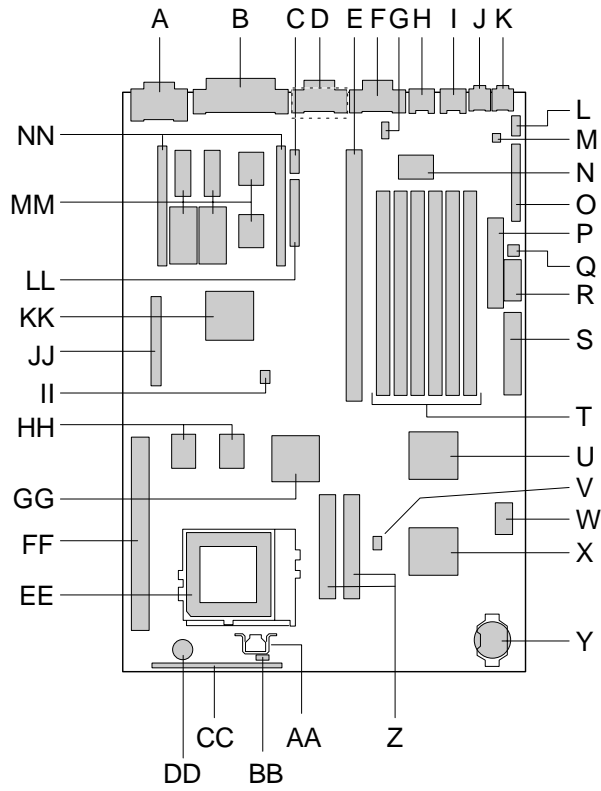
Graphics Subsystem

- ATI<sup>†</sup>-264 VT graphics controller
- VESA<sup>†</sup>/ATI multimedia channel connector
- Video memory expansion headers

Other features

- Plug and Play compatible
- Support for Advanced Power Management

Software drivers and utilities are available on Intel's FTP and World Wide Web sites (see Section 5.2).



OM05630

Figure 1. Motherboard Components

**Table 1. Motherboard Component Locations**

A	Optional VGA† connector	O	Optional MIDI Audio/Joystick connector	CC	Front panel connector
B	Parallel port connector	P	Floppy connector	DD	Onboard speaker
C	Serial 2 header	Q	Soft-OFF connector	EE	Socket 7 Pentium processor socket
D	Serial 2, or optional dual USB connector	R	3.3v power connector	FF	Optional CELP module socket
E	PCI / ISA riser connector	S	Primary power connector	GG	82439HX controller (TXC)
F	Serial 1 connector	T	Six SIMM sockets (three banks)	HH	Optional 256K L2 PBRAM
G	Optional four-pin CD-ROM audio connector	U	National PC87306B I/O controller	II	Riser Card 2/3 slot jumper
H	PS/2† Mouse port	V	BIOS Recovery and VR/VRE jumper	JJ	Optional VESA/AMC connector
I	PS/2 Keyboard port	W	Flash BIOS	KK	Optional ATI graphics controller
J	Optional Mic-In 3.5 mm audio jack	X	PCI ISA/IDE Xcelerator (PIIX3)	LL	Configuration jumper blocks
K	Optional Audio Out 3.5 mm audio jack	Y	Battery for real-time clock	MM	Optional graphics memory
L	Site for optional Wavetable connector	Z	Two PCI IDE interfaces	NN	Optional SGRAM graphics memory upgrade connectors
M	Optional Telephony connector	AA	Voltage regulator		
N	Optional Creative Labs Vibra† 16C audio codec	BB	Optional keylock header		

## 1.2 Motherboard Manufacturing Options

- Second level cache (L2)
  - 256 KB Pipeline Burst SRAM soldered to the motherboard
  - CELP socket for COASSt modules
- Audio support based on the Creative Labs Vibra16 audio codec
- ATI-264VT graphics subsystem with 1 MB SGRAM onboard
- Support for Universal Serial Bus (USB)
- Keylock header

## 1.3 Form Factor

The motherboard is designed to fit into a standard LPX form factor chassis. Figure 2 illustrates the mechanical form factor for the motherboard. Location of the I/O connectors, riser slot, and mounting holes are in strict compliance with the LPX specification.

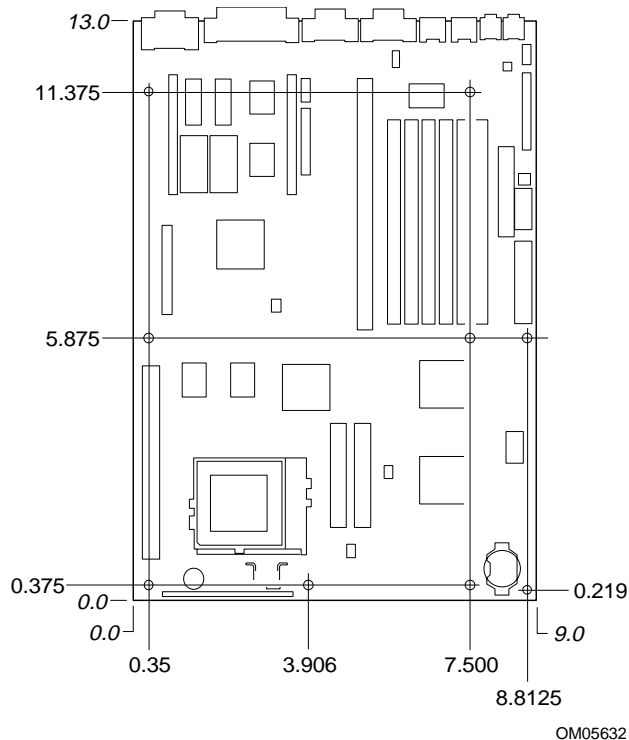


Figure 2. Motherboard Dimensions

## 1.4 Microprocessor

The motherboard supports:

- Pentium processors operating at 75, 90, 100, 120, 133, 150, 166, and 200 MHz
- Pentium processors with MMX technology operating at 166 and 200 MHz

### ⇒ NOTE

*Support for Pentium processors with MMX technology is available only on boards that have a voltage regulator (with a heatsink) next to the processor socket and USB connectors on the back panel. See the Advanced/RH Motherboard Specification Update for more information.*

An onboard voltage regulator derives the necessary voltage from the system power supply. An onboard jumper enables use of standard, VR-, or VRE-specified processors.

The Pentium microprocessor has an advanced numeric coprocessor that maintains full backward compatibility with math coprocessors and complies with ANSI/IEEE standard 754-1985.



### CAUTION

*If you use clips to secure a heat sink to the processor, do not use bail-wire style heat sink clips. These clips have been known to damage the motherboard when installed or removed incorrectly.*

## 1.4.1 Microprocessor Upgrade

The motherboard has a 321-pin Socket 7 zero insertion force (ZIF) microprocessor socket. Socket 7 supports upgrades to higher performance Pentium OverDrive processors not supported by Socket 5.

## 1.5 Memory

### 1.5.1 Main Memory

The motherboard has six SIMM sockets arranged in three banks: Bank 0, Bank 1, and Bank 2. Each bank has two sockets. SIMMs in the same bank must be the same type, size, and speed; SIMMs in different banks may differ in type, size, and speed. SIMMs must be installed in both sockets of a bank, and at least one bank must be filled. The BIOS automatically detects memory type and size so no jumper settings are required.

The motherboard supports the following:

- 72-pin SIMMs with tin-lead contacts
- Non-parity or parity SIMMs
- ECC SIMMs, when enabled as part of the BIOS setup
- Single- or double-sided SIMMs in the sizes listed in Table 2
- 70 ns fast page mode and 60 or 70 ns extended data out (EDO) SIMMs

#### ⇒ **NOTE**

*EDO SIMMs (70 ns modules) are not supported for 66 MHz host bus speeds*

**Table 2. SIMM Sizes**

SIMM Size	Non-parity Configuration	Parity Configuration
2 MB (fast page/EDO)*	512K x 32	512K x 36
4 MB (fast page/EDO)	1M x 32	1M x 36
8 MB (fast page/EDO)	2M x 32	2M x 36
16 MB (fast page/EDO)	4M x 32	4M x 36
32 MB (fast page/EDO)**	8M x 32	8M x 36

\* 512K x 32 and 512K x 36 SIMMs are supported, but they must be double-sided SIMMs.

\*\* Single-sided, high-density 32 MB SIMM modules are not recognized by the system.

#### 1.5.1.1 EDO DRAM

EDO DRAM improves memory read performance by holding the memory data valid until the next CAS# falling edge unlike fast page mode DRAM, which tri-states the memory data when CAS# negates to precharge for the next memory cycle. With EDO DRAM, the CAS# precharge overlaps the data-valid time, which allows CAS# to negate earlier while still satisfying the memory data-valid window.

### 1.5.1.2 Parity/ECC DRAM

Memory error checking and correction is supported by parity memory. With parity memory, the motherboard can be configured to support Error Checking and Correcting (ECC) memory operation. Parity SIMMs are automatically detected, but you must enter Setup to configure the memory for either Parity or ECC operation. Parity memory detects single-bit errors. ECC memory detects double-bit errors and corrects single-bit errors. Errors might be generated by a defective memory module, by different speeds of memory modules, or by DMA or memory conflicts.

## 1.5.2 Second Level Cache

The motherboard has two manufacturing options for second level (L2) cache memory:

- 256 KB direct-mapped write-back cache contained in two global write enable (GWE) Pipeline Burst SRAM (PBSRAM) devices soldered to the motherboard.
- Type 3 Card Edge Low Profile (CELP) socket conforming to Intel's COASSt 3.0 specification (see Section 5.1). The CELP socket can accept either 256 KB or 512 KB cache memory modules. The CELP socket is not available and is not stuffed if the 256 KB PBSRAM cache is soldered to the motherboard.

### ⇒ NOTE

*A 5 volt 8 KB x 8 external Tag SRAM provides caching support for up to 64 MB of main memory. If more main memory is installed, performance might suffer because memory above the first 64 MB of main memory does not have cache support.*

## 1.6 Chipset

The Intel 82430HX PCIsset consists of the 82439HX Xcelerated Controller (TXC) and one 82371SB PCI/ISA IDE Xcelerator (PIIX3) bridge chip.

### 1.6.1 82439HX Xcelerated Controller (TXC)

The 82439HX provides all control signals necessary to drive second level cache and main memory including multiplexed address signals. The TXC also controls system access to memory and generates snoop controls to maintain cache coherency. The TXC comes in a 324-pin BGA package that features:

- Microprocessor interface control
- Integrated L2 write-back cache controller
  - Pipeline Burst SRAM
  - 256 or 512 KB direct-mapped
- Integrated DRAM controller
  - 64-bit path to memory
  - EDO and fast page DRAM support
  - Parity, ECC, and non-parity support

- Fully synchronous PCI bus interface
  - 25, 30, and 33 MHz bus speeds
  - PCI to DRAM data throughput at greater than 100 MB per second
  - Up to four PCI masters in addition to the PIIX3

### 1.6.2 82371SB PCI/ISA IDE Xcelerator (PIIX3)

The PIIX3 is the interface between the PCI and ISA buses. It features an integrated dual-channel enhanced IDE interface that supports up to four IDE devices. The PIIX3 comes in a 208-pin QFP package that features:

- PCI and ISA bus interface
- Universal Serial Bus (USB) controller
  - Host/hub controller
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 16 MB per second
  - Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers
  - Bus master mode
- PCI 2.1 compliance
- Enhanced DMA controller supporting up to seven DMA channels
- Interrupt controller with PCI-to-ISA interrupt mapping circuitry
- 16-bit counters/timers
- SMI interrupt logic and timer with fast on/off mode
- NMI circuitry

### 1.6.3 Universal Serial Bus (USB) Support

There is a manufacturing option to provide two USB ports. The USB ports take the place of serial port 2. A header is provided for serial port 2 at location J4M1. The ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The motherboard fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible. Features of the USB include:

- Self-identifying, hot pluggable peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol

#### ⇒ **NOTE**

*Computer systems that have an unshielded cable attached to the USB port might not meet FCC Class B requirements, even if no device or a low-speed (sub-channel) SUB device is attached to the cable. Use shielded cable that meets the requirements for high-speed (fully rated) devices..*

## 1.6.4 IDE SUPPORT

The motherboard has two independent bus mastering PCI IDE interfaces that support PIO Mode 3, PIO Mode 4, and ATAPI (e.g., CD-ROM) devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. IDE device transfer rate and translation mode are automatically detected by the BIOS.

Normally, programmed I/O operations require a substantial amount of processor bandwidth; however, in true multi-tasking operating systems like Windows<sup>†</sup> 95, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

## 1.7 Super I/O Controller

The PC87306B Super I/O Controller from National Semiconductor provides:

- Serial ports: two NS16C550-compatible UARTs with send/receive 16-byte FIFO
- Multimode bidirectional parallel port
  - Standard mode, IBM<sup>†</sup> and Centronics<sup>†</sup> compatible
  - Enhanced Parallel Port (EPP) mode with BIOS and driver support
  - High-speed Extended Capabilities Port (ECP) mode
- Industry standard floppy controller with 16-byte FIFO and 2.88 MB floppy drive support
- 8042-compatible keyboard controller
- Real-time clock accurate within  $\pm 13$  minutes a year at 25 °C and 5V
- Support for an IrDA-compliant infrared interface

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program.

### 1.7.1 Serial Ports

The motherboard has one and optionally (if the USB option is not installed) two 9-pin D-Sub serial port connectors located on the back panel. The NS16C550-compatible UARTs support data transfers at speeds up to 115K bits/second.

### 1.7.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel of the motherboard. In the Setup program, there are four options for parallel port operation:

- Compatible (standard mode)
- Bidirectional (PS/2 compatible)
- Bidirectional Enhanced Parallel Port (EPP). A driver from the peripheral manufacturer is required for operation. See Section 5.1 for EPP compatibility (current BIOS version supports compliance with EPP version 1.7)
- Bidirectional high-speed Extended Capabilities Port (ECP)

### 1.7.3 Floppy Controller

The I/O controller is software compatible with the DP8473 and 82077 floppy drive controllers. In the Setup program, the floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch (driver required)
- 1.2 MB, 3.5-inch
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

### 1.7.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel of the motherboard. The 5 V lines to these connectors are protected with a PolySwitch<sup>†</sup> circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, power to the computer should be turned off before connecting or disconnecting a keyboard or mouse.

#### ⇒ **NOTE**

*You can plug the mouse and keyboard into either connector.*

The keyboard controller contains the AMI Megakey keyboard and mouse controller code, which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the Setup program.

The keyboard controller also supports the following hot-key sequences:

- <CTRL><ALT><DEL> Software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power On Self Test (POST).
- <CTRL><ALT><+> and <CTRL><ALT><-> Turbo mode. Note that Turbo mode could be affected by the operating system, or whether the processor is in protected mode or virtual x86 mode.
  - <CTRL><ALT><-> For Deturbo mode
  - <CTRL><ALT><+> For Turbo mode
- <CTRL><ALT><defined in Setup>: Power management. This key sequence invokes power managed mode, which reduces the computer's power consumption while maintaining its ability to service external interrupts.
- <CTRL><ALT><defined in Setup>: Keyboard lock. This key sequence is a security feature that locks the keyboard until the User password is entered. When keyboard lock is invoked, the keyboard LEDs flash. To enable the keyboard lock feature, a User password must be specified in the Setup program.

## 1.7.5 Real-time Clock, CMOS RAM and Battery

The real-time clock is compatible with DS1287 and MC146818 components. It provides a time-of-day clock and a 100-year calendar with alarm features and century rollover. The real-time clock also supports 242-bytes of battery-backed CMOS RAM in two banks, which are reserved for BIOS use.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program or by setting a configuration jumper on the motherboard.

An external coin-cell battery powers the real-time clock and CMOS memory. If the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 5 volt standby current from the motherboard's power supply extends the life of the battery. The RTC is accurate to  $\pm 13$  minutes/year at 25 °C and 5V conditions.

## 1.7.6 Infrared Support

The motherboard has a 5-pin header that supports Hewlett Packard<sup>†</sup> HSDL-1000 compatible infrared (IR) transmitters/receivers. In the Setup program, Serial Port 2 can be directed to a connected IR device. The connection can be used to transfer files to or from portable devices like laptops, PDAs and printers. The Infrared Data Association (IrDA) specification supports data transfers of 115 Kbps at a distance of 1 meter.

### 1.7.6.1 Consumer Infrared Support

The motherboard has a signal pin that supports Consumer Infrared (IR) devices (remote controls). The signal pin supports receive only. Consumer IR devices can be used to control telephony functions and multimedia operations like volume and CD track changes. A software and hardware interface is needed to use this feature.

## 1.8 Graphics Subsystem

The optional onboard graphics subsystem uses the ATI-264VT graphics controller. The ATI-264VT graphics controller has the following features:

- Drawing coprocessor that operates concurrently with the host processor
- Video coprocessor that enables simultaneous display of 24 bits per pixel (bpp) video and 8 bpp graphics
- VGA and VESA compatibility
- PCI compliance
- Support for power management
- Support for VESA Display Data Channel (DDC2B)
- Video scaler, color space converter, true color palette
- Triple-clock synthesizer
- Support for ATI multimedia channel (AMC) connector

## 1.8.1 Memory Type and Size

The first of the following video memory options are available soldered onto the motherboard. For information on graphics memory upgrade modules, contact ATI Technologies.

- SGRAM: 1 MB
- Graphic memory upgrade module. This module (available from ATI) allows expansion to a maximum of 4 MB total video memory. Earlier versions of the Advanced/RH motherboard were able to support a maximum of 2 MB total video memory.

## 1.8.2 Resolutions and Refresh Rates

**Table 3. ATI-264VT Maximum Resolutions and Refresh Rates**

1 MB Memory		Refresh Rate (Hz) at:			
Resolution	4-bit Color	8-bit Color	16-bit Color	24-bit Color	
640 x 480	120	120	120	75	
800 x 600	120	120	75	not supported	
1024 x 768	120	120	not supported		not supported
1152 x 864	60	60	not supported		not supported
1280 x 1024	47	not supported		not supported	
2 MB Memory		Refresh Rate (Hz) at:			
Resolution	4-bit Color	8-bit Color	16-bit Color	24-bit Color	
640 x 480	120	120	120	100	
800 x 600	120	120	75	70	
1024 x 768	120	120	100	not supported	
1152 x 864	85	85	43, interlaced	not supported	
1280 x 1024	75	75	not supported		not supported
4 MB Memory		Refresh Rate (Hz) at:			
Resolution	4-bit Color	8-bit Color	16-bit Color	24-bit Color	
640 x 480	120	120	120	100	
800 x 600	120	120	75	70	
1024 x 768	120	120	100	75	
1152 x 864	85	85	43, interlaced	43, interlaced	
1280 x 1024	75	75	75	75	

### 1.8.3 VESA/ATI Multimedia Channel Connector

The motherboard has a 40-pin ATI multimedia channel (AMC) connector. This feature connector serves dual functions and includes:

- A 26-pin VESA feature connector
- A section with 12 pins for the ATI Enhanced Visual Architecture bus.

#### 1.8.3.1 VESA Connector

The 26-pin VESA feature connector is used for synchronizing graphics output with an external NTSC or PAL signal. The connector features a shared frame buffer interface and a Local Peripheral Bus (LPB) with a bidirectional interface that supports video companion devices like MPEG/live video decoders.

#### 1.8.3.2 ATI Multimedia Channel (AMC) Connector

The AMC section of the connector uses 12 pins for the ATI Enhanced Visual Architecture bus. The connector features a shared frame buffer interface and a Local Peripheral Bus (LPB) with a bidirectional interface that supports video companion devices like MPEG/live video decoders.

### 1.8.4 Graphics Drivers and Utilities

Graphics drivers and common graphics utilities are available for OS/2<sup>†</sup> 2.11 and OS/2 WARP, Windows 3.x, Windows 95, and Windows NT<sup>†</sup>. Graphic drivers and utilities are available on Intel's FTP and World Wide Web sites (see Section 5.2).

## 1.9 Audio Subsystem

The optional onboard audio subsystem features the Creative Labs Vibra 16S codec (early versions of the Advanced/RH motherboard), or the Creative Labs Vibra 16C codec. It provides all the digital audio and analog mixing functions needed for recording and playing sound on personal computers.

#### ⇒ **NOTE**

The Advanced/RH motherboard audio subsystem might use either the Creative Labs Vibra 16S audio codec (early versions of the motherboard) or the 16C audio codec. The text of this section describes both devices where the two versions of the codec differ.

The Vibra 16S features the following:

- Analog mixing of six audio sources
  - Digital audio (stereo)
  - CD audio (stereo)
  - Synthesized music (stereo)
  - Line level audio (stereo)
  - Microphone level audio (mono)
  - PC speaker (mono)
- Individual software programmable volume controls

- Mixer controlled recording and source selection
- Automatic Gain Control with amplifier or fixed gain amplifier for microphone level audio
- Dynamic filtering for digital audio recording and playback
- 8- or 16-bit stereo/mono digital audio playback and recording
- FIFOs for digital audio playback and recording
- Variable sampling rates from 5 KHz to 44.1 KHz
- Built-in analog joystick quad timer
- Sound Blaster<sup>†</sup> Pro compatible
- Full-duplex operation
- Power management mode

The Vibra 16C has the following features in addition to those provided by the Vibra 16S:

- 8-level volume control mixer
- Integrated FM synthesizer
- Adlib, Sound Blaster 16, Sound Blaster Pro, and MPU-401 compatibility
- MPC and MPCII compliance
- Plug and Play support

The audio subsystem requires one IRQ and up to two DMA channels. For full duplex operation, the audio subsystem requires two DMA channels (one 16-bit channel and one 8-bit channel). The following table shows the IRQ, DMA channel, and base I/O address options for the Vibra 16S version of the audio subsystem.

**Table 4. Vibra 16S IRQ Options**

Device	IRQ (Options)	DMA Channel (Options)	I/O Address (Options)
Creative Labs Vibra 16S	5 (default)	1 (8 bit, default)	220h-22Fh (default)
	7	3 (8 bit)	240h-24Fh
	9	5 (16 bit, default)	260h-26Fh
	10	7 (16 bit)	280h-28Fh
FM Synthesis (fixed)			388h-38Bh

The following table shows the IRQ, DMA channel, and base I/O address options for the Vibra 16C version of the audio subsystem.

**Table 5. Vibra 16C IRQ Options**

Device	IRQ (Options)	DMA Channel (Options)	I/O Address (Options)
Creative Labs 16C Base	5 (default) 7 10	1 (8 bit, default) 3 (8 bit) 5 (16 bit, default) 7 (16 bit)	220h-233h (default) 240h-253h 260h-273h 280h-293h
FM Synthesis			388h-38Bh
Joystick (MIDI port)			200h-207h
MPU-401			300h-301h 330h-331h (default)

### 1.9.1 Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 5.2).

### 1.9.2 CD-ROM Audio Connector

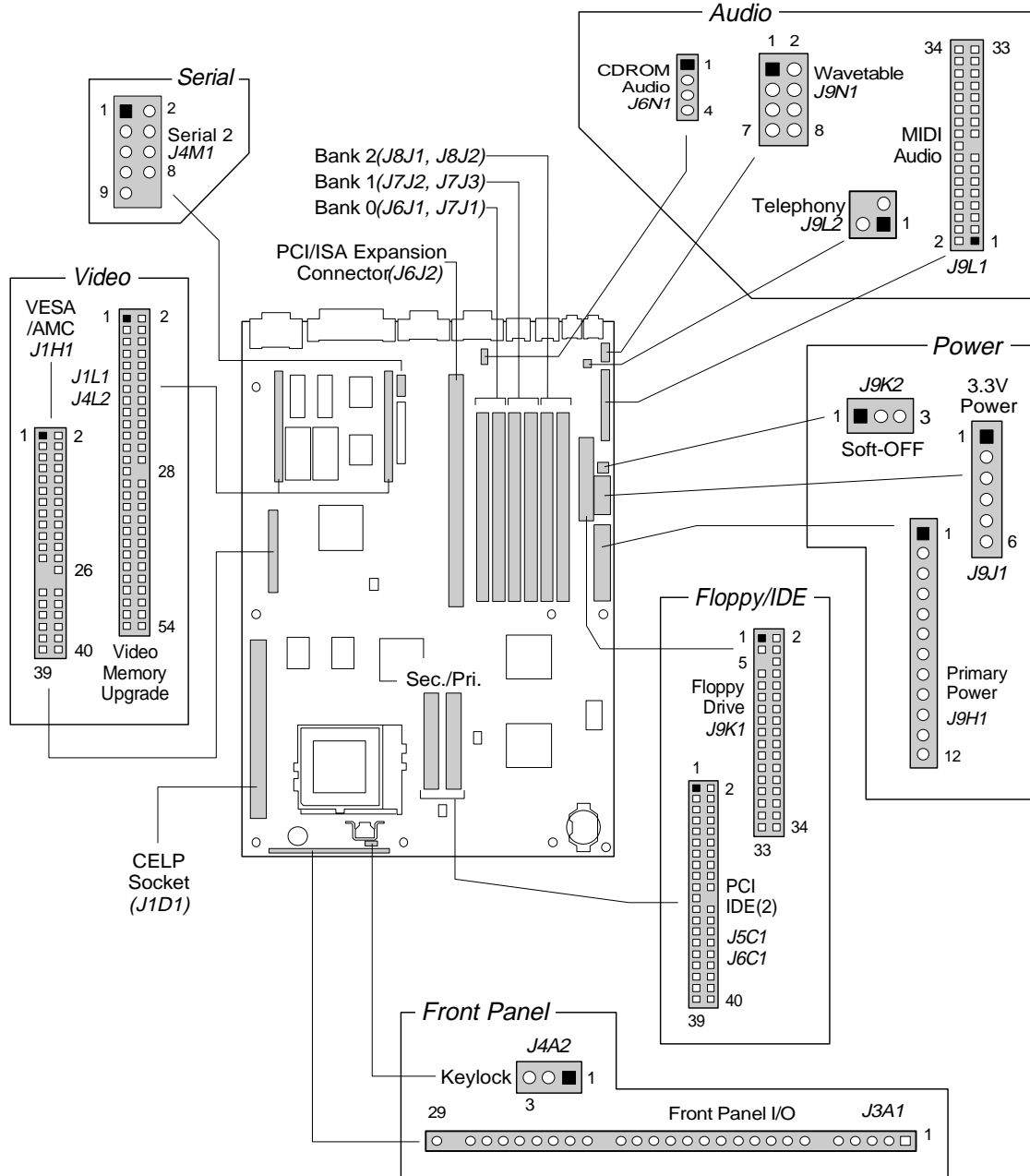
A 1x4-pin connector is available for connecting an internal CD-ROM reader to the audio subsystem's mixer. The connector is compatible with most cables supplied with ATAPI CD-ROM readers designed to connect to audio add-in cards.

### 1.9.3 Telephony Connector

A 2x2-pin connector is available for connecting the monaural audio signals of an internal telephony device such as a fax/modem to the motherboard's audio subsection. The mono-in and mono-out signal interface is necessary for telephony applications such as speakerphones and answering machines.

## 1.10 Motherboard Connectors

The following figure shows the connectors on the motherboard.



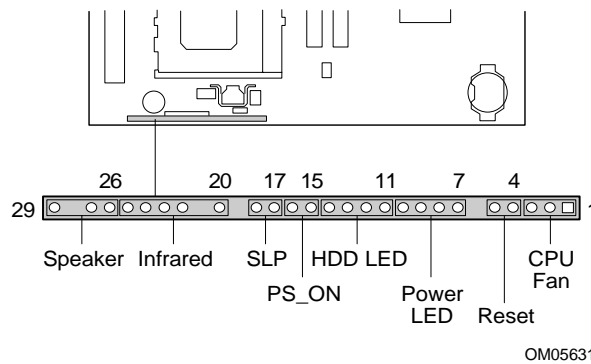
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Figure 3. Motherboard Connectors

### 1.10.1 Front Panel Connectors

The motherboard provides header connectors to support functions typically located on the chassis bezel. Figure 4 shows the front panel connector header. Front panel features supported include:

- CPU fan (FAN)
- System Reset (RST)
- Power LED (PWRLLED)
- Hard drive activity LED (HDDLED)
- Power supply ON (PS-ON)
- Sleep/Resume (SLP)
- Infrared (IrDA) port (IR)
- System Speaker (SPKR)



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**Figure 4. Front Panel I/O Connectors**

Table 6 lists the pinouts and signals for the front panel I/O connector.

**Table 6. Front Panel I/O Connector (J3A1)**

Pin	Signal Name	Pin	Signal Name
1	FANNEG	16	Ground
2	FANPOS	17	SLEEP
3	FANNEG	18	SLEPPU
4	Ground	19	Key, No connection
5	SW_RST	20	VCC
6	Key, No connection	21	No connection
7	PWR_PU	22	IRRIN
8	PWR_PU	23	Ground
9	PWR_LED_DRV	24	IRTX
10	PWR_LED_DRV	25	CONIR
11	HDD_PU	26	SPKR+
12	HDA#	27	SPKRHDR
13	PWR_LED_DRV	28	Key, No connection
14	PWR_PU	29	Ground
15	PS_ON		

#### 1.10.1.1 CPU Fan (FAN)

The 3-pin fan header of the front panel connector provides a basic 3-wire connection to a CPU fan. The center pin of the header supplies +12 VDC and the outer pins are at ground.

#### 1.10.1.2 System Reset (RST)

Connect this header to a momentary SPST type switch that is normally open. When the switch is closed, the board resets and runs the POST.

#### 1.10.1.3 Sleep/Power LED (PWRLED)

Connect this header to an LED that will light when the computer is powered on. This LED will also blink when the computer is in a power-managed state.

#### 1.10.1.4 Hard Drive Activity LED (HDDLED)

Connect this header to an LED to provide a visual indicator that data is being read from or written to an IDE hard drive. For the LED to function properly, the IDE drive must be connected to the onboard IDE controller on the motherboard.

#### 1.10.1.5 Power Supply ON (PS\_ON)

To support soft off connect this header to a power switch which could be placed on the front panel. A momentary ground must be applied to the PS\_ON pin to signal the supply to turn on or off. This requirement would normally be satisfied by using a SPST normally open momentary contact switch. Because of the motherboard's internal debounce circuitry, the ground must be applied for at least 50 ms. To prevent double-clicking, at least two seconds must pass before the power supply will recognize another on/off signal.

#### 1.10.1.6 Sleep/Resume (SLP)

When advanced power management (APM) is enabled in the system BIOS and the operating system's APM driver is loaded, the system can enter Sleep (Standby) mode in one of three ways:

- Optional front panel Sleep/Resume button
- Hot key defined in the BIOS Setup program
- Prolonged system inactivity; the default timeout is 10 minutes and can be changed in Setup

A Sleep/Resume button is supported by the 2-pin header located on the front panel I/O connector. The front panel Sleep/Resume switch must be a momentary SPST type that is normally open.

Closing the Sleep/Resume switch generates a System Management Interrupt (SMI) to the processor, which immediately goes into System Management Mode (SMM). While the system is in Sleep mode it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate the system, or Resume, you must press the Sleep/Resume button again, or use the keyboard or mouse.

#### 1.10.1.7 Infrared (IrDA) Connector (IR)

Serial Port 2 can be configured to support an IrDA module connected to this 6-pin header. After configuring the IrDA interface, you can transfer files to or from portable devices such as laptops, PDAs and printers using application software.

#### 1.10.1.8 Speaker (SPKR)

A speaker may be installed on the motherboard as a manufacturing option. The speaker provides error beep code information during the Power-On Self Test (POST) if the computer cannot use the video interface. The speaker is not connected to the audio subsystem, and does not receive output from the audio subsystem.

### 1.10.1.9 Keylock Header

In addition to the front panel I/O connector, an optional keylock header provides a means to lock the keyboard controller. This 3-pin header can be connected to a keyswitch that is normally open. When the keyswitch is closed, the system keyboard will be locked. Table 7 lists the signals for the keylock header.

**Table 7. Keylock Header (J4A2)**

Pin	Signal Name
1	Ground
2	KBLOCK#
3	Ground

### 1.10.2 Memory/Expansion Connectors

The Advanced/RH motherboard provides six 72-pin SIMM sockets for main memory. These sockets accept standard SIMM 72-pin modules, as long as they satisfy the requirements described in the “Main Memory” section of this specification, starting on page 13.

The Advanced/RH motherboard either has 256 KB of PBSRAM cache memory soldered to the motherboard or a CELP socket that supports L2 cache. Table 9 lists the pinout and signals for the optional CELP connector.

The Advanced/RH motherboard uses a PCI/ISA riser connector (J6J2) to provide for expansion PCI or ISA boards. The associated riser board can be a 5-slot ISA riser, or a PCI/ISA riser with either two or three PCI slots. A pair of jumpers on the Advanced/RH motherboard must be set to define the number of PCI slots on the riser board. Refer to Figure 6 on page 40 for jumper block details. Table 8 contains the pinout listing for the PCI/ISA riser connector.

#### ⇒ **NOTE**

*Use a low-profile heatsink on the processor. This provides clearance for a full-length card in the bottom ISA slot of the riser card.*

**Table 8. PCI/ISA Riser Connector (J6J2)**

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	IOCHK#	B1	GND	E1	GND	F1	GND
A2	SD7	B2	RSTDRV	E2	GND	F2	GND
A3	SD6	B3	Vcc	E3	PCIINTA#	F3	PCIINTC#
A4	SD5	B4	IRQ9	E4	PCIINTB#	F4	PCIINTD#
A5	SD4	B5	-5 V	E5	Vcc	F5	Vcc
A6	SD3	B6	DRQ2	E6	Key	F6	Key
A7	SD2	B7	-12 V	E7	Vcc	F7	Vcc
A8	SD1	B8	0WS#	E8	PCIRST#	F8	PCKLF
A9	SD0	B9	+12 V	E9	GNT0#	F9	GND
A10	IOCHRDY	B10	GND	E10	REQ0#	F10	GNT1#
A11	AEN	B11	SMEMW#	E11	GND	F11	GND
A12	SA19	B12	SMEMR#	E12	PCKLE	F12	REQ1#
A13	SA18	B13	IOW#	E13	GND	F13	AD31
A14	SA17	B14	IOR#	E14	AD30	F14	AD29
A15	SA16	B15	DACK3#	E15	3.3 V	F15	3.3 V
A16	SA15	B16	DRQ3	E16	Key	F16	Key
A17	SA14	B17	DACK1#	E17	3.3 V	F17	3.3 V
A18	SA13	B18	DRQ1	E18	AD28	F18	AD27
A19	SA12	B19	REFRESH#	E19	AD26	F19	AD25
A20	SA11	B20	SYSCLK	E20	AD24	F20	CBE3#
A21	SA10	B21	IRQ7	E21	AD22	F21	AD23
A22	SA9	B22	IRQ6	E22	AD20	F22	AD21
A23	SA8	B23	IRQ5	E23	AD18	F23	AD19
A24	SA7	B24	IRQ4	E24	3.3 V	F24	3.3 V
A25	SA6	B25	IRQ3	E25	Key	F25	Key
A26	SA5	B26	DACK2#	E26	3.3 V	F26	3.3 V
A27	SA4	B27	TC	E27	AD16	F27	AD17
A28	SA3	B28	BALE	E28	FRAME#	F28	IRDY#
A29	SA2	B29	Vcc	E29	CBE2#	F29	DEVSEL#
A30	SA1	B30	OSC	E30	TRDY#	F30	PLOCK#
A31	SA0	B31	GND	E31	STOP#	F31	PERR#
C1	SBHE#	D1	MEMCS16#	G1	SDONE	H1	SERR#
C2	LA23	D2	IOCS16#	G2	SBO#	H2	AD15
C3	LA22	D3	IRQ10	G3	CBE1#	H3	AD14
C4	LA21	D4	IRQ11	G4	PAR	H4	AD12
C5	LA20	D5	IRQ12	G5	GND	H5	GND
C6	LA19	D6	IRQ15	G6	Key	H6	Key

continued ➡

**Table 8. PCI/ISA Riser Connector (J6J2) (continued)**

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
C7	LA18	D7	IRQ14	G7	GND	H7	GND
C8	LA17	D8	DACK0#	G8	AD13	H8	AD10
C9	MEMR#	D9	DRQ0	G9	AD11	H9	AD8
C10	MEMW#	D10	DACK5#	G10	AD9	H10	AD7
C11	SD8	D11	DRQ5	G11	CBE0#	H11	AD5
C12	SD9	D12	DACK6#	G12	AD6	H12	AD3
C13	SD10	D13	DRQ6	G13	AD4	H13	AD1
C14	SD11	D14	DACK7#	G14	AD2	H14	AD0
C15	SD12	D15	DRQ7	G15	Key	H15	Key
C16	SD13	D16	Vcc	G16	Vcc	H16	Vcc
C17	SD14	D17	MASTER#	G17	GNT2	H17	Vcc
C18	SD15	D18	GND	G18	(GND   REQ2) *	H18	(GND   PCCLK2) *
				G19	GND	H19	GND

\* These signals are (2 slot | 3 slot) jumpered signal names.

**Table 9. CELP Connector for L2 Cache (J1D1)**

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	Ground	41	D58	81	Ground	121	D59
2	TIO0	42	D56	82	TIO1	122	D57
3	TIO2	43	Ground	83	TIO7	123	Ground
4	TIO6	44	D54	84	TIO5	124	D55
5	TIO4	45	D52	85	TIO3	125	D53
6	TIO8	46	D50	86	TIO9	126	D51
7	VCC3	47	D48	87	VCC5	127	D49
8	TWE#	48	Ground	88	TIO10	128	Ground
9	CADS#/CAA3	49	D46	89	CADV#/CAA4	129	D47
10	Ground	50	D44	90	Ground	130	D45
11	CWE4#	51	D42	91	COE#	131	D43
12	CWE6#	52	VCC3	92	CWE5#	132	VCC5
13	CWE0#	53	D40	93	CWE7#	133	D41
14	CWE2#	54	D38	94	CWE1#	134	D39
15	VCC3	55	D36	95	VCC5	135	D37
16	CCS#/CAB4	56	Ground	96	CWE3#	136	Ground
17	GWE#	57	D34	97	CAB3	137	D35
18	BWE#	58	D32	98	CALE	138	D33
19	Ground	59	D30	99	Ground	139	D31
20	A3	60	VCC3	100	RSVD	140	VCC5

continued ➡

**Table 9. CELP Connector for L2 Cache (J1D1)** (continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
21	A7	61	D28	101	A4	141	D29
22	A5	62	D26	102	A6	142	D27
23	A11	63	D24	103	A8	143	D25
24	A16	64	Ground	104	A10	144	Ground
25	VCC3	65	D22	105	VCC5	145	D23
26	A18	66	D20	106	A17	146	D21
27	Ground	67	D18	107	Ground	147	D19
28	A12	68	VCC3	108	A9	148	VCC5
29	A13	69	D16	109	A14	149	D17
30	ADSP#	70	D14	110	A15	150	D15
31	ECS1#/(CS#)	71	D12	111	RSVD	151	D13
32	ECS2#	72	Ground	112	PD0	152	Ground
33	PD1	73	D10	113	PD2	153	D11
34	PD3	74	D8	114	PD4	154	D9
35	Ground	75	D6	115	Ground	155	D7
36	CLK1	76	VCC3	116	CLK0	156	VCC5
37	Ground	77	D4	117	Ground	157	D5
38	D62	78	D2	118	D63	158	D3
39	VCC3	79	D0	119	VCC5	159	D1
40	D60	80	Ground	120	D61	160	Ground

### 1.10.3 Audio Connectors

The pinouts and signal listings for the audio headers/connectors are provided in the following tables.

**Table 10. CD-Audio Header (J6N1)**

Pin	Signal Name
1	Ground
2	CD-Left
3	Ground
4	CD-Right

**Table 11. Wavetable Header (J9N1)**

Pin	Signal Name
1	Wave Right
2	Ground
3	Wave Left
4	Ground
5	Key
6	Ground
7	MIDI_WR
8	MIDI_OUT

**Table 12. Telephony Header (J9L2)**

Pin	Signal Name
1	Ground
2	Mono Out
3	Mic In
4	Key

**Table 13. MIDI/Audio Upgrade Header (J9L1)**

Pin	Signal Name	Pin	Signal Name
1	+5 V	2	+5 V
3	Joystick Button0	4	Joystick Button2
5	Joystick X1	6	Joystick X2
7	Ground	8	MIDI Out
9	Ground	10	Joystick Y2
11	Joystick Y1	12	Joystick Button3
13	Joystick Button1	14	MIDI In
15	+5 V	16	Key
17	Key	18	Key
19	Line Out Right	20	Ground
21	Right Speaker	22	Ground
23	Left Speaker	24	Key
25	Line Out Left	26	Ground
27	Line In Right	28	-12 V
29	Line In Left	30	Ground
31	Mic In	32	+12 V
33	Ground	34	Ground

## 1.10.4 Power Connectors

The Advanced/RH motherboard can be used with a power supply that supports remote power on/off, so the motherboard can turn off the system power under software control. The Powerman utility supplied for Windows 3.1x allows for soft-off as does the shutdown icon in Windows 95 Start menu. The system BIOS turns the system power off when it receives the proper APM command from the OS. For example, Windows 95 issues this APM command after the user selects “Shutdown the computer” option. APM must be enabled in the system BIOS and OS in order for the soft-off feature to work correctly. The user has the ability to determine the state of the power supply, so if the system was turned on when power was disconnected, the system turns back on when power is reapplied or it remains off, depending on the user setup configuration in CMOS.

Table 14 provides the pinout listing for the primary power supply connector of the Advanced/RH motherboard.

**Table 14. Primary Power Supply Connector (J9H1)**

Pin	Signal Name/Function
1	PWRGD (Power good)
2	+5 V (VCC)
3	+12 V
4, key	-12 V
5	Ground
6	Ground
7, key	Ground
8	Ground
9	-5 V
10	+5 V (VCC)
11	+5 V (VCC)
12	+5 V (VCC)

Table 15 provides the pinout listing for the external 3.3 volt power supply connector of the Advanced/RH motherboard. This connector is normally not installed, because 3.3 volt power is supplied by the motherboard.

**Table 15. External 3.3 V Power Supply Connector (J9J1)**

Pin	Name
1	Ground
2, key	Ground
3	Ground
4	+3.3 V
5	+3.3 V
6	+3.3 V

The pinout listing for the soft-OFF power supply connector of the Advanced/RH motherboard is shown in Table 16. The motherboard silkscreen uses PS REMOTE to refer to this connector. This 3-pin keyed position supports a software-controlled power supply shutoff (Soft-OFF). When connected to this position, the power supply follows remote ON/OFF commands.

**Table 16. Soft-OFF Power Supply Connector (J9K2)**

Pin	Signal Name (Function)
1	PS_ON (Remote On/Off)
2	+5 VSB (+5 Volts Standby)
3	PS_COM (Supply presence)

### 1.10.5 Floppy/IDE Connectors

Table 17 lists the pinout and signal names for the floppy drive connector.

**Table 17. Floppy Drive Connector (J9K1)**

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	Index#
9	Ground	10	Motor Enable A#
11	Ground	12	Drive Select B#
13	Ground	14	Drive Select A#
15	Ground	16	Motor Enable B#
17	MSEN1	18	DIR#
19	Ground	20	STEP#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 00#
27	MSEN0	28	Write Protect#
29	Ground	30	Read Data#
31	Ground	32	Side 1 Select#
33	Ground	34	Diskette Change#

Table 18 lists the pinout and signal names for the IDE connectors.

**Table 18. IDE Connectors (J5C1, J6C1)**

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	Vcc pull-down
29	DDACK0 [DDACK1]#	30	Ground
31	IRQ14 [IRQ15]	32	Reserved
33	DAG1	34	Reserved
35	DAG0	36	DAG2
37	Chip Select 1P [1S]#	38	Chip Select 3P [3S]#
39	Activity#	40	Ground

## 1.10.6 Video Connectors

Table 19 lists the pinout and signal names for the VESA/ATI multimedia channel (AMC) connector. Table 20 and Table 21 provide the pinout and signal listings for the video memory upgrade headers.

**Table 19. VESA/ATI Multimedia Channel Connector (J1H1)**

Pin	Signal Name (Function)				Pin	Signal Name (Function)			
1	DGND (Digital Ground)				2	FC0 (Pixel Data 0)			
3	DGND (Digital Ground)				4	FC1 (Pixel Data 1)			
5	DGND (Digital Ground)				6	FC2 (Pixel Data 2)			
7*	EVIDEO	BS#1	IOR	IOR	8	FC3 (Pixel Data 3)			
9*	ESYNC	CONTROL	IOW	IOW	10	FC4 (Pixel Data 4)			
11*	EDCLK	SB#	RDY/INT	RDY/INT	12	FC5 (Pixel Data 5)			
13*	none	SDA (I <sup>2</sup> C)	SDA/SAD4	SDA	14	FC6 (Pixel Data 6)			
15	DGND (Digital Ground)				16	FC7 (Pixel Data 7)			
17	DGND (Digital Ground)				18	PCLK (Pixel Clock)			
19	DGND (Digital Ground)				20*	BLANK#	BS#0	SAD0	SAD0
21	VFSENSE# (AMC configuration sense)				22*	HSYNC	none	SAD1	SAD1
23*	none	SCL (I <sup>2</sup> C)	SCL	SCL	24*	VSYNC	none	SAD2	SAD2
25	Key (no pin)				26	DGND (Digital Ground)			
27	Key (no pin)				28	Key (no pin)			
29*	none	Vcc (+5 V)	Vcc (+5 V)	Vcc (+5 V)	30*	none	SA#	SAD3	SAD3
31*	none	RESET#	RESET#	RESET#	32*	none	SNRDY#	SAD7	SAD7
33*	none	none	SAD6	SAD6	34*	none	VMASK0	SAD5	SAD5
35*	none	Reserved	Reserved	SAD4	36*	none	AMCREV	AMCREV	AMCREV
37*	none	AGND (Audio Ground)			38*	none	+12 V	+12 V	+12 V
39*	none	AUDR (Audio right channel)			40*	none	AUDL (Audio left channel)		

\* These pins have 4 signals defined, depending on the mode of operation, and are listed in the following order:  
 Standard VESA Feature Connector (VFC)  
 MPEG Data Port (MDP)  
 Digital Video Stream (DVS)/Multimedia Peripheral Port (MPP), no video-out option  
 MPP, with video-out option

SCL is I<sup>2</sup>C clock; SDA is I<sup>2</sup>C data

SAD[7:0] are multiplexed address/data lines

**Table 20. Video Memory Upgrade Header #1 (J4L2)**

Pin	Signal Name / Function	Pin	Signal Name / Function	Pin	Signal Name / Function
1	MCLK	19	VMD2	37	VMD41
2	Ground	20	VMD1	38	VMD42
3	VCC3	21	VMD0	39	VMD43
4	VWEVTR#	22	Ground	40	VMD44
5	VMD8	23	VCC3	41	VMD45
6	VMD9	24	VCAS0R#	42	Ground
7	VMD10	25	VCAS1R#	43	VMD46
8	VMD11	26	VCAS2R#	44	VMD47
9	VMD12	27	VCAS3R#	45	VMD39
10	VMD13	28	Vacant, Key	46	VMD38
11	VMD14	29	VCAS4R#	47	VMD37
12	Ground	30	VCAS5R#	48	VMD36
13	VMD15	31	VCAS6R#	49	VMD35
14	VMD7	32	Ground	50	VMD34
15	VMD6	33	VCAS7R#	51	VMD33
16	VMD5	34	VWE_CAS0R#	52	Ground
17	VMD4	35	VWE_CAS1R#	53	VCC3
18	VMD3	36	VMD40	54	VMD32

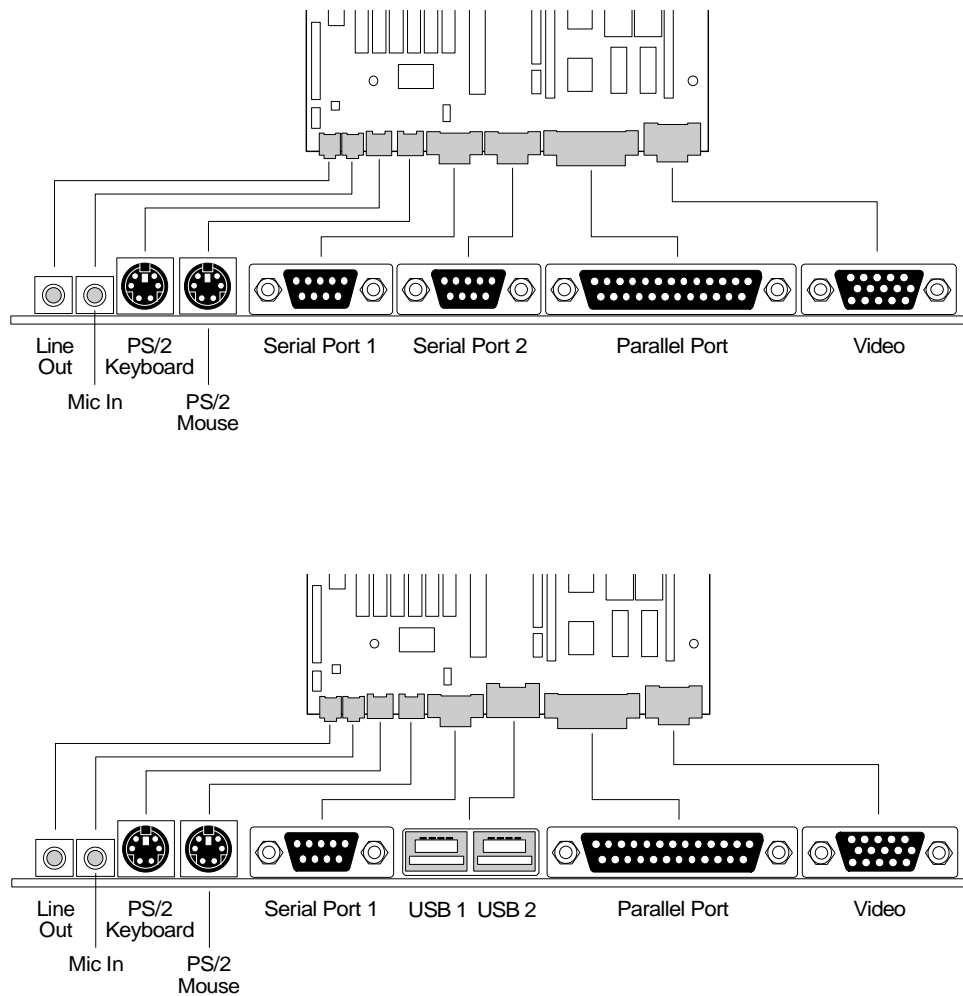
**Table 21. Video Memory Upgrade Header #2 (J1L1)**

Pin	Signal Name / Function	Pin	Signal Name / Function	Pin	Signal Name / Function
1	Ground	19	VMD31	37	VMD49
2	VMD16	20	VRAS0R#	38	VMD50
3	VMD17	21	Ground	39	VMD51
4	VCC3	22	VRAS1R#	40	VMD52
5	VMD18	23	VMAR0	41	Ground
6	VMD19	24	VMAR1	42	VMD53
7	VMD20	25	VMAR2	43	VMD54
8	VMD21	26	VMAR3	44	VMD55
9	VMD22	27	VMAR4	45	VMD56
10	VMD23	28	Vacant, Key	46	VMD57
11	Ground	29	VMAR5	47	VMD58
12	VMD24	30	VCC3	48	VMD59
13	VMD25	31	Ground	49	VMD60
14	VMD26	32	VMAR6	50	VMD61
15	VMD27	33	VMAR7	51	DSF
16	VMD28	34	VMAR8	52	VMD62
17	VMD29	35	VMAR9	53	VMD63
18	VMD30	36	VMD48	54	VCC3

## 1.10.7 Back Panel Connectors

Figure 5 shows the location of the back panel I/O connectors, which include:

- VGA monitor connector
- One parallel port
- One or optionally two serial ports (both options shown in Figure 5)
- Two optional USB connectors (option shown in Figure 5)
- PS/2-style keyboard and mouse connectors
- Optional external audio jacks: Line Out and Mic In



OM05633B

**Figure 5. Back Panel I/O Connectors**

**Table 22. Serial Port Connectors**

Pin	Signal Name	Description
1	DCD	Carrier Detect
2	SIN#	Serial Data In
3	SOUT#	Serial Data Out
4	DTR	Data Terminal Ready
5	GND	Chassis Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

**Table 23. USB Connectors**

Pin	Signal Name
1	Power
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

**Table 24. PS/2 Keyboard and Mouse Connectors**

Pin	Signal Name
1	Data
2	No connect
3	Ground
4	+5 V (fused)
5	Clock
6	No connect

**Table 25. Parallel Port Connector**

Pin	Signal Name	Description	Pin	Signal Name	Description
1	STB#	Strobe	14	AFD#	Auto Feed
2	PPD0	Data Bit 0	15	ERROR#	Fault
3	PPD1	Data Bit 1	16	INIT#	Initializing printer
4	PPD2	Data Bit 2	17	SLCTIN#	Select input
5	PPD3	Data Bit 3	18	GND	Chassis Ground
6	PPD4	Data Bit 4	19	GND	Chassis Ground
7	PPD5	Data Bit 5	20	GND	Chassis Ground
8	PPD6	Data Bit 6	21	GND	Chassis Ground
9	PPD7	Data Bit 7	22	GND	Chassis Ground
10	ACK#	Acknowledge	23	GND	Chassis Ground
11	BUSY	Port Busy	24	GND	Chassis Ground
12	PE	Paper end	25	GND	Chassis Ground
13	SLCT	Select			

**Table 26. VGA Video Monitor Connector**

Pin	Signal Name / Function	Pin	Signal Name / Function
1	Red Video	9	Key (no pin)
2	Green Video	10	Sync Return (Ground)
3	Blue Video	11	Monitor ID Bit 0 (not used)
4	Monitor ID Bit 2 (not used)	12	Monitor ID Bit 1 (not used)
5	Chassis Ground	13	Horizontal Sync
6	Red Return (Ground)	14	Vertical Sync
7	Green Return (Ground)	15	Not used
8	Blue Return (Ground)	Shield	Chassis Ground

## 1.11 Jumper Settings

There are three jumper blocks on the Advanced/RH motherboard. The jumper block at J4G1 defines the number of PCI slots (two or three slots) available on the riser board used with the motherboard. The jumper block at J6C2 sets the Flash memory to either normal or recovery mode of operation. The jumper block at J4L1 defines a range of microprocessor and motherboard configuration parameters. Figure 6 shows the jumper block locations on the motherboard.

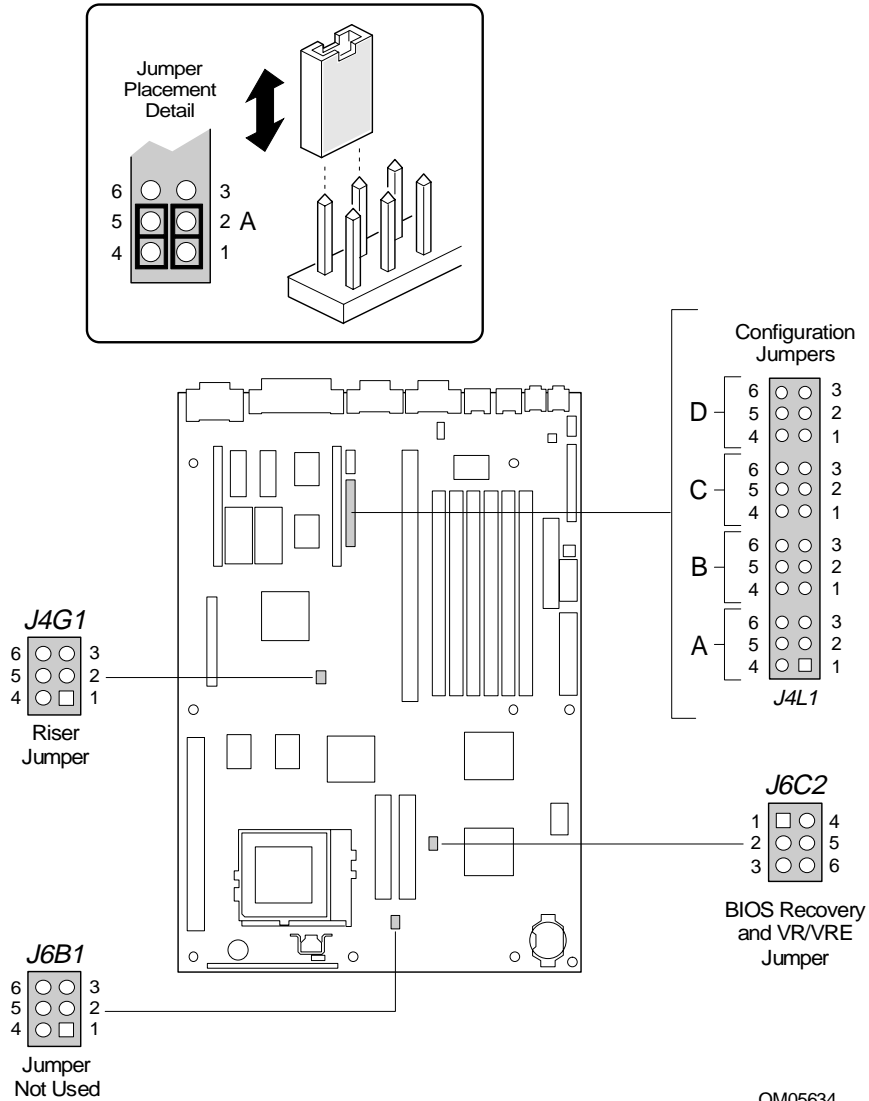


Figure 6. Jumper Locations



**CAUTION**

*Do not move any of the jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumpers.*

**Table 27. Jumper Settings**

Function **	Jumper	Configuration **
Password Clear ( <i>PSWD</i> )	J4L1-A	1-2 <b>KEEP</b> (Password enabled, <b>Default</b> ) 2-3 <b>CLR</b> (Password clear/disabled)
CMOS (NVRAM and ESCD) Clear ( <i>CMOS</i> )	J4L1-A	4-5 <b>KEEP (Default)</b> 5-6 <b>CLR</b> (reset to default settings)
BIOS Setup Access ( <i>SETUP</i> )	J4L1-B	1-2 <b>ENBL</b> (Access enabled, <b>Default</b> ) 2-3 <b>DIS</b> (Access denied)
Host Bus Frequency*	J4L1-C	See Table 28
Processor Frequency (host bus multiplier)	J4L1-D	See Table 28
2/3 PCI Select ( <i>RISER</i> )	J4G1	1-2 and 4-5 <b>2 SLOTS</b> (Two PCI slots) 2-3 and 5-6 <b>3 SLOTS</b> (Three PCI slots)
Flash BIOS Recovery	J6C2	1-2 <b>NORM</b> (Normal operation, <b>Default</b> ) 2-3 <b>RCVR</b> (Recover Flash)
Processor Voltage	J6C2	4-5 VR voltage (VR, <b>Default</b> ) 5-6 VRE voltage (VRE)

\* These jumpers also set the PCI and ISA bus frequencies

\*\* The text appearing in a **BOLD-ITALIC** font duplicates the text of the motherboard silkscreening.

### 1.11.1 Processor Configuration (J4L1, C & D)

The motherboard must be configured for the frequency of the installed processor. Table 28 shows the jumper settings for each frequency and the corresponding host bus, PCI bus, and ISA bus frequencies.

**Table 28. Jumper Settings for Processor and Host Bus Frequencies**

Processor Freq. (MHz)	Jumpers J4L1-C	Jumpers J4L1-D	Host Bus Freq. (MHz)	PCI Bus Freq. (MHz)	ISA Bus Freq. (MHz)	Bus/Processor Freq. Ratio
200	1-2 and 5-6	1-2 and 5-6	66	33	8.33	3
166	1-2 and 5-6	2-3 and 5-6	66	33	8.33	2.5
150	2-3 and 4-5	2-3 and 5-6	60	30	7.5	2.5
133	1-2 and 5-6	2-3 and 4-5	66	33	8.33	2
120	2-3 and 4-5	2-3 and 4-5	60	30	7.5	2
100	1-2 and 5-6	1-2 and 4-5	66	33	8.33	1.5
90	2-3 and 4-5	1-2 and 4-5	60	30	7.5	1.5
75	2-3 and 5-6	1-2 and 4-5	50	25	6.25	1.5
reserved	2-3 and 5-6	1-2 and 5-6				
reserved	1-2 and 4-5	All				

### 1.11.2 Password Clear (J4L1-A)

Use this jumper to clear the password if the password is forgotten. The default setting is pins 1-2, (password enabled). To clear the password, turn off the computer, move the jumper to pins 2-3, and turn on the computer. Then turn off the computer, and return the jumper to pins 1-2 to restore normal operation. If the jumper is in the 2-3 position (password disabled), you cannot set a password.

### 1.11.3 Clear CMOS (J4L1-A)

This jumper resets the CMOS settings to the default values. This procedure must be done each time the system BIOS is updated. The default setting for this jumper is pins 4-5 (keep CMOS settings). To reset the CMOS settings to the default values, turn off the computer, move the jumper to pins 5-6, then turn on the computer. When the computer displays the message “NVRAM cleared by jumper,” turn off the computer and return the jumper to pins 4-5 to restore normal operation.

### 1.11.4 BIOS Setup Access (J4L1-B)

This jumper enables or disables access to the Setup program. The default setting is pins 1-2 (access enabled). To disable access to the Setup program, move the jumper to pins 2-3.

### 1.11.5 VR/VRE Jumper (J6C2)

This jumper sets the output of the onboard voltage regulator. For processors that require VR voltage (nominally +3.3 volts), place the jumper on pins 4-5. For processors that require VRE voltage, place the jumper on pins 5-6. Voltage specifications are as follows:

- VR = 3.3 - 3.465 V
- VRE = 3.465 - 3.63 V



#### **CAUTION**

*When installing a processor in the motherboard for the first time or upgrading to a new processor, check the processor's documentation for the correct voltage setting.*

### 1.11.6 2/3 PCI Slot Select (J4G1)

These jumper settings define the number of PCI slots available in the riser board. Jumpers installed at J4G1 pins 1-2 and 4-5 indicate that the installed riser board has just two PCI slots available. Jumpers installed at J4G1 pins 2-3 and 5-6 indicate that the installed riser board has three PCI slots available.

### 1.11.7 BIOS Recovery (J6C2)

This jumper lets you recover the BIOS data from a diskette in the event of a catastrophic failure. The default setting is pins 1-2 (normal operation). To recover the BIOS, turn off the computer, move the jumper to pins 2-3, then turn on the computer to perform BIOS recovery. After recovery, turn off the computer and return the jumper to pins 1-2 to restore normal operation. See Section 3.1.14 for more details.

## 1.12 Reliability

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data @ 55°C.

Motherboard MTBF: 72706 hours calculated

## 1.13 Environmental

**Table 29. Motherboard Environmental Specifications**

Parameter	Specification															
Temperature																
Non-Operating	-40°C to +70°C															
Operating	+0°C to +55°C															
Vibration																
Unpackaged	5 Hz to 20 Hz : 0.01g <sup>2</sup> Hz sloping up to 0.02 g <sup>2</sup> Hz 20 Hz to 500 Hz : 0.02g <sup>2</sup> Hz (flat)															
Packaged	10 Hz to 40 Hz : 0.015g <sup>2</sup> Hz (flat) 40 Hz to 500 Hz : 0.015g <sup>2</sup> Hz sloping down to 0.00015 g <sup>2</sup> Hz															
Shock																
Unpackaged	50 G trapezoidal waveform Velocity change of 170 inches/sec.															
Packaged	Half Sine 2 millisecond															
	<table border="1"> <thead> <tr> <th>Product (Weight)</th> <th>Free Fall (Height in inches)</th> <th>Velocity (Change (in/sec))</th> </tr> </thead> <tbody> <tr> <td>&lt; 20 lb.</td> <td>36</td> <td>167</td> </tr> <tr> <td>21 - 40</td> <td>30</td> <td>152</td> </tr> <tr> <td>41 - 80</td> <td>24</td> <td>136</td> </tr> <tr> <td>81 - 100</td> <td>18</td> <td>118</td> </tr> </tbody> </table>	Product (Weight)	Free Fall (Height in inches)	Velocity (Change (in/sec))	< 20 lb.	36	167	21 - 40	30	152	41 - 80	24	136	81 - 100	18	118
Product (Weight)	Free Fall (Height in inches)	Velocity (Change (in/sec))														
< 20 lb.	36	167														
21 - 40	30	152														
41 - 80	24	136														
81 - 100	18	118														

## 1.14 Power Consumption

Table 30 and Table 31 list the voltage and current specifications for a typical computer based on the Advanced/RH that contains the motherboard, a 166 MHz Pentium processor, 24 MB EDO RAM, 256 KB PDSRAM L2 cache, 3.5-inch floppy drive, 1.6 GB hard drive, and 4X IDE CD-ROM. This information is preliminary and is provided only as a guide for calculating approximate power usage with additional resources added.

**Table 30. DC Voltage**

DC Voltage	Acceptable Tolerance
+3.3 V	± 5%
+5 V	± 5%
+5 VSB (standby)	± 5%
-5 V	± 5%
+12 V	± 5%
-12 V	± 5%

**Table 31. Power Usage**

Operating Conditions	AC (watts)	DC (amps)					
		+3.3 V	+5 V	-5 V	+12 V	-12 V	+5VSB
APM disabled, using Windows 95	28	426 mA	4.0A	< 10 mA	160mA	40 mA	N/A
APM enabled, in System Management Mode (SMM) using Windows 95	24.4	420 mA	2.2A	< 10 mA	160mA	41 mA	N/A
System powered down	N/A	N/A	N/A	N/A	N/A	N/A	< 10 mA

### 1.14.1 Power Supply Considerations

The motherboard is designed to operate with at least a 200 W LPX power supply for typical configurations or a higher wattage supply for heavily loaded configurations. The power supply must meet the following requirements:

- Rise time for power supply: 2 ms to 20 ms
- Minimum delay for Reset to Power Good: 100 ms
- Minimum Powerdown warning: 1 ms
- 3.3 V output must reach its minimum regulation level within ± 20 ms of the 5V output reaching its minimum regulation level

## 1.15 Regulatory Compliance

This printed circuit assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system.

### 1.15.1 Safety

#### 1.15.1.1 UL 1950 - CSA 950-95, 3rd edition, Dated 07-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada).

#### 1.15.1.2 CSA C22.2 No. 950-95, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

#### 1.15.1.3 EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

#### 1.15.1.4 IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

#### 1.15.1.5 EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

### 1.15.2 EMI

#### 1.15.2.1 FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)

#### 1.15.2.2 CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

#### 1.15.2.3 EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

**1.15.2.4 EN 50 082-1 (1992)**

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)

**1.15.2.5 VCCI Class 2 (ITE)**

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

**1.15.2.6 ICES-003, Issue 2**

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

**1.15.3 Product Certification Markings**

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the board and shipping container.
- UL Recognition Mark: Consists of the UL File No. E139761 on the component side of the board and the PB No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of board.

## 2 Motherboard Resources

### 2.1 Memory Map

Table 32. Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 196608 K	100000 - C000000	191 MB	Extended Memory
960 K - 1024 K	F0000 - FFFFF	64 K	System BIOS
944 K - 960 K	EC000 - EFFFF	16 K	Boot Block (available as UMB)
936 K - 944 K	EA000 - EBFFF	8 K	ESCD (Plug and Play configuration and DMI)
932 K - 936 K	E9000 - E9FFF	4 K	Reserved for BIOS
928 K - 932 K	E8000 - E8FFF	4 K	OEM Logo or Scan Flash Area
896 K - 928 K	E0000 - E7FFF	32 K	POST BIOS (available as UMB)
800 - 896 K	C8000 - DFFFF	96 K	Available High DOS memory (open to ISA and PCI bus)
640 K - 800 K	A0000 - C7FFF	160 K	Onboard video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 K	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 K	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 K	Conventional memory

### 2.2 DMA Channels

Table 33. DMA Channels


DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio* / Parallel Port
2	8- or 16-bits	Floppy Drive
3	8- or 16-bits	Parallel Port (for ECP or EPP) / Audio
4		Reserved - Cascade Channel
5	16-bits	Audio*
6	16-bits	Open
7	16-bits	Audio

\* Default resource assignment.

## 2.3 I/O Map

**Table 34. I/O Map**

Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX3 - DMA 1
0020 - 0021	2 bytes	PIIX3 - Interrupt Controller 1
002E - 002F	2 bytes	Super I/O Controller Configuration Registers
0040 - 0043	4 bytes	PIIX3 - Counter/Timer 1
0048 - 004B	4 bytes	PIIX3 - Counter/Timer 2
0060	1 byte	Keyboard Controller Byte - Reset IRQ
0061	1 byte	PIIX3 - NMI, Speaker Control
0064	1 byte	Keyboard Controller, CMD/STAT Byte
0070, bit 7	1 bit	PIIX3 - Enable NMI
0070, bits 6:0	7 bits	87C306 - Real Time Clock, Address
0071	1 byte	87C306 - Real Time Clock, Data
0078	1 byte	Reserved - Board Configuration
0079	1 byte	Reserved - Board Configuration
0080 - 008F	16 bytes	PIIX3 - DMA Page Registers
00A0 - 00A1	2 bytes	PIIX3 - Interrupt Controller 2
00B2 - 00B3	2 bytes	APM Control
00C0 - 00DE	31 bytes	PIIX3 - DMA 2
00F0	1 byte	Reset Numeric Error
0170 - 0177	8 bytes	Secondary IDE Channel
01F0 - 01F7	8 bytes	Primary IDE Channel
0200 - 0207	8 bytes	Audio / Game Port
0220 - 022F	16 bytes	Audio (Sound Blaster compatible)
0278 - 027F	8 bytes	LPT2
02E8 - 02EF	8 bytes	COM4 / Video (8514A)
02F8 - 02FF	8 bytes	COM2
0330 - 0331	2 bytes	MPU-401 (MIDI)
0376	1 byte	Secondary IDE Channel Command Port
0377	1 byte	Floppy Channel 2 Command
0377, bit 7	1 bit	Floppy Disk Change, Channel 2
0377, bits 6:0	7 bits	Secondary IDE Channel Status Port
0378 - 037F	8 bytes	Parallel Port 1
0388 - 038B	4 bytes	ADLIB (FM synthesizer)

continued 

**Table 34. I/O Map** (continued)

Address (hex)	Size	Description
03B4 - 03B5	2 bytes	Video (VGA)
03BA	1 byte	Video (VGA)
03BC - 03BF	4 bytes	LPT3
03C0 - 03CA	11 bytes	Video (VGA)
03CC	1 byte	Video (VGA)
03CE - 03CF	2 bytes	Video (VGA)
03D4 - 03D5	2 bytes	Video (VGA)
03DA	1 byte	Video (VGA)
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Floppy Channel 1
03F6	1 byte	Primary IDE Channel Command Port
03F7 (Write)	1 byte	Floppy Channel 1 Command
03F7, bit 7	1 bit	Floppy Disk Change Channel 1
03F7, bits 6:0	7 bits	Primary IDE Channel Status Port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge/level triggered PIC
0604 - 060B	8 bytes	Windows Sound System
LPT $n$ + 400h	8 bytes	ECP port, LPT $n$ base address + 400h
0CF8 - 0CFB*	4 bytes	PCI Configuration Address Register
0CF9**	1 byte	Turbo and Reset Control Register
0CFC - 0CFF	4 bytes	PCI Configuration Data Register
FF00 - FF07	8 bytes	IDE Bus Master Register
FFA0 - FFA7	8 bytes	Primary Bus Master IDE Registers
FFA8 - FFAF	8 bytes	Secondary Bus Master IDE Registers
***	32 bytes	USB

\* DWORD access only

\*\* Byte access only

\*\*\* Dynamically allocated in PCI I/O space

## ⇒ NOTE

See the Audio section(s) in Chapter 1 for specific I/O addresses that can be used by the audio components on your motherboard. This table does not list I/O addresses that may be used by add-in cards in the system.

### 2.3.1 Port 79 Definition

I/O Port 78 is reserved for BIOS use. I/O Port 79 is a read-only port. Table 35 lists the bits and definitions for I/O Port 79.

**Table 35. I/O Port 79 Bit Definition**

Bit	Description	Bit = 1	Bit = 0															
0	Reserved	N/A	N/A															
1	Soft-off capable power supply present	No	Yes															
2	Onboard Audio present	Yes	No															
3 and 4	Host bus frequency	<table border="1"> <thead> <tr> <th>4</th> <th>3</th> <th>Host Bus Frequency</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>==&gt; 50 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>==&gt; 60 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>==&gt; 66 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>==&gt; Not allowed</td> </tr> </tbody> </table>		4	3	Host Bus Frequency	0	0	==> 50 MHz	0	1	==> 60 MHz	1	0	==> 66 MHz	1	1	==> Not allowed
4	3	Host Bus Frequency																
0	0	==> 50 MHz																
0	1	==> 60 MHz																
1	0	==> 66 MHz																
1	1	==> Not allowed																
5	Setup Access	Enable access	Disable access															
6	Clear CMOS RAM	Keep values	Clear values															
7	Password Clear	Keep password	Clear password															

## 2.4 PCI Configuration Space Map

**Table 36. PCI Configuration Space Map**

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Intel FW82439HX (TXC)
00	07	00	Intel 82371SB (PIIX3 ) PCI/ISA bridge
00	07	01	Intel 82371SB (PIIX3 ) IDE Bus Master
00	07	02	Intel 82371SB (PIIX3 ) USB
00	08	00	ATI VGA Graphics
00	0B	00	PCI Expansion Slot: Optional for 3-slot riser
00	11	00	PCI Expansion Slot: User Available
00	13	00	PCI Expansion Slot: User Available

## 2.5 Interrupts

Table 37 lists the interrupt configuration options for onboard devices. The serial ports, parallel ports, and IDE controller can be configured using the BIOS Setup, the ICU, or any other Plug-and-Play resource manager (such as the Windows 95 Device Manager). The audio controller can be configured only using a Plug-and-Play resource manager. The graphics interrupt is assigned by the auto-configure utility during boot up.

**Table 37. Interrupts**

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer Full
2	Reserved, Cascade Interrupt From Slave PIC
3	COM2*
4	COM1*
5	LPT2 (Plug and Play option) / Audio* / User available
6	Floppy Drive
7	LPT1* / Audio / LPT3
8	Real Time Clock
9	Audio / User available
10	Audio / User available
11	USB (if enabled, else user available)
12	Onboard Mouse Port (if present, else user available)
13	Reserved, Math Coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

\* Default, but can be changed to another IRQ

## 2.6 PCI Interrupt Routing Map

The PCI specification allows for sharing of interrupts between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the normal operation or throughput of the devices. However, in some special cases where maximum performance is needed from a device, you may want to ensure that it does not share an interrupt with other PCI devices.

This section describes the interrupt sharing mechanism and how the interrupt signals are connected between the motherboard's PCI expansion slots and onboard PCI devices. Use this information to avoid sharing an interrupt for a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- **INTA:** By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- **INTB:** Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- **INTC and INTD:** Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX3 PCI-to-ISA bridge has four Programmable Interrupt Request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 38 lists the PIRQ signals and shows how the signals are connected to the PCI expansion slots and to onboard PCI interrupt sources.

**Table 38. PCI Interrupt Routing Map**

PIIX3 PIRQ Signal	Riser Card, First PCI Expansion Slot	Riser Card, Second PCI Expansion Slot	Riser Card, Optional Third PCI Expansion Slot	Onboard PCI Video Controller	USB
PIRQA	INTB	INTA	INTC		
PIRQB	INTA	INTC	INTB		
PIRQC	INTC	INTB	INTA		
PIRQD	INTD	INTD	INTD	X	X

For example, assume that you plug an add-in card that has one interrupt (group INTA) into the first PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQB signal. Now, however, plug an add-in card that has one interrupt (group INTA) into the first PCI slot. Plug a second add-in card that has two interrupts (groups INTA and INTB) into the second PCI slot. INTA in the first slot is connected to signal PIRQB. INTA in the second slot is connected to signal PIRQA, and INTB is connected to signal PIRQC. With no other cards added, the three interrupt sources on the first two cards each have a PIRQ signal to themselves. Typically, they will not share an interrupt.

**⇒ NOTE**

*The PIIX3 can connect each PIRQ line internally to one of the IRQ signals (3,4,5,7,9,11,14,15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.*



## 3 BIOS and Setup Utility

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### 3.1 Introduction

The motherboard uses an Intel BIOS, which is stored in Flash EEPROM and can be upgraded using a floppy disk-based program. In addition to the BIOS, the Flash EEPROM contains the Setup program, power-on self tests (POST), advanced power management (APM), the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 5.1 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS on the motherboard is identified as 1.00.01.CV2. New revisions and new BIOS identifiers are documented in the *Advanced/RH Motherboard Specification Update*. The motherboard specification documents, as well as the latest versions of the BIOS are available from Intel's FTP or World Wide Web sites (see Section 5.2).

Information on BIOS functions can be found in the *IBM PS/2 and Personal Computer BIOS Technical Reference* published by IBM, and the *ISA and EISA Hi-Flex AMIBIOS Technical Reference* published by AMI. Both manuals are available at most technical bookstores.

#### 3.1.1 BIOS Flash Memory Organization

The Intel PA28F002BX 2 Mb Flash component is organized as 32K x 8 (256 KB). The Flash device is divided into areas as described in Table 39. The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS Recovery Mode).

**Table 39. Flash Memory Organization**

System Address (Hex)	Size	Description
FFFF0000 - FFFFFFFF	64 KB	Main BIOS *
FFFE0000 - FFFEFFFF	16 KB	Boot Block (system BIOS recovery)
FFFEA000 - FFFEBFFF	8 KB	Virtual Product Data (VPD) Extended System Configuration Data (ESCD) (DMI configuration data / Plug and Play data)
FFFE9000 - FFFE9FFF	4 KB	Used by BIOS (e.g., for Event Logging)
FFFE8000 - FFFE8FFF	4 KB	OEM logo or Scan Flash Area
FFFC0000 - FFFE7FFF	160 KB	Main BIOS Block

\* At runtime, only this section is shadowed into RAM below the 1 MB address

### 3.1.2 BIOS Upgrades

Flash memory simplifies distributing BIOS upgrades. You can install a new version of the BIOS from a diskette. BIOS upgrades are available to be downloaded from the secure section on the Intel bulletin board or from Intel's FTP or World Wide Web sites (see Section 5.2).

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- Update the Flash BIOS from a file on a disk
- Copy the current BIOS code from the Flash EEPROM to a disk file as a backup, in the event that an upgrade cannot be successfully completed
- Compare the BIOS in the Flash device with a file to make sure the system has the correct version

The upgrade utility ensures that the upgrade BIOS extension matches the target system to prevent accidentally installing a BIOS for a different type of system.

### 3.1.3 Plug and Play: PCI Auto-Configuration

The PCI auto-configuration utility operates in conjunction with the Setup program to let you insert and remove PCI cards without user configuration (Plug and Play). When you turn on the system after adding a PCI card, the BIOS automatically configures interrupts, I/O space, and other parameters. Any interrupts set to "available" in Setup are considered free for use by PCI add-in cards. PCI interrupts are distributed to available ISA interrupts that have been not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. An ISA device cannot share an interrupt allocated to PCI.

PCI system configuration information is stored in ESCD format. You can clear the ESCD data by moving the CMOS Clear jumper (see Section 1.11.3).

For information about the version of PCI and Plug and Play supported by this BIOS, see Section 5.1. You can obtain copies of the specifications from the Intel World Wide Web site (see Section 5.2). Peer-to-peer hierarchical PCI Bridge is supported, and by using an OEM-supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

### 3.1.4 PCI IDE Support

If you select "Auto Configured" in Setup, the BIOS automatically sets up the two local bus IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives and tape drives (see Section 5.1 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in Setup. The ATAPI Specification recommends that ATAPI devices be configured as shown in Table 40.

**Table 40. Recommendations for Configuring an ATAPI Device**

	Primary Cable		Secondary Cable	
	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE System with only one cable	ATA	ATAPI		
Enhanced IDE with CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

### 3.1.5 ISA Plug and Play

If you select in Setup to boot with a Plug and Play OS (see Section 3.4.14.1.1), the BIOS auto-configures only ISA Plug and Play cards that are required for booting (IPL devices). If you select to not boot with a Plug and Play OS, the BIOS auto-configures all Plug and Play ISA cards.

### 3.1.6 ISA Legacy Devices

Since ISA legacy devices are not auto-configurable, the resources for them must be reserved. You can reserve resources in the Setup program or with an ISA configuration utility (see Section 5.2 for a Web site address).

System configuration information is stored in ESCD format. You can clear the ESCD data by moving the CMOS Clear jumper (see Section 1.11.3).

### 3.1.7 Desktop Management Interface

Desktop Management Interface (DMI) is a method of managing computers in an enterprise. The main component of DMI is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using DMI, a system administrator can obtain the system types, capabilities, operational status, installation date and other information about the system components. The DMI specification requires that certain information about the system's motherboard be made available to an applications program. This information is located in a series of data structures which are accessed in various ways by the DMI service layer. Component instrumentation allows the service layer to gain access to information stored in the general-purpose area of non-volatile RAM. The MIF database defines the data and provides the method for accessing the information.

The BIOS support for DMI enables the maximum benefit from applications such as LANDesk® Client Manager from Intel. The BIOS stores and can report on the following types of DMI information:

- BIOS data, such as the BIOS revision level
- Fixed system information, such as data about the motherboard, peripherals, serial numbers and asset tags, etc.
- System information discovered during bootup, such as memory size, cache size, processor speed, etc.
- Dynamic information, such as event detection and error logging (see also Section 3.4.15)

An OEM can use a utility that makes DMI calls to program system and chassis-related information into the Flash memory, so the BIOS can also report that information. Once this information is written, it is locked (read-only).

Intel can provide a utility for making DMI calls to the BIOS. Contact your local Intel Sales office for further information. The latest DMI specification is available from Intel (see Section 5.2) and other sites.

DMI does not work directly under non-Plug and Play operating systems (e.g., Windows NT). However, the BIOS supports a DMI table interface for such OSs. Using this support, a DMI service-level application running on a non-Plug and Play OS can access the DMI BIOS information.

### **3.1.8 Advanced Power Management**

The BIOS supports Advanced Power Management (APM); see Section 5.1 for the version supported. You can initiate the energy saving Standby mode in these ways:

- Keyboard hot key sequence specified in Setup
- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector

When in Standby mode, the motherboard reduces power consumption by using the processor's System Management Mode (SMM) capabilities and by spinning down hard drives and reducing power to or turning off VESA DPMS-compliant monitors. In Setup you can select the DPMS mode to use for the monitor: Standby, Suspend, Sleep, or Disabled (see Section 3.4.13.3).

While in Standby mode, the system retains the ability to respond to external interrupts; it can service requests such as incoming faxes or network messages while unattended. Any keyboard or mouse activity brings the system out of Standby mode and immediately restores power to the monitor.

APM is enabled in the BIOS by default; however, the system must be configured with an OS-dependent APM driver for the power-saving features to take effect. For example, Windows 95 enables APM automatically upon detecting the presence of the APM BIOS.

### **3.1.9 Language Support**

The BIOS Setup utility and help messages can be supported in 32 languages. Five languages are available at this time: American English, German, Italian, French, and Spanish. The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets. Translations of other languages may become available at a later date.

The default language is American English, which is always present unless another language is programmed into the BIOS using the Flash Memory Update Program (FMUP.EXE). See Section 5.2 for information about downloading FMUP and other utilities.

### 3.1.10 Boot Options

Booting from CD-ROM is supported in adherence to the “El Torito” bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the Boot Options field in Setup, CD-ROM is one of four possible boot devices, which are defined in priority order. The default setting is for the floppy drive to be the primary boot device and the hard drive to be the secondary boot device. (By default the third and fourth devices are disabled.) If you select CD-ROM as the boot device, it must be the first device.

#### ⇒ **NOTE**

*A copy of the “El Torito” specification is available on the Phoenix Web site <http://www.ptltd.com/techs/specs.html>.*

In Setup you can also select the network as a boot device, which allows booting from a network add-in card with a remote boot ROM installed.

### 3.1.11 OEM Logo or Scan Flash Area

The motherboard supports a 4 KB programmable Flash user area at memory location E8000-E8FFF. You can use this area to display a custom OEM logo during POST, or can insert a binary image that executes at certain times during the POST. A utility is available from Intel to assist with installing a logo into Flash for display during POST. Contact your local Intel Sales office for further information.

### 3.1.12 USB Support

When the optional USB connector is installed on the motherboard, it allows you to attach any of several USB devices as they become available. Typically, the device driver for USB devices will be managed by the OS. However, because keyboard and mouse support may be needed in the Setup program before the OS boots, the BIOS supports USB keyboards and mice. You can disable this support if necessary.

### 3.1.13 BIOS Setup Access Jumper

You can move the Setup Access jumper on the motherboard to enable or disable access to the Setup utility. The default is for access to be enabled. See Section 1.11.4 for the specific pins on which to place the jumper.

### 3.1.14 Recovering BIOS Data

Some types of failure can destroy the BIOS data. For example, the data could be lost if a power outage occurs while you are updating the BIOS in Flash memory. You can recover the BIOS data from a diskette by changing the setting of the BIOS Recovery jumper (see Section 1.11.7).

To create a BIOS recovery diskette, you must make a bootable DOS diskette and place the recovery files on it. The recovery files are available from Intel; contact your local Intel Sales office for further information. You can also get recovery instructions and download BIOS data by contacting the World Wide Web or FTP sites identified in Section 5.2.

## 3.2 BIOS Setup Program

The Setup program lets you modify the configuration for most basic changes without opening the system. Setup is accessible only during the Power-On Self Test (POST). To enter Setup, press the <F1> key after the POST memory test has begun and before boot begins. By default, there is a prompt to press the <F1> key to access Setup, but this prompt may be disabled. See Section 1.11.4 for information on placing the jumper that prevents user access to Setup for security purposes.

### 3.2.1 Overview of the Setup Menu Screens

Table 41 lists the screens displayed by the Setup utility. Setup initially displays the Main menu screen. In each screen there are options for modifying the system configuration. Select a menu screen by pressing the left <←> or right <→> arrow keys. Use the up <↑> or down <↓> arrow keys to select items in a screen. Use the <Enter> key to select an item for modification. For certain items, pressing <Enter> brings up a subscreen. After you have selected an item, use the arrow keys to modify the setting.

⇒ **NOTE**

*The Setup menu screens described in the following sections are based on the BIOS release numbered 1.00.12.CV2. Other BIOS releases are likely to have somewhat different screens or screen contents.*

**Table 41. Overview of the Setup Menu Screens**

Screen	Subscreen Options	Described in	Modifiable
<b>Main Screen</b>		(Sec. 3.3)	
System Date		(Sec. 3.3.1)	Yes
System Time		(Sec. 3.3.2)	Yes
Floppy Options Subscreen		(Sec. 3.3.3 and 3.3.15)	Yes
	Floppy A:		No
	Floppy B:		No
	Floppy A: Type		Yes
	Floppy B: Type		Yes
	Floppy Access		Yes
Primary IDE Master Subscreen		(Sec. 3.3.4 and 3.3.16)	Yes
Primary IDE Slave Subscreen		(Sec. 3.3.5 and 3.3.16)	Yes
Secondary IDE Master Subscreen		(Sec. 3.3.6 and 3.3.16)	Yes
Secondary IDE Slave Subscreen		(Sec. 3.3.7 and 3.3.16)	Yes
	IDE Device Configuration		Yes
	Number of Cylinders		Yes
	Number of Heads		Yes
	Number of Sectors		Yes
	Maximum Capacity		Indirectly
	IDE Translation Mode		Yes
	Multiple Sector Setting		Yes
	Fast Programmed I/O Modes		Yes
Language		(Sec. 3.3.8)	No
Boot Options Subscreen		(Sec. 3.3.9 and 3.3.17)	Yes
	First Boot Device		Yes
	Second Boot Device		Yes
	Third Boot Device		Yes
	Fourth Boot Device		Yes
	System Cache		Yes
	Boot Speed		Yes
	Num Lock		Yes
	Setup Prompt		Yes
	Hard Disk Pre-Delay		Yes
	Typematic Rate Programming		Yes
	Typematic Rate Delay		Yes
	Typematic Rate		Yes
	Scan User Flash Area		Yes
Video Mode		(Sec. 3.3.10)	No
Mouse		(Sec. 3.3.11)	No
Base Memory		(Sec. 3.3.12)	No
Extended Memory		(Sec. 3.3.13)	No
BIOS Version		(Sec. 3.3.14)	No
<b>Advanced Screen</b>		(Sec. 3.4)	
Processor Type		(Sec. 3.4.1)	No
Processor Speed		(Sec. 3.4.2)	No
Cache Size		(Sec. 3.4.3)	No

continued ➡

**Table 41. Overview of the Setup Menu Screens** (continued)

Screen	Subscreen Options	Described in	Modifiable
Peripheral Configuration Subscreen		(Sec. 3.4.4 and 3.4.10)	Yes
	Primary PCI IDE Interface		Yes
	Secondary PCI IDE Interface		Yes
	Floppy Interface		Yes
	Serial Port 1 Address		Yes
	Serial Port 2 Address		Yes
	Serial Port 2 IR Mode		Yes
	Parallel Port Address		Yes
	Parallel Port Mode		Yes
USB Support		Yes	
Audio Configuration Subscreen *		(Sec. 3.4.5 and 3.4.11)	Yes
	Interrupts		Yes
	8-Bit DMA		Yes
	16-Bit DMA		Yes
	Base Address		Yes
	MPU-401 Address		Yes
	Joystick Address		Yes
FM Address		Indirectly	
Advanced Chipset Configuration Subscreen		(Sec. 3.4.6 and 3.4.12)	Yes
	Base Memory Size		Yes
	ISA LFB Size		Yes
	ISA LFB Base Address		No
	Video Palette Snoop		Yes
	Latency Timer (PCI Clocks)		Yes
	Memory Error Detection		Yes
	Bank 0 SIMM Detected		No
	Bank 1 SIMM Detected		No
Bank 2 SIMM Detected		No	
Power Management Configuration Subscreen		(Sec. 3.4.7 and 3.4.13)	Yes
	Advanced Power Management		Yes
	IDE Drive Power Down		Yes
	VESA Video Power Down		Yes
	Inactivity Timer		Yes
Hot Key		Yes	
Plug and Play Configuration Subscreen		(Sec. 3.4.8 and 3.4.14)	Yes
	Configuration Mode		Yes
	Boot with PnP OS		Yes
	ISA Shared Memory Size		Yes
	ISA Shared Memory Base Address		Yes
IRQ 3-15		Yes	
Event Logging Configuration Subscreen		(Sec. 3.4.9 and 3.4.15)	Yes
	Event Log Status		No
	Log Capacity		No
	Count Granularity		No
	Log Control		Yes
	Clear Log		Yes
	Mark Existing Events Read		Yes
Critical Events in Log		No	

continued 

**Table 41. Overview of the Setup Menu Screens** (continued)

Screen	Subscreen Options	Described in	Modifiable
<b>Security Screen</b> .....		(Sec. 3.5)	
	Administrative and User Access Modes .....	(Sec. 3.5.1).....	Yes
	Security Screen Options .....	(Sec. 3.5.2).....	Yes
	User Password is .....		Indirectly
	Administrative Password is .....		Indirectly
	Set User Password .....		Yes
	Set Administrative Password.....		Yes
	Unattended Start .....		Yes
	Security Hot Key .....		Yes
<b>Exit Screen</b> .....		(Sec. 3.6)	
	Exit Saving Changes.....	(Sec. 3.6.1) .....	N/A
	Exit Discarding Changes.....	(Sec. 3.6.2).....	N/A
	Load Setup Defaults .....	(Sec. 3.6.3).....	N/A
	Discard Changes .....	(Sec. 3.6.4).....	N/A

\* The only configuration options available when using the Creative Labs Vibra 16C are Enabled or Disabled.

### 3.3 Main BIOS Setup Screen

This section describes the Setup options found on the main menu screen. If you select certain options from the main screen (e.g., Primary IDE Master), Setup switches to a subscreen for the selected option.

#### 3.3.1 System Date

Specifies the current date. Select the month, day, and year from a pop-up menu.

#### 3.3.2 System Time

Specifies the current time. Select the hour, minute, and second from a pop-up menu.

#### 3.3.3 Floppy Options

When selected, this displays the Floppy Options menu.

#### 3.3.4 Primary IDE Master

Reports if an IDE device is connected to the Primary IDE master interface. When selected, this displays the IDE Device Configuration subscreen.

#### 3.3.5 Primary IDE Slave

Reports if an IDE device is connected to the Primary IDE slave interface. When selected, this displays the IDE Device Configuration subscreen.

### **3.3.6 Secondary IDE Master**

Reports if an IDE device is connected to the Secondary IDE master interface. When selected, this displays the IDE Device Configuration subscreen.

### **3.3.7 Secondary IDE Slave**

Reports if an IDE device is connected to the Secondary IDE slave interface. When selected, this displays the IDE Device Configuration subscreen.

### **3.3.8 Language**

Specifies the language of the text strings used in the Setup utility and the BIOS. The options are any installed languages.

### **3.3.9 Boot Options**

When selected, this displays the Boot Options subscreen.

### **3.3.10 Video Mode**

Reports the video mode. There are no options.

### **3.3.11 Mouse**

Reports if a mouse is installed or not. There are no options.

### **3.3.12 Base Memory**

Reports the amount of base memory. There are no options.

### **3.3.13 Extended Memory**

Reports the amount of extended memory. There are no options.

### **3.3.14 BIOS Version**

Reports the BIOS identification string. There are no options.

### **3.3.15 Floppy Options Subscreen**

#### **3.3.15.1 Floppy A:**

Reports if a diskette drive is connected to the system. There are no options.

#### **3.3.15.2 Floppy B:**

Reports if a second diskette drive is connected to the system. There are no options.

### 3.3.15.3 Floppy A: Type

Specifies the physical size and capacity of the diskette drive. The options are:

- Disabled
- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44/1.25 MB, 3.5-inch (**default**)
- 2.88 MB, 3.5-inch

### 3.3.15.4 Floppy B: Type

Specifies the physical size and capacity of the diskette drive. The options are:

- Disabled (**default**)
- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.44/1.25 MB, 3.5-inch
- 2.88 MB, 3.5-inch

### 3.3.15.5 Floppy Access

The following options change the access for all attached floppy drives:

- Read/Write (**default**)
- Read Only

## 3.3.16 Primary/Secondary IDE Master/Slave Configuration Subscreens

There are four subscreens used to enable IDE devices:

- Primary IDE Master
- Primary IDE Slave
- Secondary IDE Master
- Secondary IDE Slave

All four subscreens contain the same eight fields described below.

### 3.3.16.1 IDE Device Configuration

Used to manually configure the hard drive or have the system auto-configure it. The options are:

- Auto Configured (**default**)
- User Definable
- Disabled

If you select User Definable, you can modify the Number of Cylinders, Number of Heads, and Number of Sectors items. If you select Disabled, the BIOS will not scan for a device on that interface.

### 3.3.16.2 Number of Cylinders

If IDE Device Configuration is set to Auto Configured, this field reports the number of cylinders for your hard disk and cannot be modified. If IDE Device Configuration is set to User Definable, you must type the correct number of cylinders for your hard disk.

### 3.3.16.3 Number of Heads

If IDE Device Configuration is set to Auto Configured, this field reports the number of heads for your hard disk and cannot be modified. If IDE Device Configuration is set to User Definable, you must type the correct number of heads for your hard disk.

### 3.3.16.4 Number of Sectors

If IDE Device Configuration is set to Auto Configured, this field reports the number of sectors for your hard disk and cannot be modified. If IDE Device Configuration is set to User Definable, you must type the correct number of sectors for your hard disk.

### 3.3.16.5 Maximum Capacity

Reports the maximum capacity of your hard disk, which is calculated from the number of cylinders, heads, and sectors. There are no options.

### 3.3.16.6 IDE Translation Mode

Specifies the IDE translation mode. The options are:

- Standard CHS (standard cylinder head sector, for drives with fewer than 1024 cylinders)
- Logical Block (LBA)
- Extended CHS (extended cylinder head sector, for drives with more than 1024 cylinders)
- Auto Detected (BIOS detects IDE drive support for LBA) (default)



#### **CAUTION**

*Do not change the IDE translation mode from the option selected when the hard drive was formatted. Changing the option after formatting can result in corrupted data.*

### 3.3.16.7 Multiple Sector Setting

Sets the number of sectors transferred by an IDE drive per interrupt generated. The options are:

- Disabled
- 4 Sectors/Block
- 8 Sectors/Block
- Auto Detected (**default**)

Check the specifications for your hard disk drive to determine which setting provides optimum performance for your drive.

### 3.3.16.8 Fast Programmed I/O Modes

Sets how fast the transfers occur on the IDE interface. The options are:

- Disabled (transfers occur at a less than optimized speed)
- Auto Detected (transfers occur at the drive's maximum speed) (**default**)

### 3.3.17 Boot Options Subscreen

This section describes the options available on the Boot Options subscreen.

#### 3.3.17.1 First Boot Device

Sets which drive the system checks first to find an operating system to boot from. The options are:

- Disabled
- Floppy (**default**)
- Hard Disk
- CD-ROM
- Network

#### 3.3.17.2 Second Boot Device

Sets which drive the system checks second to find an operating system to boot from. The options are:

- Disabled
- Floppy
- Hard Disk (**default**)
- Network

#### 3.3.17.3 Third Boot Device

Sets which drive the system checks third to find an operating system to boot from. The options are:

- Disabled (**default**)
- Floppy
- Hard Disk
- Network

#### 3.3.17.4 Fourth Boot Device

Sets which drive the system checks fourth to find an operating system to boot from. The options are:

- Disabled (**default**)
- Floppy
- Hard Disk
- Network

#### 3.3.17.5 System Cache

Enables or disables both primary and secondary cache memory. The options are:

- Enabled (**default**)
- Disabled

### 3.3.17.6 Boot Speed

Sets the system's boot speed. The options are:

- Deturbo (the motherboard operates at the speed of an AT<sup>T</sup> system)
- Turbo (boot-up occurs at full speed) (**default**)

### 3.3.17.7 Num Lock

Sets the beginning state of the Num Lock feature on the numeric keypad of your keyboard. The options are:

- Off (**default**)
- On

### 3.3.17.8 Setup Prompt

#### ⇒ **NOTE**

*The Setup Prompt option does not affect your ability to access the Setup program. It only enables or disables the prompt.*

Controls whether the “Press <F1> Key if you want to run Setup” prompt is displayed during the power-up sequence. The options are:

- Enabled (**default**)
- Disabled

### 3.3.17.9 Hard Disk Pre-Delay

Sets the hard disk drive pre-delay. When enabled, this option causes the BIOS to wait the specified time before it accesses the first hard drive. If your system contains a hard drive and you don't see the drive type displayed during boot-up, the hard drive may need more time before it is able to communicate with the controller. Setting a pre-delay provides additional time for the hard drive to initialize. The options are:

- Disabled (**default**)
- 3 seconds
- 6 seconds
- 9 seconds
- 12 seconds
- 15 seconds
- 21 seconds
- 30 seconds

### 3.3.17.10 Typematic Rate Programming

Sets the typematic rates. The options are:

- Default (**default**)
- Override (lets you enter Typematic Rate Delay and Typematic Rate options)

### 3.3.17.11 Typematic Rate Delay

Sets the delay time (in milliseconds) before the key-repeat function starts when you hold down a key on the keyboard. If Typematic Rate Programming is set to Default, this option will not be visible. The options are:

- 250 msec (**default**)
- 500 msec
- 750 msec
- 1000 msec

### 3.3.17.12 Typematic Rate

Sets the speed at which characters repeat when you hold down a key on the keyboard. The higher the number, the faster the characters repeat. If Typematic Rate Programming is set to Default, this option will not be visible. The options are:

- 6 char/sec (**default**)
- 8 char/sec
- 10 char/sec
- 12 char/sec
- 15 char/sec
- 20 char/sec
- 24 char/sec
- 30 char/sec

### 3.3.17.13 Scan User Flash Area

Scans the user Flash area for an executable binary to be executed during POST. The options are:

- Disabled (no scan)
- Enabled (scan occurs during POST) (**default**)

## 3.4 Advanced Screen

This section describes the Setup options found on the Advanced menu screen. If you select certain options from the Advanced screen (e.g., Peripheral Configuration), the Setup program switches to a subscreen for the selected option. Subscreens are described in the sections following the description of the Advanced screen options.

### 3.4.1 Processor Type

Reports the processor type. There are no options.

### 3.4.2 Processor Speed

Reports the processor clock speed. There are no options.

### 3.4.3 Cache Size

Reports the size of the secondary cache. There are no options. If your computer contains no L2 cache, this item does not appear.

### 3.4.4 Peripheral Configuration

When selected, this displays the Peripheral Configuration subscreen.

### 3.4.5 Audio Configuration

When selected, this displays the Audio Configuration subscreen.

### 3.4.6 Advanced Chipset Configuration

When selected, this displays the Advanced Chipset Configuration subscreen.

### 3.4.7 Power Management Configuration

When selected and enabled, this displays the Advanced Power Management subscreen.

### 3.4.8 Plug and Play Configuration

When selected, this displays the Plug and Play Configuration subscreen.

### 3.4.9 Event Logging Configuration

When selected, this displays the Event Logging Configuration subscreen.

### 3.4.10 Peripheral Configuration Subscreen

This section describes the Setup options for the Peripheral Configuration subscreen. For peripherals set to Auto, the BIOS automatically configures the peripheral during power up. The Configuration Mode options are:

- Auto (**default**)
- Manual

#### 3.4.10.1 Primary PCI IDE Interface

Disables or automatically configures the primary PCI IDE hard disk interface. The options are:

- Disabled
- Enabled (**default**)

### 3.4.10.2 Secondary PCI IDE Interface

Disables or automatically configures the secondary PCI IDE hard disk interface. The options are:

- Disabled
- Enabled (**default**)

### 3.4.10.3 Floppy Interface

Disables or automatically configures the diskette drive interface. The options are:

- Disabled
- Enabled (**default**)

### 3.4.10.4 Serial Port 1 Address

Selects the logical COM port, I/O address and interrupt for Serial Port 1. The options that are displayed can vary, depending on whether you choose Windows 95 in the Boot with PnP OS screen (see Section 3.4.14.1.1). The options appear in the following format:

- Disabled
- COM1, 3F8, IRQ4 (**default**)
- COM3, 3E8, IRQ4

### 3.4.10.5 Serial Port 2 Address

Selects the logical COM port, I/O address and IRQ of Serial Port 2. The options that are displayed can vary, depending on whether you choose Windows 95 in the Boot with PnP OS screen (see Section 3.4.14.1.1). The options appear in the following format:

- Disabled
- COM2, 2F8, IRQ3 (**default**)
- COM3, 3E8, IRQ4

#### ⇒ **NOTE**

*If you specifically set either serial port address, that address will not appear in the list of options for the other serial port. If an ATI mach32<sup>†</sup> or an ATI mach64<sup>†</sup> video controller is active (either onboard or as an add-in card), the COM4, 2E8h address will not appear in the list of options for either serial port.*

### 3.4.10.6 Serial Port 2 IR Mode

Makes Serial Port 2 available to infrared applications. The options are:

- Disabled (**default**)
- Enabled

### 3.4.10.7 Parallel Port Address

Selects the logical printer port, I/O address, interrupt, and DMA channel (if applicable) of the parallel port. The options that are displayed can vary, depending on the Parallel Port Mode you choose (see Section 3.4.10.8) and whether you choose Windows 95 in the Boot with PnP OS screen (see Section 3.4.14.1.1).

### 3.4.10.8 Parallel Port Mode

Selects the mode for the parallel port. The options are:

- Compatible (operates in AT-compatible mode) **(default)**
- Bi-directional (operates in bidirectional PS/2-compatible mode)
- ECP (Extended Capabilities Port, a high-speed bidirectional mode)
- EPP (Enhanced Parallel Port, a high-speed bidirectional mode)

The compatible and bi-direction mode options are described and listed in Table 42.

**Table 42. Parallel Port Compatible or Bi-directional Configuration Options**

Option	Description
Disabled	Port not enabled
LPT3, 3BC, IRQ7	Enabled as LPT3 at indicated I/O address and IRQ
LPT1, 378, IRQ7	Enabled as LPT1 at indicated I/O address and IRQ <b>(default)</b>
LPT2, 278, IRQ7	Enabled as LPT2 at indicated I/O address and IRQ
LPT3, 3BC, IRQ5	Enabled as LPT3 at indicated I/O address and IRQ
LPT1, 378, IRQ5	Enabled as LPT1 at indicated I/O address and IRQ
LPT2, 278, IRQ5	Enabled as LPT2 at indicated I/O address and IRQ

The EPP mode options are described and listed in Table 43.

**Table 43. Parallel Port EPP Configuration Options**

Option	Description
LPT1, 378, IRQ7	Enabled as LPT1 at indicated I/O address and IRQ
LPT2, 278, IRQ7	Enabled as LPT2 at indicated I/O address and IRQ
LPT1, 378, IRQ5	Enabled as LPT1 at indicated I/O address and IRQ
LPT2, 278, IRQ5	Enabled as LPT2 at indicated I/O address and IRQ

The ECP mode options are described and listed in Table 44.

**Table 44. Parallel Port ECP Configuration Options**

Option	Description
Disabled	Port not enabled
LPT1, 378, IRQ7, DMA3	Enabled as LPT1 at indicated I/O address, IRQ, and DMA channel.
LPT2, 278, IRQ7, DMA3	Enabled as LPT2 at indicated I/O address, IRQ, and DMA channel.
LPT1, 378, IRQ5, DMA3	Enabled as LPT1 at indicated I/O address, IRQ, and DMA channel.
LPT2, 278, IRQ5, DMA3	Enabled as LPT2 at indicated I/O address, IRQ, and DMA channel.

### 3.4.10.9 USB Support

Enables or disables the USB interface. USB support requires that the BIOS allocate a PCI interrupt, which could cause an interrupt to be shared with another device. If interrupt sharing is a problem and you do not need support for USB, you can free an interrupt by disabling USB.

- Disabled (frees the PCI interrupt used to support USB)
- Enabled (**default**)

### 3.4.11 Audio Configuration Subscreen

This option configures or disables the onboard audio subsystem. The options are:

- Auto (**default**)
- Manual
- Disabled (frees the I/O resources and addresses used to support the audio interface)

When Auto is selected, the audio configuration options are selected automatically. When Manual is selected, the subscreens described in the following sections are displayed. The Disabled option frees all audio-associated IRQs, I/O resources, and addresses so they can be used elsewhere.

#### ⇒ **NOTE**

*The only configuration options available when using the Creative Labs Vibra 16C device are Enabled (**default**) or Disabled.*

#### 3.4.11.1 Interrupt

Selects the interrupt that the subsystem will use. The options are:

- IRQ 5 (**default**)
- IRQ 7
- IRQ 9
- IRQ 10

#### 3.4.11.2 8-Bit DMA

Selects the channel that will be used for 8-bit DMA transfers. The options are:

- Channel 1 (**default**)
- Channel 3

#### 3.4.11.3 16-Bit DMA

Selects the channel that will be used for 16-bit DMA transfers. The options are:

- Channel 5 (**default**)
- Channel 7

#### 3.4.11.4 Base Address

Selects the base I/O address that will be used for audio operations. The options are:

- 0220h - 022Fh (**default**)
- 0240h - 024Fh
- 0260h - 026Fh
- 0280h - 028Fh

#### 3.4.11.5 MPU-401 Address

Selects the I/O address used as the MPU-401 address. The options are:

- 0330h - 0331h (**default**)
- 0300h - 0301h
- Disabled

#### 3.4.11.6 Joystick Address

Selects the I/O address used as the joystick address. The options are:

- 0200h - 0207h (**default**)
- Disabled

#### 3.4.11.7 FM Address

This field has no options. Unless the audio configuration options are Disabled, the I/O address range of 0388h through 038Bh is reserved for the FM address.

### 3.4.12 Advanced Chipset Configuration Subscreen

This section describes the options available on the Advanced Chipset Configuration subscreen.

#### 3.4.12.1 Base Memory Size

Sets the size of the base memory. The options are:

- 512 KB
- 640 KB (**default**)

### 3.4.12.2 ISA LFB Size

Sets the size of the linear frame buffer. The options are:

- Disabled (**default**)
- 1 MB (if selected, the ISA LFB Base Address field appears)

### 3.4.12.3 ISA LFB Base Address

Reports the base address of the linear frame buffer. There are no options. This field does not appear if the ISA LFB Size is set to Disabled.

### 3.4.12.4 Video Palette Snoop

Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card. The options are:

- Disabled (**default**)
- Enabled

### 3.4.12.5 Latency Timer (PCI Clocks)

Sets the length of time (measured in the number of PCI clock cycles) that an agent on the PCI bus can hold the bus when another agent has requested the bus. The options are Auto Configured, 16, 24, 32, ... 128 clocks. The default is Auto Configured.

### 3.4.12.6 Memory Error Detection



#### **CAUTION**

*Parity or ECC memory **MUST** be manually enabled in the BIOS if it is to be used. In order to use either parity or ECC memory error detection, **ALL** onboard memory must be capable of supporting the selected option. If **ANY** of the installed onboard memory does not support either the parity or ECC option, **NONE** of the onboard memory can be configured to support that option.*

Memory error detection sets the type of error detection or correction. This field appears if either ECC or Parity system memory is detected. Parity and ECC memory may be configured to run either as Parity or ECC (parity memory may be configured to run in ECC mode). The options are:

- Disabled (**default**)
- ECC
- Parity

### 3.4.12.7 Bank 0 SIMM Detected

Reports the size and type of memory found in bank 0. There are no options.

### 3.4.12.8 Bank 1 SIMM Detected

Reports the size and type of memory found in bank 1. There are no options.

### 3.4.12.9 Bank 2 SIMM Detected

Reports the size and type of memory found in bank 2. There are no options.

### 3.4.13 Power Management Configuration Subscreen

This section describes the options available on the Power Management Configuration subscreen.

#### 3.4.13.1 Advanced Power Management

Enables or disables the Advanced Power Management (APM) support in the BIOS. APM manages power consumption only when used with an APM-capable operating system. The options are:

- Disabled (none of the following fields in the Advanced Power Management subscreen appear)
- Enabled (**default**)

#### 3.4.13.2 IDE Drive Power Down

Sets any IDE drives to spin down when the computer goes into power managed mode. The options are:

- Disabled
- Enabled (**default**)

#### 3.4.13.3 VESA Video Power Down

Sets any VESA-compliant monitor to be power managed when the system goes into power managed mode. The options are:

- Disabled (the monitor is not under power management)
- Standby (minimal power reduction, HSYNC signal not active)
- Suspend (significant power reduction, VSYNC signal not active)
- Sleep (maximum power reduction, HSYNC and VSYNC not active) (**default**)

#### 3.4.13.4 Inactivity Timer

Sets the number of minutes the computer must be inactive before it enters power-managed mode. The range is 0 - 255 minutes. The default is 10 minutes.

#### 3.4.13.5 Hot Key

Sets the hot key for power-managed mode. When a user presses this key while holding down the <Ctrl> and <Alt> keys, the system enters power-managed mode. All alphabetic keys are valid entries for this field. The BIOS must be connected to an OS-dependent APM driver for this option to work.

#### ⇒ **NOTE**

*If you set the APM hot key and the Security hot key (see Section 3.5.2.6) to the same key, the APM function has priority.*

## 3.4.14 Plug and Play Configuration Subscreen

This section describes the options in the Plug and Play configuration subscreen.

### 3.4.14.1 Configuration Mode

Sets how the BIOS gets information about ISA cards that do not have Plug and Play capabilities. The options are:

- Use Setup Utility (displays a choice of operating systems as listed in the following section) **(default)**
- Use ICU (ISA Configuration Utility resource reserving options for ISA legacy devices)

#### 3.4.14.1.1 Boot with PnP OS

This option is only available if the Use ICU option is selected in the Plug and Play Configuration Mode screen. This option applies only to Plug and Play ISA cards; the BIOS always auto-configures PCI devices. The option lets the computer boot with an operating system capable of managing Plug and Play add-in cards. If you choose one of the Plug and Play OS options (Other or Windows 95), the BIOS assigns resources to ISA Plug and Play initial program load (IPL) devices. The OS must then enable devices and assign resources (I/O addresses, interrupts, etc.) for all remaining devices.

The options are:

- None (for DOS; BIOS configures and enables all devices at boot time)
- Other (BIOS auto-configures PCI devices before onboard motherboard devices)
- Windows 95 (BIOS auto-configures onboard motherboard devices before PCI devices) **(default)**

### 3.4.14.2 ISA Shared Memory Size

This option is only available if the Use Setup Utility option is selected in the Plug and Play Configuration Mode screen. It allows you to specify a range of memory addresses that will be usable by ISA add-in cards for shared memory, and that will not be used for shadowing ROM memory from other devices. The options are:

- Disabled (the ISA Shared Memory Base Address field does not appear) **(default)**
- 16 KB
- 32 KB
- 48 KB
- 64 KB
- 80 KB
- 96 KB

Enable this field only if you are using a legacy ISA add-in card without Plug and Play capabilities, and the card requires non-ROM memory space. For example, this could include LAN cards that have onboard memory buffers or video capture cards that have video buffer memory.

By default, upper memory is allocated as follows: Memory from C0000-C7FFF is automatically shadowed (this memory range is typically reserved for video BIOS). Memory from C8000-DFFFF is initially unshadowed. The BIOS scans this range for any ISA add-in cards that may be present and notes their location and size. The BIOS then auto-configures the PCI devices and Plug and

Play devices, shadowing their ROM requirements (other than video) into the area above E0000. If that area becomes full, it continues shadowing to the area between C8000 and DFFFF. If an ISA legacy card has non-ROM memory requirements, the auto-configure routine might write into an area that is needed by the ISA card. Use the ISA Shared Memory Size and ISA Shared Memory Base Address fields to reserve a block of memory that will not be used for shadowing.

### 3.4.14.3 ISA Shared Memory Base Address

This option is only available if the Use Setup Utility option is selected in the Plug and Play Configuration Mode screen and the Disabled option is NOT selected in the ISA Shared Memory Size field. It sets the base address for the ISA Shared Memory. The options are:

- C8000h (**default**)
- CC000h
- D0000h
- D4000h
- D8000h
- DC000h

The options that appear depend on the ISA Shared Memory Size field. The total amount of ISA Shared Memory cannot extend to the E0000h address. For example, if you specify a size of 64KB, options D4000h, D8000h, and DC000h will not be available.

### 3.4.14.4 IRQ 3, 4, 5, 7, 9, 10, 11, 14, 15

This option is only available if the Use Setup Utility option is selected in the Plug and Play Configuration Mode screen. It sets the status of the IRQ. The options are:

- Available (**default**)
- Used By ISA Card

The PCI auto-configuration code uses these settings to determine whether these interrupts are available for use by PCI add-in cards. If an interrupt is marked available, the auto-configuration code can assign the interrupt to be used by the system. If your computer has an ISA add-in card that requires an interrupt, select Used By ISA Card for that interrupt.

#### ⇒ **NOTE**

*IRQs 5, 9, 10, and 11 are the default user-available IRQs. Depending on the configuration of your computer, other IRQs may be listed (for example, if you disable the parallel port and/or serial ports). The IRQs listed in this section are available if all options under Peripheral Configuration and Audio Configuration subscreens are set to Disabled. Refer to Section 2.5 for a full list of the IRQs used with this motherboard.*

## 3.4.15 Event Logging Configuration Subscreen

This section describes the options available in the Event Logging Configuration subscreen.

### 3.4.15.1 Event Log Status

This information field tells whether the status is valid or not. There are no options.

### 3.4.15.2 Log Capacity

This information field tells whether the log is full or not. There are no options.

### 3.4.15.3 Count Granularity

This information field tells the number of log events that will occur before the event log is updated. There are no options.

### 3.4.15.4 Time Granularity (Minutes)

This information field tells the number of minutes that will pass before the event log is updated. There are no options.

### 3.4.15.5 Log Control

Enables event logging. The options are:

- Enabled (**default**)
- ECC Disabled
- Disabled

### 3.4.15.6 Clear Log

Sets a flag that clears the event log the next time the POST runs. The options are:

- No (the event log will not be cleared) (**default**)
- Yes (the event log will be cleared)

### 3.4.15.7 Mark Existing Events Read

Sets a flag that marks all events in the log as having been read, the next time the POST runs. The options are:

- No (events will not be marked as read) (**default**)
- Yes (all events will be marked as read)

### 3.4.15.8 Critical Events in Log

The bottom of the Event Log screen includes several information fields that display information about the date and time of the last event of a specific type, as well as a count of how many events of that type are logged. Selecting a field and pressing Enter displays a subscreen that shows information specific to that type of event.

Table 45 lists the event types for which subscreens are available.

**Table 45. Event Log Subscreens**

Event Type	Subscreen Detail	
Single Bit ECC Events	Date of Last Occurrence	None <i>(initial value)</i>
	Time of Last Occurrence	None <i>(initial value)</i>
	Total Count of Events/Errors	None <i>(initial value)</i>
	Memory Bank with Errors	None <i>(initial value)</i>
Multiple Bit ECC Events	Date of Last Occurrence	None <i>(initial value)</i>
	Time of Last Occurrence	None <i>(initial value)</i>
	Total Count of Events/Errors	None <i>(initial value)</i>
	Memory Bank with Errors	None <i>(initial value)</i>
POST Errors	Number of errors logged during POST	None <i>(initial value)</i>

## 3.5 Security Screen

This section describes the passwords you can set to restrict access to the Setup program and to restrict who can boot the computer.

### 3.5.1 Administrative and User Access Modes

The options on the Security screen let you set a User password and/or an Administrative password. The access restrictions for the User and Administrative modes are:

- **Setup options:** The Administrative password gives you full access to Setup options; the User password can be limited to only certain options. Thus, by setting separate Administrative and User passwords, a system administrator can limit who can change critical Setup values. The actual limitations depend on whether one or both passwords are set. Table 46 shows how the passwords work together.
- **Booting the system:** To limit access to who can boot the system, set the User password. This is the password that the system asks for before booting. If only the Administrative password is set, the system boots up without asking for a password. If both passwords are set, you can enter either password to boot the system.

Table 46 shows the effects of setting the Administrative and User passwords. The table is for reference only, and is not shown on the Security screen.

**Table 46. Administrative and User Password Functions**

Password Set	Administrative Mode	User Mode	Password Required During Boot Process
Neither	Can change all options*	Can change all options*	None
Administrative only	Can change all options	Can change a limited number of options **	None
User only	N/A	Can change all options	User
Both	Can change all options	Can change a limited number of options **	Administrative or User

\* If no password is set, any user can change all Setup options.

\*\* Limited options include only: system date and time, power management hot key, User password, security hot key, and unattended start

## 3.5.2 Security Screen Options

### 3.5.2.1 User Password is

Reports if there is a User password set. There are no options.

### 3.5.2.2 Administrative Password is

Reports if there is an Administrative password set. There are no options.

### 3.5.2.3 Set User Password

Sets the User password. The password can be up to seven alphanumeric characters.

### 3.5.2.4 Set Administrative Password

Sets the Administrative password. The password can be up to seven alphanumeric characters.

### 3.5.2.5 Unattended Start

Controls when the security password is requested. The User password must be set to enable this field. The options are:

- Enabled (the system boots, but the keyboard is locked until the User password is entered)
- Disabled (**default**)

### 3.5.2.6 Security Hot Key (CTRL-ALT-)

Sets a hot key that locks the keyboard until the User password is entered. All alphabetic keys are valid entries for this field. When a user presses this key while holding down the <Ctrl> and <Alt> keys, the keyboard locks and the keyboard LEDs flash to indicate that the keyboard is locked.

When you enter the User password to unlock the keyboard, you do not have to press <Enter>.

#### ⇒ **NOTE**

*If you set the Security hot key and the APM hot key (see Section 3.4.13.5) to the same key, the APM function has priority.*

## 3.6 Exit Screen

This section describes how to exit Setup with or without saving the changes you have made.

### 3.6.1 Exit Saving Changes

Exits Setup and saves the changes in CMOS RAM. You can also press the <F10> key anywhere in the Setup utility to do this.

### **3.6.2 Exit Discarding Changes**

Exits Setup program without saving any changes. This means that any changes you have made while in Setup are discarded and not saved. Pressing the <Esc> key in any of the four main screens will also exit and discard changes.

### **3.6.3 Load Setup Defaults**

Returns all of the Setup options to their defaults. The default Setup values are loaded from the ROM table. You can also press the <F5> key anywhere in Setup to load the defaults.

### **3.6.4 Discard Changes**

Discards any changes made up to this point in Setup without exiting Setup. This selection loads the CMOS RAM values that were present when the system was turned on. You can also press the <F6> key anywhere in Setup to discard changes.

## 4 Error Messages and Beep Codes

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### 4.1 BIOS Beep Codes

One long beep followed by short beeps indicates a video problem. Table 47 lists the short beeps and describes the associated error messages.

**Table 47. BIOS Beep Codes**

<b>Beeps</b>	<b>Error Message</b>	<b>Description</b>
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error occurred in system memory.
3	Base 64 KB Memory Failure	Memory failure in the first 64 KB.
4	Timer Not Operational	Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning.
5	Processor Error	The processor on the motherboard generated an error.
6	Gate A20 Failure	The keyboard controller may be bad. The BIOS cannot switch to protected mode.
7	Processor Exception Interrupt Error	The processor generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	ROM checksum value does not match the value encoded in BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM failed.

## 4.2 PCI Configuration Error Messages

The following PCI messages are displayed as a group with bus, device, and function information.

**Table 48. PCI Configuration Error Messages**

Message	Explanation
Bad PnP Serial ID Checksum	The Serial ID checksum of a Plug and Play card is invalid.
Floppy Disk Controller Resource Conflict	The floppy disk controller has requested a resource that is already in use.
NVRAM Checksum Error, NVRAM Cleared	The Extended System Configuration Data (ESCD) was reinitialized because of an NVRAM checksum error. Try rerunning the ISA Configuration Utility (ICU).
NVRAM Cleared By Jumper	The Clear CMOS jumper has been moved to the Clear position and CMOS RAM has been cleared.
NVRAM Data Invalid, NVRAM Cleared	Invalid entry in the ESCD.
Parallel Port Resource Conflict	The parallel port requested a resource that is already in use.
PCI Error Log is Full	More than 15 PCI conflict errors have been detected and no additional PCI errors can be logged.
PCI I/O Port Conflict	Two devices requested the same I/O address, resulting in a conflict.
PCI IRQ Conflict	Two devices requested the same IRQ, resulting in a conflict.
PCI Memory Conflict	Two devices requested the same memory resource, resulting in a conflict.
Primary Boot Device Not Found	The designated primary boot device (hard disk drive, diskette drive, or CD-ROM drive) could not be found.
Primary IDE Controller Resource Conflict	The primary IDE controller has requested a resource that is already in use.
Primary Input Device Not Found	The designated primary input device (keyboard, mouse, or other device if input is redirected) could not be found.
Secondary IDE Controller Resource Conflict	The secondary IDE controller has requested a resource that is already in use.
Serial Port 1 Resource Conflict	Serial Port 1 has requested a resource that is already in use.
Serial Port 2 Resource Conflict	Serial Port 2 has requested a resource that is already in use.
Static Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.
System Board Device Resource Conflict	A non Plug and Play ISA card has requested a resource that is already in use.

**Table 49. BIOS Error Messages**

<b>Error Message</b>	<b>Explanation</b>
Gate - A20 Error	Gate A20 on the keyboard controller is not working.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
Cache Memory Bad, Do Not Enable Cache!	Cache memory is defective. Replace it.
CH-2 Timer Error	There is an error in Counter/Timer 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run Setup.
CMOS System Options Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount indicated in CMOS RAM. Run Setup.
CMOS Time and Date Not Set	Run Setup to set the date and time in CMOS RAM.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the system. Use another boot disk and follow the screen instructions.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the system from it. Use another boot disk.
Keyboard Is Locked...Unlock It	The keyboard lock on the system is engaged. The system must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard.
KB/Interface Error	There is an error in the keyboard connector.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) where XXXX is the hex address where the error occurred.
Parity Error ????	Parity error in system memory at an unknown address.

**Table 50. ISA NMI Messages**

<b>NMI Message</b>	<b>Explanation</b>
Memory Parity Error at xxxxx	Memory failed. If the memory location can be determined, it is displayed as xxxxx. If not, the message is Memory Parity Error ?????.
I/O Card Parity Error at xxxxx	An expansion card failed. If the address can be determined, it is displayed as xxxxx. If not, the message is I/O Card Parity Error ?????.
DMA Bus Time-out	A device has driven the bus signal for more than 7.8 microseconds.

# 5 Compliance with Specifications

## 5.1 Specifications

The motherboard complies with the following specifications:

**Table 51. Compliance with Specifications**

Specification	Description	Revision Level
ACP	Advanced Configuration and Power Interface specification	Draft Revision 0.7, June, 1996 Intel Corp., Microsoft Corporation, Toshiba Corporation
APM	Advanced Power Management BIOS interface specification	Revision 1.1, September, 1993 Intel, Microsoft
ATA-33	Synchronous DMA Transfer Protocol specification (to be proposed as Ultra DMA/33 standard)	Revision 0.7, May 21, 1996 Quantum document no. 70-108412-1
COASt	Flexible cache solution for the Intel 430FX, 430HX, 430VX PCIsset	Revision 3.0, February 14, 1996 Intel Corporation
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel, Phoenix Technologies Ltd, SystemSoft Corporation
"El Torito"	Bootable CD-ROM format specification	Version 1.0, January 25, 1995 Phoenix Technologies, IBM Corporation
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2]
Feature Connector	Standard VGA Pass-Through Connector (VSPC)	Video Electronics Standards Association
IrDA	Serial Infrared Physical Layer Link specification	Version 1.1, October 17, 1995 Infrared Data Association.
LPX	LPX de-facto form factor standard	No formal document available
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1996 PCI Special Interest Group
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corp, Phoenix Technologies, Intel
USB	Universal Serial Bus specification	Revision 1.0, January 15, 1996 Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom

## 5.2 Online Support

Find information about Intel motherboards at one of these World Wide Web sites:

<http://www.intel.com/design/motherbd>

<http://developer.intel.com/design/motherbd>

or at this FTP site:

<ftp://ftp.intel.com/pub/>