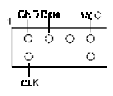
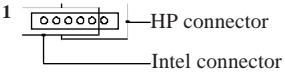


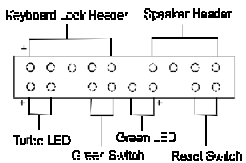
J4: PS/2 mouse connector



J10: IR connector



J16: Front Panel header set



J17: Hard disk LED header



J18: CPU cooling fan header



JP1: Keyboard grounding setting jumper

Short: (default)
Open: to decrease the EMI radiation, while finishing the system assembly.

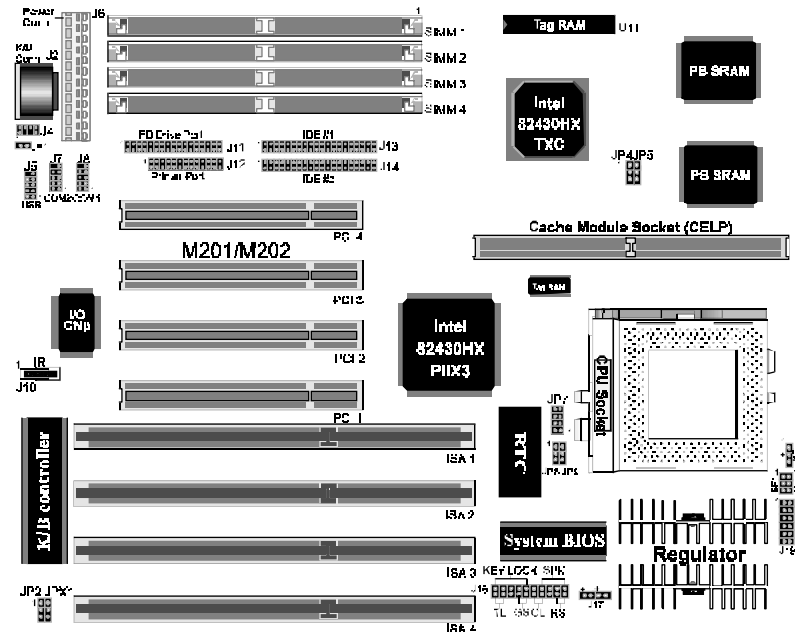
JP2: PS/2 Mouse Enable/Disable setting jumper

1~2 short: Normal (default)
2~3 short: PS/2 mouse disable

JPX1: Password bypass control jumper

1~2 short: Normal (default)
2~3 short: Password bypass

U14: Adding an extra Tag-RAM(8K*8) to expand DRAM cacheable range up to 512MB



JP4, JP5: External cache size jumper setting

Cache size	Cache on Board	Cache Module	JP4, JP5
256KB	32K*32 x 2	--	JP4 JP5 1
512KB	32K*32 x 2	32K*32 x 2	JP4 JP5 1 2

Int. CPU Speed = Speed rate x System clock	BF1	BF2
75/90/100 = 1.5 x system clock	1-2	1-2
110/120/133 = 2 x system clock	2-3	1-2
150/166 = 2.5 x system clock	2-3	2-3
180/200 = 3 x system clock	1-2	2-3

For VRT (Voltage Reduction Technology) processor (such as Intel P55C), the split power plan (CPU's core voltage ≠ CPU's I/O voltage) design is required.

	CPU Core Voltage			CPU I/O Voltage	
	JP7	J19	Core Vcc	J19	I/O Vcc
4			2.5		3.3
5			2.7		
6			2.8		
7			2.9		3.5

CPU-type	Spec.	CPU Power Voltage			System clock		CPU Speed							
		Vcc	J19	JP7	MHz	JP8, JP9	Speed rate	BF1, BF2						
Intel	P54C-75	3.3			50		x1.5							
	P54C-90								3.5		x1.5			
	P54C-120	3.3			60		x2							
	P54C-150	3.5			60		x2.5							
	P54C-180								x3					
	P54C-100	3.3			66		x1.5							
	P54C-133	3.5							66		x2			
	P54C-166												x2.5	
	P54C-200													
	Cyrilx	6x86-P120 ⁺ @100MHz	3.5							50		x2		
6x86-P133 ⁺ @110MHz		55												
6x86-P150 ⁺ @120MHz		60												
6x86-P166 ⁺ @133MHz		66												
AMD	K5-PR75	3.5		50		1.5								
	K5-PR90			60										
	K5-PR100			66										