SF2

Micro ATX Main Board
Internal Specification

For PCB Version 1.X, B Only

Ver. 1.1

September, 2003

HARDWARE DEVELOPMENT DEPARTMENT

INDEX

1. Mainboard Specification

1.1. PCB

- Form Factor: microATX
- Size: 244*230mm
- Layer: 4 layers
- Rear I/O Panel: ECS Rear I/O panel

1.2. CPU

- Type: 1.5G/1.6G/1.7G…2.8G and above
- Socket type: P4 Socket478
- FSB Speed: 400/533/800MHz

1.3. Chipsets

- North Bridge: SiS661FX
- South Bridge: SiS964 / 964L
- LPC Super I/O: ITE8705F
- AC'97 Audio Codec: ALC655
- LAN: RTL8100C
- IEEE1394: VT6307

1.4. Memory Type

- Module Speed: DDR266 / DDR333/ DDR400
- Socket Type: Two DDR 184-pin unbuffered DIMM sockets
- Maximum Memory size: 2GB.

1.5. PCI Slots

- PCI Revision: PCI v2.2 Compliant
- PCI Slots: 3 PCI slots.

1.6. AGP Slot

- AGP Revision: AGP 3.0 Compliant
- AGP slot: 1 AGP slot
- Speed: 4x/8x

1.7. IDE

- Headers: Two 40-pin IDE low profile headers
- Devices: Up to 4 IDE devices
- Speed: PIO mode, ATA100/133

1.8. Serial ATA

- Revision: Serial ATA V1.0 Compliant
- Connectors: Two 7-pin SATA connectors
- Devices: Up to 2 SATA devices
- Speed: 1.5Gbps

1.9. Audio Connectors and Headers

- Real Audio Connector: Line Out, Line In, Microphone In
- One CD-in header (4*1)
- One Aux-in header (4*1)
- One Intel specification audio header (5*2)

1.10. USB Connectors and Headers

- USB Revision: USB V2.0 Compliant
- Connector: Two rear USB connector with 4-ports in rear I/O panel
- Header: Two Intel specification USB header (5*2) with 4-ports in front I/O

1.11. LAN

- Speed: 10/100Mbps
- Connector: Rear RJ45 connector with two status LED

1.12. 1394

- Speed: 400Mbps
- Connector: One rear connector with 1-port in rear I/O panel
- Header: One Intel specification 1394 header (5*2) with 1-port in front I/O

1.13. Misc

- One 34-pin FDD low profile header
- Three 3-pin FAN header: CPU, System, Power
- One 4-pin speaker
- One Intel specification front panel header (5*2)
- One COM connector in rear I/O
- One LPT connector in rear I/O
- One PS/2 keyboard and mouse connector in rear I/O
- One 20-pin ATX power supply connector
- One 4-pin ATX12V power supply connector

2. Chipset Feature

2.1. North Bridge: SiS661FX

- Host interface controller.
  - ✧ Supports Intel Pentiumâ 4 processor family with data transfer rate
  - ✧ Supports Hyper-Threading Technology
  - ✧ Supports 12 outstanding transactions and out-of-order completion
  - ✧ Supports Quasi-synchronous/as ynchronous Host-to-DRAM timing
  - ✧ AGTL+ & AGTL compliant bus driver with auto compensation

- DRAM controller
  - ✧ Supports DDR400/DDR333/DDR266 SDRAM
  - ✧ Supports up to 2 un-buffered DIMM DDR400
  - ✧ Up to 1 GB per DIMM with maximum memory size
  - ✧ Supports 32Mb, 64Mb, 128Mb, 256Mb, 512Mb, 1Gb SDRAM technology with page size from 2KB up to 32 KB
  - ✧ Sustains DDR SDRAM CAS Latency at options of 2, 2.5, & 3 clocks
  - ✧ Supports Suspend-To-RAM (STR).

- AGP controller
  - ✧ AGP 3.0 compliant.
  - ✧ Support 1.5V AGP Interface Only
  - ✧ Supports Graphic Window Size from 4Mbytes to 512Mbytes
  - ✧ Supports Pipelined process in CPU-to-AGP Access
  - ✧ Supports AGP 8X/4X Interface w/ Fast Write Transaction

- High Throughput SiS MuTIOL® 1G interconnecting to SiS964 MuTIOL® 1G Media I/O
  - ✧ Bi-directional 16 bit data bus
  - ✧ Perform 1GB/s bandwidth in 133MHz x 4 mode

- High Quality 3D Accelerator
  - ✧ Built-in 32-bit floating point format VLIW triangle setup engine
  - ✧ Built-in 2 pixel rendering pipelines and 4 texture units
  - ✧ Supports Ultra-AGPII™ up to 2.7GB/s bandwidth

- ✧ Up to 166 MHz 3D engine clock speed
- ✧ Supports 16/24/32 bits integer Z buffer format and 32 bits floating point Z format
- ✧ Supports up to 2048x2048 texture size

- MPEG-2/1 Video Decoder
  - ✧ MPEG-2 ISO/IEC 13818-2 MP@HL and MPEG-1 ISO/IEC 11172-2 standards compliant
  - ✧ Built-in advanced hardware DVD acceleration logic
  - ✧ Supports up to 20 Mbit/sec bit rate decoding
  - ✧ Support VCD, DVD and HDTV (all ATSC modes) decoding
  - ✧ Direct DVD to TV playback

- Video Accelerator
  - ✧ Supports YUV-to-RGB color space conversion
  - ✧ Supports bi-linear video interpolation with integer increments of 1/2048
  - ✧ Supports RGB555, RGB565, YUV422, and YUV420 video playback format
  - ✧ Built-in independent Gamma correction RAM
  - ✧ Supports Direct Draw Drivers

- High Integration
  - ✧ Built-in CRT FIFOs to support ultra high resolution graphics modes and reduce CPU wait-state
  - ✧ Built-in two clock generators for CRT, 2D, 3D and MPEG Engine
  - ✧ Built-in TV Encoder Interface

- Power Management
  - ✧ Supports VESA Display Power Management Signaling (DPMS) compliant VGA monitor for power management
  - ✧ Supports PCI power management configuration registers for supporting ACPI power down controller
  - ✧ Supports clock stopping for video accelerator, 2D, 3D and MPEG decoder when disabled
  - ✧ Supports auto clock throttling for 2D engine, 3D engine

- 839-Balls BGA Package.
- 1.5V Core with Mixed 1.2V, 1.5V, 1.8V, 2.5V and 3.3V I/O CMOS Technology

2.2. South Bridge: SiS964 / 964L

- Support Hi-Precision Event Timer (HPET) for Microsoft Windows
- Multiple DMA Bus Architecture
  - ✧ Concurrent servicing of all DMA Devices: Dual IDE Controllers, SATA controller, USB 1.1 HC, USB 2.0 HC, MAC Controller and Audio/Modem DMA Controller.
  - ✧ Separate 32 Bit Input and Output Data Bus Scheme for each DMA Device
  - ✧ Support isochroous request and continuous packet transmission

- Integrated MuTIOL 1G to PCI Bridge
  - ✧ PCI 2.3 Specification Compliance
  - ✧ Supports up to 6 PCI Masters
  - ✧ Each PCI request can be programmed at one of four level priority

- Dual IDE Master/Slave controller
  - ✧ Integrated Multithreaded I/O Link Mastering with Read Pipelined Streaming
  - ✧ Dual Independent IDE Channels Each with 32 DW FIFO
  - ✧ Supports PIO mode 0,1,2,3,4 and Multiword DMA mode 0,1,2.
  - ✧ Supports Ultra DMA 33/66/100/133.

- Serial ATA Host Controller (SiS964L without SATA Host Controller)
  - ✧ Two independent ports and flexible channel allocation
  - ✧ Compliant with Serial ATA 1.0 Specification
  - ✧ Ultra DMA 150
  - ✧ Support Power saving mode

- Universal Serial Bus Host Controller
  - ✧ Three Independent OHCI USB 1.1 Host Controllers and One EHCI USB 2.0 Host Controller, support up to eight ports
  - ✧ Supports wake-up from S1-S3
  - ✧ Legacy keyboard/mouse support.

- Integrated Audio Controller with AC97 Interface
  - ✧ AC97 v2.2 compliance
  - ✧ 6 channels of AC97 speaker outputs and V.90 HSP-Modem

- Power management
  - ✧ Meets ACPI 2.0 requirements.
  - ✧ Meets APM 1.2 requirements.
  - ✧ ACPI sleep states include S1, S3, S4 and S5.
  - ✧ CPU power states include C0, C1, C2, C3 and C4.
  - ✧ RTC Day-Of Month, Month-Of Year Alarm.
  - ✧ LED blinking in S0, S1, and S3 modes.
  - ✧ System wake-up events include “Power Button”, “Keyboard Password/Hot Key”, “RTC Alarm”, “Modem”, “Ring-In”, "LAN", “AC’97 Wake-Up” and “USB Wake-Up”
  - ✧ PCI bus power management interface Spec. 1.1.
  - ✧ Support one GTL-level input signal used to assert SMI#/SCI#

- Integrated DMA Controller
  - ✧ Two 8237A Compatible DMA Controllers
  - ✧ 8/16- bit DMA Data Transfer

- Keyboard controller.
  - ✧ Supports PS2 mouse interface
  - ✧ System Sleep and Power-Up by Hot-Key
  - ✧ KBC and PS2 mouse can be individually disabled.

- Integrated Interrupt Controller
  - ✧ Two 8259A Compatible Interrupt Controllers for up to 15 interrupts
  - ✧ Programmable Level or Edge Triggered Interrupts
  - ✧ Integrated I/O APIC in Serial Mode or FSB Interrupt Delivery Model for up to 24 Interrupts

- Three 8254 Compatible Programmable 16-bit Counters
  - ✧ System Timer Interrupt
  - ✧ Speaker Tone Output

- Integrated PCI to LPC Bridge
  - ✧ LPC 1.0 compliance.
  - ✧ Support Two Master/DMA devices

- Integrated Real time Clock (RTC) with 512B CMOS SRAM
  - ✧ Supports ACPI Day-of-Month and Month-of-Year alarm
  - ✧ 512 Bytes of CMOS SRAM.

- 505-Balls mBGA Package
- 1.8V Core with Mixed 1.5V, 1.8V, 2.65V and 3.3V I/O CMOS Technology

2.3. AC'97 Audio Codec

- Compliant with AC'97 v2.2 specification
- 18-bit stereo full-duplex CODEC with independent and variable sampling rate
- Advanced power management
- 48-pin LQFP

2.4. LPC Super I/O: ITE8705F

- Low pin count interface
  - ✧ Supports serial IRQ protocol.
  - ✧ Comply with Intel LPC interface Rev1.0.
  - ✧ Supports PCI PME# interface.
- IEEE1284 parallel port
  - ✧ Supports standard mode (bi-directional SPP).
  - ✧ Supports enhanced mode (EPP V1.7 and V1.9 compliant).
  - ✧ Supports high speed (ECP, IEEE1284 compliant).

- UARTS
  - ✧ One for serial port.
  - ✧ One for either serial port or IrDA 1.0/ASKIR.

- Floppy
  - ✧ Supports 1.44/2.88 mode 3 floppy.
  - ✧ 3-mode drives supported.

- Enhanced hardware monitor.
  - ✧ 2 thermal inputs to.
  - ✧ Detect Socket370 CPU/System temperature.
  - ✧ 8 voltage monitor inputs.
  - ✧ Monitors 2 fan tachometer inputs to detect case, CPU fan speed.

- Single 24/48 MHz clock inputs.
- Single +5V power supply.
- 128-pin PQFP.

2.5. LAN Chip: RTL8100C

- Integrated Fast Ethernet MAC, Physical chip and transceiver in one chip.
- 10 Mbps and 100Mbps operation
- PCI local bus single-chip Fast Ethernet controller
  - ✧ Compliant to PCI Revision 2.2
  - ✧ Supports PCI clock 16.75MHz-40MHz
  - ✧ Supports ACPI, PCI power management

- Compliant to PC99/PC2001 standard
- Supports Wake-On-LAN function and remote wake-up.
- Supports auxiliary power-on internal reset.
- Advanced power saving mode when LAN function or wakeup function is not used
- Supports Full Duplex Flow Control (IEEE 802.3x)
- 2.5/3.3V power supply with 5V tolerant I/Os.
- 0.25u CMOS process
- 128 pin QFP/LQFP

2.6. IEEE1394: VT6307

- Single Chip PCI Host Controller for IEEE 1394-1995 Release 1.0 and IEEE 1394a-2000
- Compliant with 1394 Open HCI Specifications v1.0 and v1.1
- 32-Bit Power-Managed PCI Bus Interface
  - ✧ Compliant with PCI specification v2.2
  - ✧ Compliant with PCI Bus Power Management Specification v1.1
  - ✧ Supports power states D0, D1, D2, D3hot, and D3 cold

- Integrated 400 Mbit 2-Port PHY
  - ✧ Provides two 1394a fully compliant cable ports at 100 / 200 / 400 Mbit per second
  - ✧ Host notification of PHY LinkOn events
  - ✧ Incoming data resynchronized to local clock.
  - ✧ Cable power presence monitoring.
  - ✧ Separate TPBIAS for each port

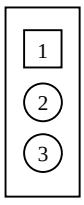
- 3.3V Power Supply with 5V Tolerant Inputs
- 0.3 μm, Low Power CMOS Process
- 128-Pin PQFP

3. Jumper Setting

Location	Header Type	Description	Function
JP1	Header 3*1	Clear CMOS	1-2: Normal 2-3: Clear
JP3	Header 3*1	BIOS Protection	1-2: Write Enable 2-3: Write Disable
JP4	Header 3*1	Reserved	1-2: Reserved 2-3: Reserved
JP5	Header 3*1	Reserved	1-2: Reserved 2-3: Reserved
JPT1	Header 3*1	COM1 Pin9 Function Selection	1-2: Ring 2-3: VCC
JPT2	Header 3*1	COM2 Pin9 Function Selection	1-2: Ring 2-3: VCC
JPT3	Header 3*1	Reserved	1-2: Reserved 2-3: Reserved

*ECS may make changes at any time, without notice.

3.1. JP1, JP3, JP4, JP5, JPT1, JPT2, JPT3



4. Header Definition

Name	Connector type	Description	Notes
PSKBM1	MINI-6P-DUAL	PS/2 Keyboard and Mouse Connector	Fig-(4.1)
COM1	CONN-9P2R-90M	Serial Port 1	Fig-(4.2)
VGA1	CONN.D-TYPE-15P3R	VGA Port	Fig-(4.3)
LPT1	CONN-25P2R-90FM-DM	Parallel Port	Fig-(4.4)
USBLAN1	USB-DUAL/LAN	USB Dual Port + LAN Connector	Fig-(4.5)
USB1394A1	USB-DUAL/IEEE1394	USB Dual Port + IEEE1394 Connector	Fig-(4.6)
JS1	Triple Stacked Jack	Rear Audio Connector	Fig-(4.7)
FDD1	H17*2LW	Floppy Connector	Fig-(4.8)
IDE1	H20*2LW	HDD Primary Connector	Fig-(4.9)
IDE2	H20*2LW	HDD Secondary Connector	Fig-(4.9)
CPUFAN1	AMP640456-3	CPU Fan Header	Fig-(4.10)
CASFAN1	AMP640456-3	Chassis Fan Header	Fig-(4.10)
NBFAN1	AMP640456-3	North Bridge Fan Header	Fig-(4.10)
COM2	H5*2	COM2 header	Fig-(4.11)
CDIN1	H4*1	CD-in Header	Fig-(4.12)
AUXIN1	H4*1	Auxiliary Audio Input Header	Fig-(4.13)
SPDIFO1	H4*1	SPDIF-out Header	Fig-(4.14)
AUDIO1	H5*2	Front Audio Header with Intel spec.	Fig-(4.15)
USB3, USB4	H5*2	USB Header with Intel spec.	Fig-(4.16)
1394A2	H4*2	IEEE1394 Header with Intel spec.	Fig-(4.17)
PANEL1	H5*2	Front Panel with Intel spec.	Fig-(4.18)
SATA1, SATA2	CONN.SATA 7P 2R	Serial ATA Connector	Fig-(4.19)

4.1. PSKBM1

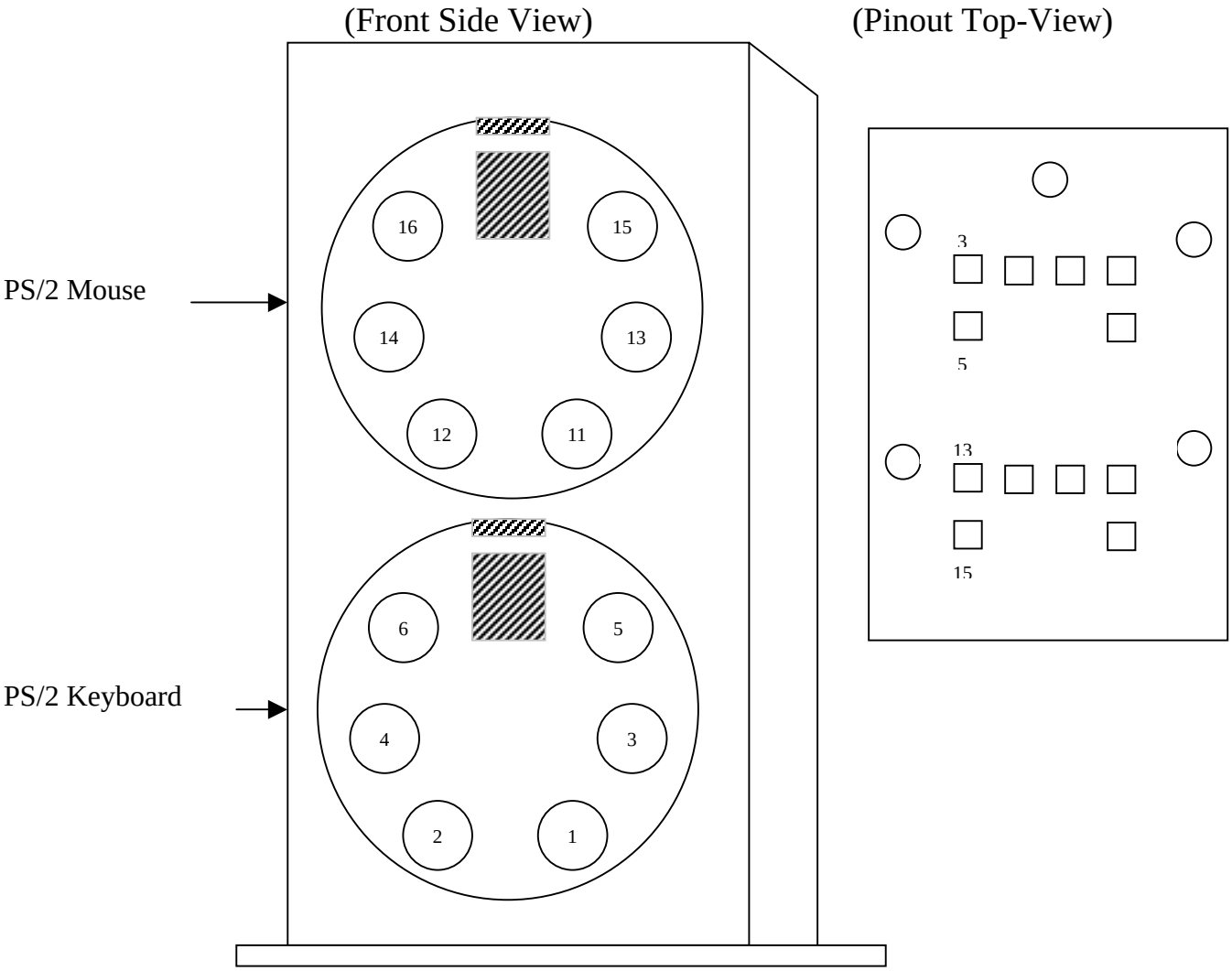
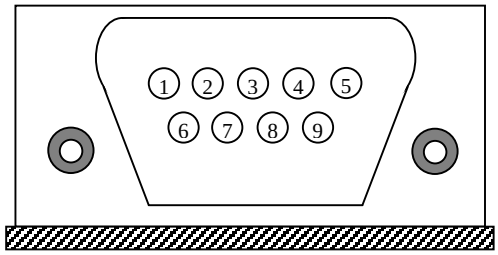


Figure-(4.1)

PS/2 Keyboard		PS/2 Mouse	
1	KBDATA	11	MDATA
2	NC	12	NC
3	Ground	13	Ground
4	VCC	14	VCC
5	KBCLK	15	MCLK
6	NC	16	NC

4.2. COM1

Front Side View



Pinout Top-View

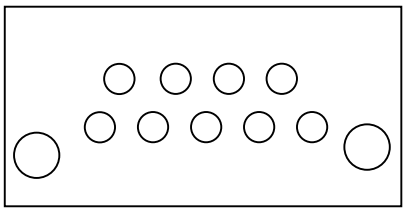
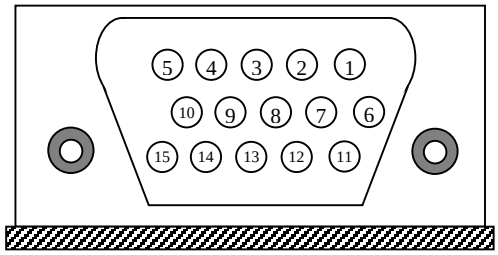


Figure-(4.2)

Pin	Signal Name
1	DCD
2	RxD
3	TxD
4	DTR
5	Ground
6	DSR
7	RTS
8	CTS
9	RI

4.3. VGA1

Front Side View



Pinout Top-View

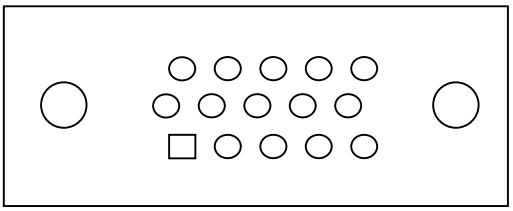
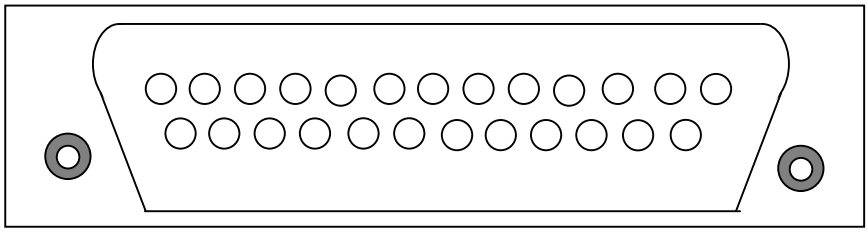


Figure-(4.3)

Pin	Signal Name
1	RED
2	GREEN
3	BLUE
4	NC
5	GND
6	GND
7	GND
8	GND
9	NC
10	GND
11	NC
12	DDC1DATA
13	HSYNC
14	VSYNC
15	DDC1CLK

4.4. LPT1

Front Side View



Pinout Top-View

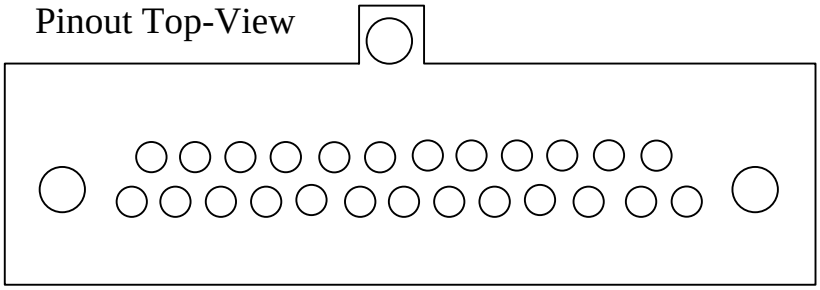


Figure-(4.4)

Pin	Signal Name	Pin	Signal Name
1	STROBE	13	SLCT
2	PD0	14	ALF
3	PD1	15	ERROR
4	PD2	16	INIT
5	PD3	17	SLCTIN
6	PD4	18	Ground
7	PD5	19	Ground
8	PD6	20	Ground
9	PD7	21	Ground
10	ACK	22	Ground
11	BUSY	23	Ground
12	PE	24	Ground
		25	Ground

4.5. USBLAN1

(Pinout Top-View)

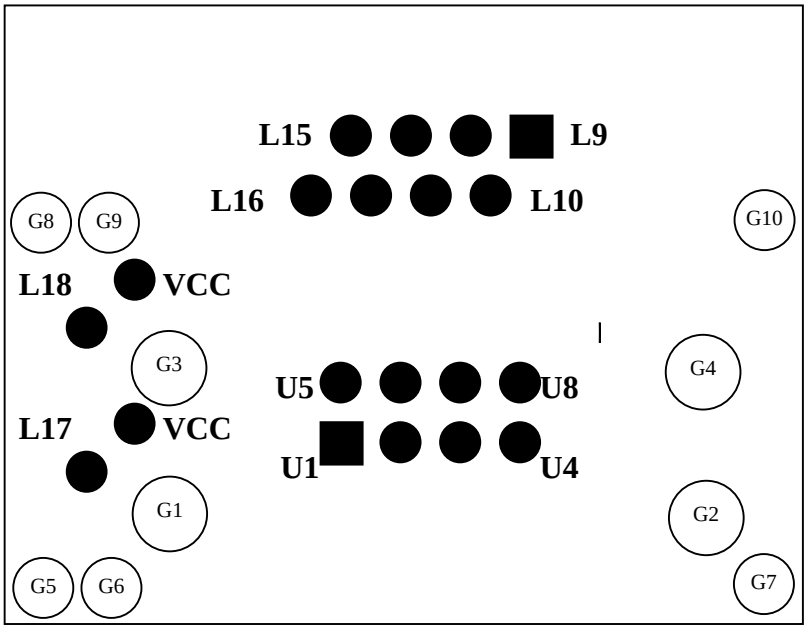


Figure-(4.5)

Pin	Signal Name	Pin	Signal Name
U1	VCC	G7	HOLE_LAN
U2	-DATA0	G8	HOLE_LAN
U3	+DATA0	G9	HOLE_LAN
U4	GND	G10	HOLE_LAN
U5	VCC	L1	TX+
U6	-DATA1	L2	TX-
U7	+DATA1	L3	RX+
U8	GND	L4	NC
G1	HOLE_USB	L5	NC
G2	HOLE_USB	L6	RX-
G3	HOLE_USB	L7	NC
G4	HOLE_USB	L8	NC
G5	HOLE_LAN	L17	PLED0
G6	HOLE_LAN	L18	PLED1

4.6. USBIEEE1

(Pinout Top-View)

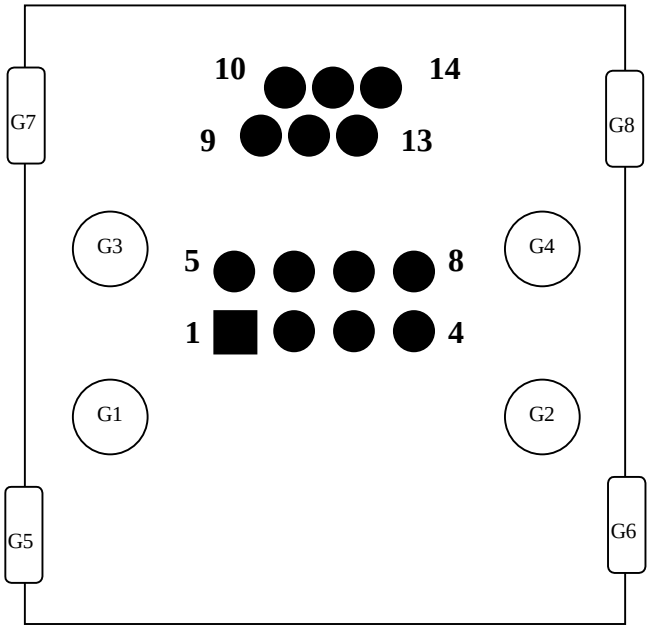


Figure-(4.6)

Pin	Signal Name	Pin	Signal Name
1	VCC	G1	HOLE
2	-DATA0	G2	HOLE
3	+DATA0	G3	HOLE
4	GND	G4	HOLE
5	VCC	G5	HOLE
6	-DATA1	G6	HOLE
7	+DATA1	G7	HOLE
8	GND	G8	HOLE
9	VP		
10	VG		
11	TPB-		
12	TPB+		
13	TPA-		
14	TPA+		

4.7. JS1

(Pinout Top-View)

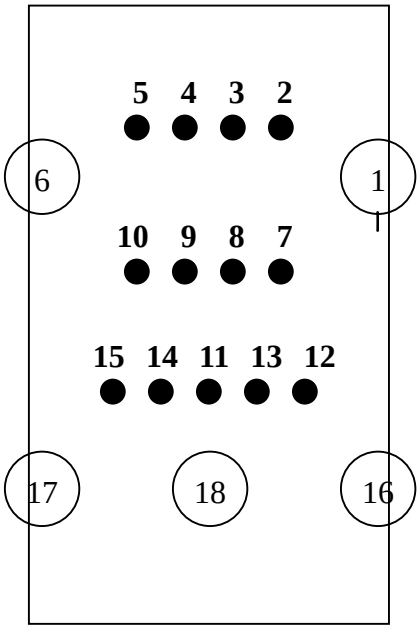


Figure-(4.7)

Pin	Signal Name	Pin	Signal Name
1	HOLE	10	ROUTL2
2	LINL1	11	GND
3	LSW1	12	LMIC3
4	RSW1	13	LSW3
5	LINR1	14	RSW3
6	HOLE	15	RMIC3
7	LOUTL2	16	HOLE
8	LSW2	17	HOLE
9	RSW2	18	HOLE

4.8. FDD1

(Top-View)

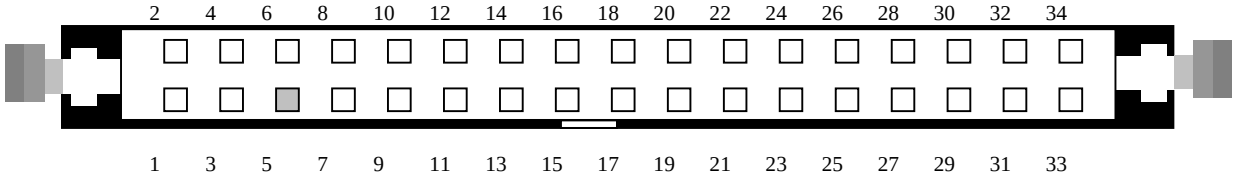


Figure-(4.8)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DRVDEN0
3	Ground	4	HDL-
5	Keypin	6	DS3-
7	Ground	8	INDEX-
9	Ground	10	MTR0-
11	Ground	12	DS0-
13	Ground	14	DS1-
15	Ground	16	MTR1-
17	Ground	18	DIR-
19	Ground	20	STEP-
21	Ground	22	WDATA
23	Ground	24	WGATE-
25	Ground	26	TRK0-
27	Ground	28	WP-
29	Ground	30	RDATA
31	Ground	32	HDSEL-
33	Ground	34	DSKCHG-

4.9. IDE1 & IDE2

(Top-View)

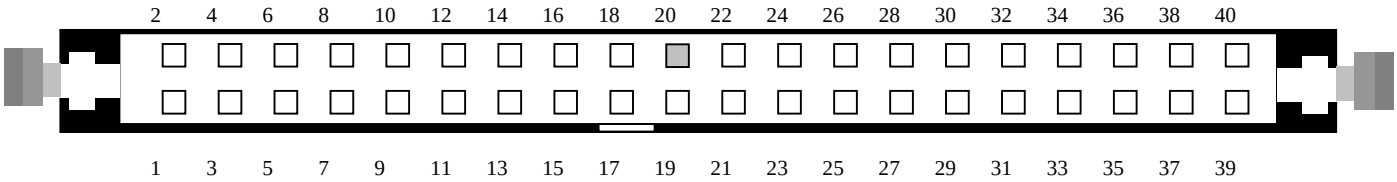
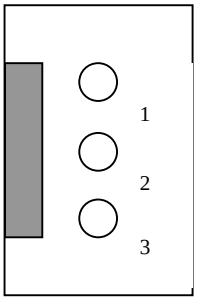


Figure-(4.9)

Pin	Signal Name	Pin	Signal Name
1	RESET-	2	Ground
3	DD7	4	DD8
5	DD6	6	DD9
7	DD5	8	DD10
9	DD4	10	DD11
11	DD3	12	DD12
13	DD2	14	DD13
15	DD1	16	DD14
17	DD0	18	DD15
19	Ground	20	Keypin
21	DMARQ	22	Ground
23	DIOW-	24	Ground
25	DIOR-	26	Ground
27	IORDY	28	PSYNC:CSEL
29	DMACK-	30	Ground
31	INTRQ	32	IOCS16-
33	DA1	34	PDIAG-
35	DA0	36	DA2
37	CS1FX-	38	CS3FX-
39	DASP-	40	Ground

4.10. CPUFAN1, CASEFAN1, NBFAN1

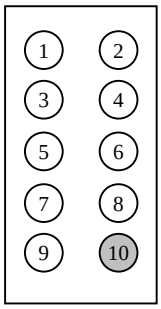
(Top-View)



Pin	Signal Name
1	Ground
2	+12V
3	SENSE

Figure-(4.10)

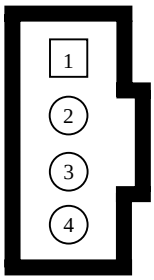
4.11. COM2



Pin	Signal Name	Pin	Signal Name
1	DCD	2	RxD
3	TxD	4	DTR
5	Ground	6	DSR
7	RTS	8	CTS
9	RI	10	KEY

Figure-(4.11)

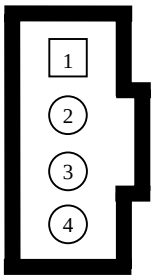
4.12. CDIN1



Pin	Signal Name
1	CD_L
2	GND
3	GND
4	CD_R

Figure-(4.12)

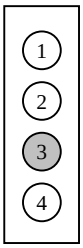
4.13. AUXIN1



Pin	Signal Name
1	AUX_L
2	GND
3	GND
4	AUX_R

Figure-(4.13)

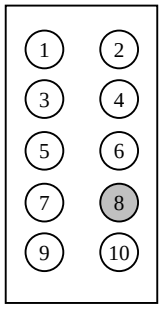
4.14. SPDIFO1



Pin	Signal Name
1	SIGNAL
2	VCC
3	KEY
4	GND

Figure-(4.14)

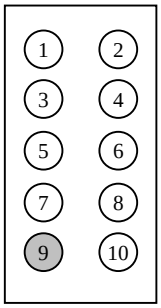
4.15. AUDIO1



Pin	Signal Name	Pin	Signal Name
1	AUD_MIC	2	AUD_GND
3	MIC_BIAS	4	AUD_VCC
5	AUD_F_R	6	AUD_RET_R
7	REVD	8	KEY
9	AUD_F_L	10	AUD_RET_L

Figure-(4.15)

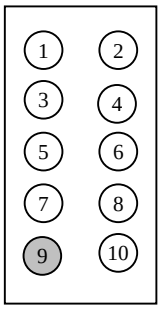
4.16. USB3, USB4



Pin	Signal Name	Pin	Signal Name
1	USBPWR0	2	USBPWR1
3	USB_FP_P0-	4	USB_FP_P1-
5	USB_FP_P0+	6	USB_FP_P1+
7	GND	8	GND
9	KEY	10	USB_FP_OC0

Figure-(4.16)

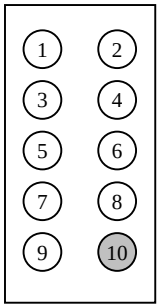
4.17. 1394A2



Pin	Signal Name	Pin	Signal Name
1	TPA+	2	TPA-
3	GND	4	GND
5	TPB+	6	TPB-
7	VCCBUS	8	VCCBUS
9	KEY	10	GND

Figure-(4.17)

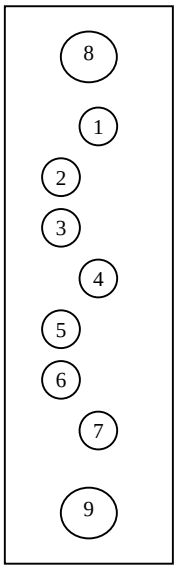
4.18. PANEL1



Pin	Signal Name	Pin	Signal Name
1	HD_LED_P	2	PWR_SLP
3	HD_LED_N	4	PWR_SLP
5	RST_SW_N	6	PWR_SW_P
7	RST_SW_P	8	PWR_SW_N
9	RSVD	10	KEY

Figure-(4.18)

4.19. SATA1, SATA2



Pin	Signal Name
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND
8	HOLE
9	HOLE

Figure-(4.19)

5. Rear I/O Panel Connectors