# CU430HX Motherboard
# Technical Product Specification

Order Number 281839-002

February 1997

The CU430HX motherboard may contain design defects or errors known as errata. Characterized errata that may cause the CU430HX motherboard's behavior to deviate from published specifications are documented in the CU430HX Motherboard Specification Update.

# Revision History

| Revision | Revision History | Date |
|---|---|---|
| -001 | Initial release of the CU430HX Technical Product Specification. | 8/96 |
| -002 | Incorporate minor changes. | 2/97 |

This product specification applies only to standard CU430HX motherboards with BIOS identifier 1.00.0X.DK0.

Changes to this specification will be published in the CU430HX Motherboard Specification Update before being incorporated into a revision of this document.



Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-879-4683, Europe 44-0-1793-431-155, France 44-0-1793-421-777, Germany 44-0-1793-421-333, other Countries 708-296-9333.

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# 1 Motherboard Description

## 1.1 Overview

The CU430HX motherboard has been designed for use in the commercial desktop market. The CU430HX motherboard supports the following set of features:

- Uses a 9-inch by 13-inch LPX form factor.
- Uses a type 7 Zero Insertion Force (ZIF) socket to house any of the Intel Pentium® processors, and provides an upgrade path to future Pentium OverDrive® processors.
- Accepts Pentium processors with core clock frequencies of 75 MHz, 90/100 MHz, 120 MHz, 133 MHz, 150 MHz, 166 MHz, and 200 MHz.
- Uses Intel's 82430HX PCIset. The Intel 82371SB PCI/ISA IDE Xccelerator (PIIX3) provides an integrated Bus Mastering IDE controller with two high performance IDE interfaces for up to four devices (such as hard drives or CD-ROM).
- Supports up to 192 MB of DRAM using six standard 72-pin tin lead SIMM † sockets that accept Fast Page Mode (FPM) and Extended Data Out (EDO) memory. Both non-parity (32-bit wide) and parity (36-bit wide), as well as ECC memory SIMMs are supported.
- Uses a Flash BIOS with the following features:
  - Uses both hardware and software Secure Flash features to protect Flash contents from corruption.
  - Uses a BIOS that complies with the Desktop Management Interface (DMI-compliant).
- Uses the National PC87306BV I/O controller to integrate the following standard PC I/O functions:
  - floppy interface,
  - two FIFO serial ports,
  - one EPP/ECP capable parallel port,
  - a Real Time Clock,
  - keyboard controller,
  - support for an IrDA† and Consumer Infra Red compatible interface.
- Integrates an ATI† Mach64GT graphics controller with SGRAM graphics memory to support SVGA graphics at resolutions up to 1280 x 1024 with 1MB of SGRAM installed. Supports up to 4MB of graphics memory using an add-in module from ATI.
- Integrates a business audio solution using a Creative Laboratories 16C audio codec on the motherboard to provide 16-bit stereo, Sound Blaster Pro† compatible audio.
- Integrates a complete LAN interface onboard using the Intel 82557 LAN controller.
- Provides an onboard telephony (modem) connector to support the latest telephony applications.
- A hardware monitoring ASIC provides the following monitoring functions:
  - Integrated temperature sensor
  - Fan speed monitoring
  - Power supply voltage monitoring
  - Storage of POST results and error codes

- Back panel connectors are provided for video and audio, the PS/2 keyboard/mouse, a parallel interface, an RJ45 LAN interface, and the serial interface. An optional Universal Serial Bus (USB) connector provides two USB connectors instead of the single serial DB9 connector.
- PCI and ISA expansion slots are supported by a connector on the motherboard designed to accept a riser card. An on-board jumper allows support of risers with either two or three PCI slots.

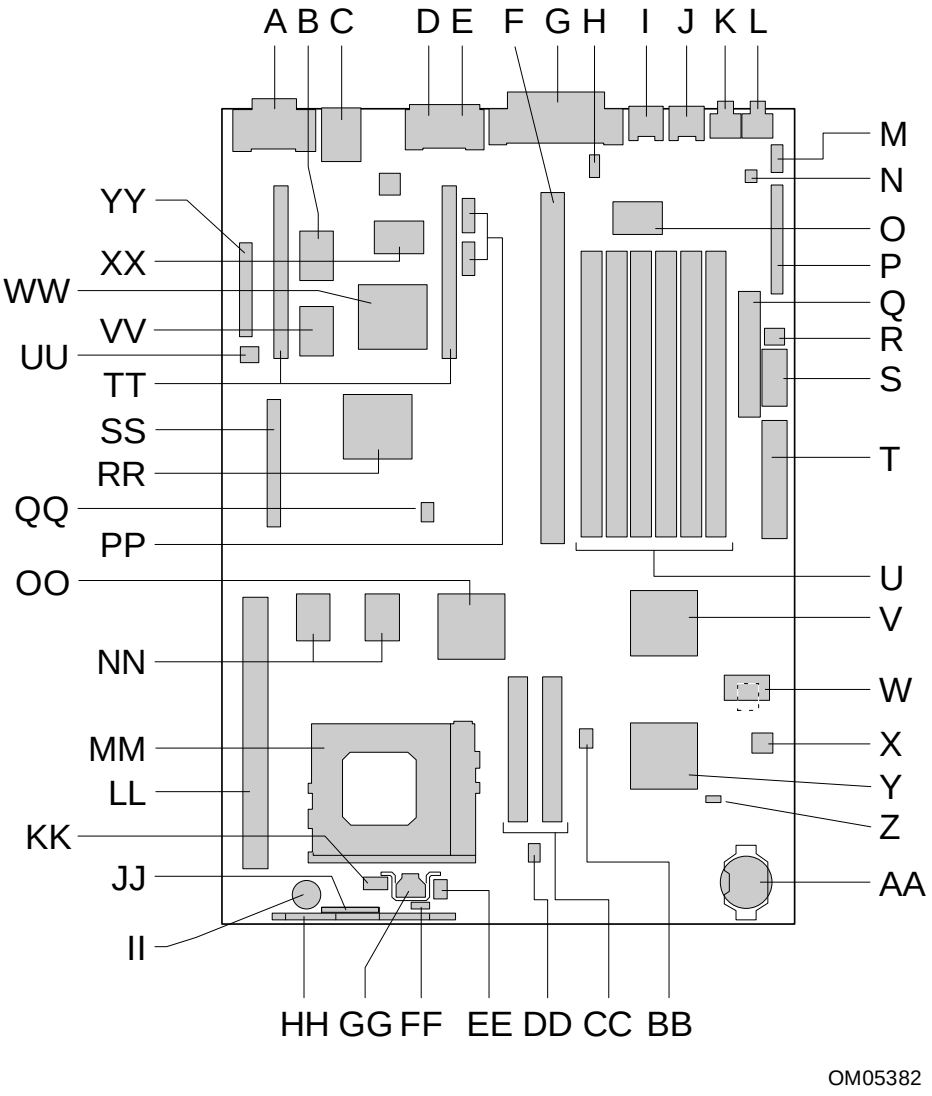


**Figure 1. Motherboard Features**

**Table 1. Key to Motherboard Features**

| Key | Description | Key | Description | Key | Description |
|---|---|---|---|---|---|
| A | VGA connector (15-pin, J1N1) | B | SGRAM, video, 128Kx32x2 (U2L2) | C | LAN connector (RJ45, J2N1) |
| D | Side-by-side USB connector option (4x1x2, J4N1) | E | Serial connector option (9-pin, J4N2) | F | ISA/PCI riser socket (J6J2) |
| G | Parallel connector (DB25, J6N1) | H | CD Audio header (1x4, J6N2) | I | PS/2 Mouse connector (J7N1) |
| J | PS/2 Keyboard Connector (J8N1) | K | Microphone input jack (J8N2) | L | Audio output jack (J9N2) |
| M | Wave Table header (2x4, J9N1) | N | Telephony (modem) header (2x2, J9M1) | O | Creative Labs Vibra16C audio controller (U7M1) |
| P | MIDI/Audio header (2x17,J9L1) | Q | Floppy connector (J9K1) | R | Soft-OFF header (1x3, J9K2) |
| S | Std 3.3V power connector (J9J1) | T | Main power connector (J9H1) | U | SIMM sockets (J6J1, J7J1, J7J2, J7J3, J8J1, J8J2) |
| V | National PC87306B Ultra I/O controller (U7E1) | W | Flash BIOS TSOP/PSOP(E28F002, U9D1, U9D2) | X | Hardware monitor ASIC (U9C1) |
| Y | Intel SB82371SB (PIIX3, U7C1) | Z | Intrusion-detect photo-transistor (Q8B1) | AA | Real-time clock battery (BT9A1) |
| BB | Flash recovery jumper block (2x3, J6C2) | CC | IDE connectors (J5C1, J6C1) | DD | Vcc regulator header (2x3, J5B1) |
| EE | 3-wire fan header (1x3, J4A4) | FF | Keyboard lock header (1x3, J4A3) | GG | Voltage regulator (U3A1) |
| HH | Front panel connector (1x29, J4A1) | II | Onboard speaker (LS2A1) | JJ | Front panel header 2 (1x9, J2A2) |
| KK | PWR/HDD LED header (1x4, J3A2) | LL | CELP socket (J1D1) | MM | Socket 7 Pentium processor socket (U3C1) |
| NN | Mcache PBSRAM (32Kx32, U3E1, U2E1) | OO | Intel FW82439HX (TXC, U4E1) | PP | COM1/COM2 header (5x2, J4L1, J4M1) |
| QQ | Jumper block, 2/3 PCI slot (2x3, J4G1) | RR | ATI 264GT-B video controller (U3H1) | SS | VGA header (2x20, J1H1) |
| TT | Video memory upgrade header (2x27, J1L1, J4L2) | UU | Security header (1x2, J1K1) | VV | SGRAM, video, 128Kx32x2 (U2K2) |
| WW | LAN Controller (82557, U3K1) | XX | National DP83840 (U3L1) | YY | Jumper block header (J1K2) |

## 1.2 Motherboard Manufacturing Options

Contact your local Intel Field Sales Office for options and ordering information.

## 1.3 Form Factor

The CU430HX motherboard is designed to fit into a standard LPX form factor chassis. Figure 2 illustrates the mechanical form factor for the CU430HX motherboard. Location of the I/O connectors, riser slot, and mounting holes are in strict compliance with the LPX specification.

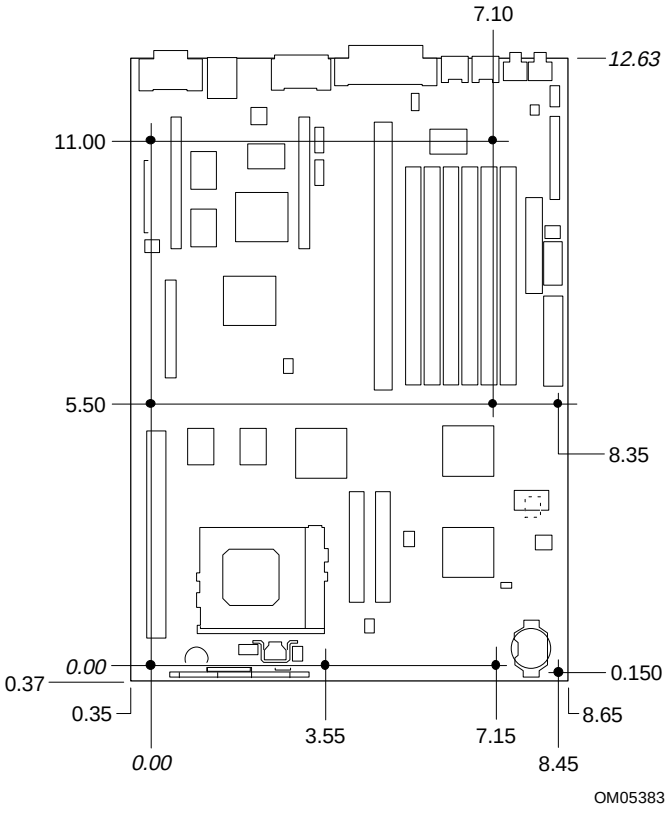


**Figure 2. Motherboard Dimensions**

## 1.4 Microprocessor

The CU430HX motherboard is designed to operate with 3.3 volt Pentium processors. An onboard linear voltage regulator circuit provides the required 3.3 volts from the 5.0 volt tap of the power supply. An on-board jumper enables use of OverDrive processors and Pentium processors with MMX™ technology. All Pentium processors (those running internally at 75, 90, 100, 120, 133, 150, 166, and 200 MHz) are supported.

The Pentium processor maintains full backward compatibility with the 8086, 80286, Intel386™ and Intel486™ processors. It supports both read and write burst mode bus cycles, and includes separate 8 KB on-chip code and data caches that employ a write-back policy. The Pentium processor has an advanced numeric coprocessor that significantly increases the speed of floating point operations, while maintaining backward compatibility with math coprocessors that comply with ANSI/IEEE standard 754-1985.

### 1.4.1 Microprocessor Upgrade

The CU430HX motherboard provides a 321-pin Socket 7 ZIF processor socket. Socket 7 supports a processor upgrade path that includes all Pentium OverDrive processors.

### 1.4.2 Main System Memory

The board has six 72-pin, tin lead SIMM sockets, arranged as three banks, each with two sockets. Some important considerations are:

- The board supports Fast Page Mode (FPM) memory in 70ns (or faster) SIMMs, and either 70ns or 60ns Extended Data Out (EDO) SIMMs. If the maximum host bus speed is 60MHz or slower, 70ns EDO DRAM can be used.
- The board supports both parity and ECC memory.
- Both sockets of a bank must be used.
- Both sockets of a bank must contain the same type (fast page or EDO), speed (60 or 70ns), and size of SIMM.
- You can have different types, speeds, and sizes in different banks.
- Only tin lead 72-pin SIMMs can be used with the standard tin lead SIMM sockets.
- There are no jumper settings required for the memory size or type. This information is automatically detected by the system BIOS.

The sockets support the following SIMM sizes:

| SIMM Size | Configuration (without parity) | Configuration (with parity) |
|---|---|---|
| 4 MB | 1 M x 32 | 1 M x 36 |
| 8 MB | 2 M x 32 | 2 M x 36 |
| 16 MB | 4 M x 32 | 4 M x 36 |
| 32 MB | 8 M x 32 | 8 M x 36 |

## 1.5 Chipset

The Intel 82430HX PCIset consists of the 82439HX Xcelerated Controller (TXC) and one 82371SB PCI/ISA IDE Xcelerator (PIIX3) bridge chip.

### 1.5.1 82439HX Xcelerated Controller (TXC)

The 82439HX provides all control signals necessary to drive a second level cache and the DRAM array, including multiplexed address signals. The TXC also controls system access to memory and generates snoop controls to maintain cache coherency. The TXC comes in a 324-pin BGA package and includes the following features:

- CPU interface control
- Integrated L2 write-back cache controller
  - — Pipeline burst SRAM
  - — 256 or 512 KB direct-mapped
- Integrated DRAM controller
  - — 64 bit path to memory
  - — Support for EDO and fast page DRAM
  - — 8 MB to 512 MB main memory
  - — Parity, non-parity, and ECC memory support
- Fully synchronous PCI bus interface
  - — 25/30/33 MHz
  - — PCI to DRAM > 100 Mbytes/sec
  - — Up to 4 PCI masters in addition to the PIIX3 and IDE.

### 1.5.2 82371SB PCI/ISA IDE Xcelerator (PIIX3)

The PIIX3 provides the interface between the PCI and ISA buses and integrates a dual channel fast IDE interface capable of supporting up to four devices. The PIIX3 integrates seven DMA channels, one 16-bit timer/counter, two eight-channel interrupt controllers, PCI-to-AT interrupt mapping circuitry, NMI logic, ISA refresh address generation, and PCI/ISA bus arbitration circuitry together on the same device. The PIIX3 comes in a 208-pin QFP package and includes the following features.

- Interface between the PCI and ISA buses
- Universal Serial Bus controller
  - — Host/hub controller
- Integrated fast IDE interface
  - — Support for up to four devices
  - — PIO Mode 4 transfers up to 16 MB/sec
  - — Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers
  - — Bus master mode
- PCI 2.1 compliant
- Enhanced fast DMA controller
- Interrupt controller and steering
- Counters/timers
- SMI interrupt logic and timer with fast on/off mode

### 1.5.3 Universal Serial Bus (USB) Support

The CU430HX motherboard optionally provides two USB ports. This permits connection of two USB peripheral devices directly to the system without an external hub. If more devices are required, an external hub can be connected to either of the built-in ports. The CU430HX motherboard completely supports the standard universal host controller interface (UHCI) and takes advantage of the standard software drivers written to be compatible with UHCI. Features of the USB include:

- Support for hot swapping of Plug and Play devices without opening the system chassis.
- Both low-speed and high-speed devices can be intermixed on the bus.
- Self-identifying peripherals.
- Automatic mapping of function to driver and configuration.
- Support for isochronous and asynchronous transfer types over the same set of wires.
- Support for up to 127 physical devices.
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications.
- Error handling and fault recovery mechanisms built into protocol.
- Low cost cables and connectors.

### 1.5.4 IDE Support

The motherboard provides two independent high performance bus-mastering PCI IDE interfaces capable of supporting PIO Mode 3 and Mode 4 devices. The system BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Sector Head (ECHS) translation modes as well as ATAPI (e.g. CD-ROM) devices on both IDE interfaces. Detection of IDE device transfer rate and translation mode capability is automatically determined by the system BIOS.

Programmed I/O operations normally require a substantial amount of CPU bandwidth. In true multi-tasking operating systems like Windows† 95, the CPU bandwidth freed up by using bus mastering IDE can be used to complete other tasks while disk transfers are occurring. When used in conjunction with the appropriate driver for the Windows 95 environment, the IDE interface can operate as a PCI bus master capable of supporting PIO Mode 4 devices with transfer rates of up to 16 MB/sec.

## 1.6 Super I/O Controller (National PC87306B)

Control for the integrated serial ports, parallel port, floppy drive, RTC and keyboard controller is incorporated into a single component, the National Semiconductor 306BV. This component provides:

- Two NS16C550-compatible UARTs with send/receive 16 byte FIFO
- Support for an IrDA compliant Infra Red interface
- Multi-mode bi-directional parallel port
  - — Standard mode; IBM and Centronics compatible
  - — Enhanced Parallel Port (EPP) with BIOS/Driver support
  - — High Speed mode; Extended Capabilities Port (ECP) compatible
- Industry standard floppy controller with 16 byte data FIFO (2.88 MB floppy support)

- Integrated Real Time Clock accurate within +/- 13 minutes/yr at 25º C and 5 volts when the system is continuously powered on.
- Integrated 8042 compatible keyboard controller

By default, the 306BV interfaces are automatically configured by the BIOS during boot-up. You can also manually configure the interfaces with the BIOS Setup utility. Chapter 3 describes and tells how to invoke the BIOS Setup utility.

### 1.6.1 Floppy Controller

The I/O controller is software compatible with the DP8473 and 82077 floppy disk controllers. You can configure the floppy interface for 360 KB or 1.2 MB 5¼ inch media, or for 720 KB, 1.2 MB, 1.44 MB, or 2.88 MB 3½ inch media with the BIOS setup utility. By default, the Floppy A interface is configured for 1.44 MB and Floppy B is disabled. A Setup option makes it possible to prevent a user from being able to write to a floppy drive. A driver is required for configuring the floppy interface for 1.2 MB 3.5-inch (3-mode floppy) operation.

### 1.6.2 Keyboard and Mouse Interface

PS/2† keyboard and mouse connectors are located on the back panel side of the motherboard. The 5V lines to these connectors are protected with a PolySwitch† circuit that acts much like a self-healing fuse, re-establishing the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, you should still be sure to turn off the system power before installing or removing a keyboard or mouse.

**NOTE**

*Although they are labeled as "Keyboard" and "Mouse" on the motherboard and the back panel, the PS/2 keyboard/mouse connectors can be used interchangeably for either keyboard or mouse. The BIOS detects the attached devices during POST, and configures the system accordingly.*

The integrated 8042 microcontroller contains the AMI Megakey keyboard and mouse controller code that, besides providing traditional keyboard and mouse control functions, supports Power-On/Reset (POR) password protection. The POR password can be defined by the user via the Setup program. The keyboard controller also provides for the following "hot key" sequences:

- <CTRL><ALT><DEL>: System software reset. This sequence performs a software reset of the system by jumping to the beginning of the BIOS code and running the POST operation.
- <CTRL><ALT><+> and <CTRL><ALT><->: Turbo mode selection.
- <CTRL><ALT><-> sets the system for de-turbo mode, emulating an 23 MHz AT.
- <CTRL><ALT><+> sets the system for turbo mode. Changing the Turbo mode may be prohibited by an operating system, or when the CPU is in Protected mode or virtual x86 mode under DOS.
- <CTRL><ALT><defined in setup>: Power down and coffee-break key sequences take advantage of the SMM capabilities of the Pentium processor to greatly reduce the system's power consumption while maintaining the responsiveness necessary to service external interrupts.

- <CTRL><ALT><defined in setup>: Keyboard lock key sequence provides system security by blanking the screen and ignoring keyboard input until the BIOS User Password is typed. When the Keyboard lock sequence is invoked, the keyboard LEDs will flash to indicate that the User Password must be entered to unlock the system. This feature will not take effect unless the User Password has been set in the BIOS setup.

### 1.6.3 Real-time Clock, CMOS RAM and Battery

The integrated real-time clock (RTC) is DS1287 and MC146818 compatible and provides a time of day clock, 100-year calendar with alarm features and is accurate to within 13 minutes per year. The RTC can be set via the BIOS SETUP program. The RTC also supports 242-byte battery-backed CMOS RAM in two banks which is reserved for BIOS use. The CMOS RAM can be set to specific values or cleared to the system default values using the BIOS SETUP program. Also, the CMOS RAM values can be cleared to the system defaults by using a configuration jumper on the motherboard.

An external coin-cell style battery provides power to the RTC and CMOS memory. The battery has an estimated lifetime of three years if the system is not plugged into the wall socket. When the system is plugged in, power is supplied from the power supply 5v standby current to extend the life of the battery.

### 1.6.4 Infrared Support

A 5-pin header connector is provided to allow connection to a Hewlett Packard HSDSL-1000 compatible Infra-red (IrDA) transmitter/receiver. Once the module is connected to the header, Serial port 2 can be re-directed to the IrDA module. Once configured for IrDA, the user can transfer files to or from portable devices such as laptops, PDA's and printers using application software such as LapLink†. The IrDA specification provides for data transfers at 115 Kbps from a distance of 1 meter.

The Consumer Ir is receive only (for the motherboard) and can be used to control telephony functions and multimedia operation such as volume control, CD track change, and related functions.

### 1.6.5 Parallel Port

The parallel port can be configured in the BIOS setup as output only compatible mode, bi-directional mode, ECP or EPP modes. The parallel port can also be assigned to I/O addresses 278H, 378H, or 3BCH and IRQ's 5 or 7. Furthermore, a routable DMA scheme allows Plug and Play operating systems such as Windows 95 to route either DMA channels 1 or 3 to the parallel port for ECP mode. EPP BIOS support must be provided by a device driver or TSR.

## 1.7 ATI-GT 3-D Graphics Controller

The ATI-GT 3-D graphics controller is a highly integrated, 208 pin, VLSI multimedia graphics and video controller that integrates the following features:

- Controller housed in a 208-pin PQFP package.
- The controller implements video acceleration and 3-D rendering.
- The controller supports 3-D rendering with as little as 1MB of SGRAM graphic memory.

- The controller is able to become a PCI bus master.
- The controller supports connection to Plug and Play monitors with both DDC1 (Data Display Channel 1) and DDC2B capability. This allows changing of the monitor resolutions and color options without rebooting the computer.

### 1.7.1 Graphics Upgrade Options

The CU430HX motherboard has several headers that support expansion of the graphic subsystem. The LBP VESA feature connector supports connection to devices such as ATI MPEG and TV products.

Two video memory upgrade connectors support connection to video memory upgrade modules from ATI. These upgrade modules allow upgrading the total video memory from the standard 1MB (or 2MB) of onboard SGRAM, to either 2MB or 4MB of total video memory.

### 1.7.2 Resolutions Supported

Table 2 lists the available video resolutions using the video controller and a standard 1MB of SGRAM video memory. The controller supports 3-D rendering with as little as 1MB of SGRAM graphic memory. The video memory can be upgraded to a maximum of 4MB of video memory using plug-in daughterboards. Refer to the video controller data sheet for the video resolutions available with more than 1MB of video memory.

**Table 2. Supported Video Resolutions**

| Resolution | Supported with 1 MB SGRAM | Refresh Rate (Hz) |
|---|---|---|
| 640 x 480 x 256 colors | Yes | 100 |
| 640 x 480 x 64K colors | Yes | 100 |
| 640 x 480 x 16.7M colors | Yes | 100 |
| 800 x 600 x 256 colors | Yes | 100 |
| 800 x 600 x 64K colors | Yes | 100 |
| 800 x 600 x 16.7M colors | No | 100 |
| 1024 x 768 x 256 colors | Yes | 100 |
| 1024 x 768 x 64K colors | No | 100 |
| 1152 x 864 x 256 colors | Yes | 80 |
| 1152 x 864 x 64K colors | No | 80 |
| 1280 x 1024 x 16 colors | Yes | 75 |
| 1280x 1024 x 256 colors | No | 75 |

### 1.7.3 Graphics Drivers and Utilities

Common graphics drivers and utilities for DOS, Windows 3.1x, Windows 95, and other operating systems, as well as a variety of applications (such as AutoCAD) are available for the CU430HX motherboard. Contact your vendor for a list of available drivers. The Windows 3.1x and Windows 95 drivers include the ATI WinSwitch utility that allows users to change screen resolution without rebooting Windows, and the ATI DeskTop that supports panning and scrolling across a virtual workspace of up to 2048 x 1536.

Drivers for some operating systems such as OS/2† are native to the operating systems. Drivers for SCO† and Interactive UNIX† should be obtained from the respective UNIX vendor. Although Windows 95 installs native drivers for the onboard video, these drivers are not optimized, so you should obtain and install the accelerated drivers available through your vendor.

## 1.8 Audio Subsystem (Creative Labs Vibra 16C)

The CU430HX motherboard optionally features a 16-bit stereo audio subsystem. The audio subsystem is based upon the Creative Labs Vibra 16C (CT2505) multimedia codec. The Vibra 16C provides all the digital audio and analog mixing functions required for recording and playing of audio on personal computers. The Creative Labs Vibra 16C is a single chip VLSI solution which integrates FM synthesis, is Sound Blaster compatible and Roland MPU-401 UART mode compatible. Creative Labs Vibra 16C also provides MPCII, Adlib, and Multimedia PC Level 2 compliance to meet all of the requirements of today's multi-media applications.

The Vibra 16C has been implemented as a Plug and Play motherboard device. This means that there is a device node defined for the Vibra 16C and the BIOS must configure it. Although it is not a Plug and Play device, the Vibra 16C is very flexible in that it accommodates a variety of I/O addresses, DMA channels and interrupts.

The audio subsystem requires up to two DMA channels (to support full duplex operation) and one interrupt. When the Vibra 16C is programmed for full duplex operation, two DMA channels are assigned: one of the channels will be a 16-bit channel and the other will be 8 bits. The system can be configured to use either DMA channels 1 or 3 (8 bit channels) and DMA channels 5 or 7 (16 bit channels). The interrupt can be mapped to IRQ 5, 7, 9, or 10. The base address register is also configurable for a variety of base addresses ranging from I/O address 220 through address 280 (see the resource map below for more details). The ICU (ISA Configuration Utility) must be installed and configured before installing the DOS and Windows audio drivers.

### 1.8.1 Resource Map

Table 3 lists the interrupts, DMA channels, and I/O addresses associated with the audio subsystem of the CU430HX motherboard.

**Table 3. Vibra 16C Resource Map**

| Device | Interrupt (IRQ) | DMA Channel | I/O Address |
|---|---|---|---|
| Creative Labs 16C Base | 2/9 | 8 bit DMA 1 (default) | 220h-233h (default) |
| | 5 (default) | 8 bit DMA 3 | 240h-253h |
| | 7 | 16 bit DMA 5 (default) | 260h-273h |
| | 10 | 16 bit DMA 7 | 280h-293h |
| FM Synthesis | | | 388h-38Bh |
| Joystick (midi-port) | | | 200h-207h |
| MPU-401 | default is disabled | | 300h-301h |
| | | | 330h-331h |

### 1.8.2 Audio Drivers

Audio software and utilities are provided on the foundation software CD for the CU430HX motherboard for DOS, Windows 3.1x, and Windows 95. A setup program installs the appropriate software programs and utilities onto the system hard drive. Included in the audio software are DOS utilities that allow the user to play a CD-ROM, control sound volume and mixer settings, run diagnostics, and switch between Sound Blaster Pro and Windows Sound System modes. Windows drivers and utilities include the Windows sound driver, audio input control panel, audio mixer control panel, and a business audio transport utility.

## 1.9 Management Extension Hardware

The Management Extension hardware option provides low-cost instrumentation capabilities designed to reduce the total cost of PC ownership. The Management Extension hardware incorporates features that support the requirements of the Desktop Management Interface (DMI) compliant areas of the BIOS, as well as those of the LANDesk® Client Manager software. The hardware implementation is a single-chip ASIC with the following features:

- An integrated temperature sensor plus support for an external temperature sensor
- Support for a fan speed sensor
- Power supply voltage monitoring to detect levels above or below acceptable values
- Registers for storing power on self test (POST) hardware test results and error codes
- Intrusion detection support for an onboard photo-transistor and an optional mechanical switch. Allows detection of physical intrusion, such as when the chassis lid has been removed (even when power is off)
- Remote reset capabilities from a remote peer or server through LANDesk Client Manager, Version 3.0 and service layers (when available)
- Hardware compatibility with Windows NT†.

When an out-of-range condition (temperature, fan speed, or voltage) is reached, an interrupt is activated. The Management Extension circuitry connects to the ISA bus as an 8-bit I/O mapped device and uses the I/O addresses identified in the I/O map.

## 1.10 Onboard Networking

### 1.10.1 EtherExpress™ PRO/100B PCI LAN Subsystem

The EtherExpress™ PRO/100B PCI LAN Subsystem is an high performance Ethernet LAN subsystem that provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32 bit direct bus mastering on the PCI bus.
- Shared memory structure in the host memory that copies data directly to/from host memory.
- 10Base-T and 100Base-TX capability using a single RJ-45 connector.
- IEEE 802.3u Auto-Negotiation for hardware selection of highest operating speed.
- Support for boot ROM (Flash or EPROM) up to 256 KB.
- Jumperless configuration; the LAN subsystem is totally software configurable.

### 1.10.2 Intel 82557 LAN Controller

This device is the heart of the LAN subsystem and provides the following functions:

- CSMA/CD Protocol Engine
- Compatible with the PCI Bus Interface 2.1
- DMA engine for movement of commands, status, and network data across PCI
- Access to EEPROM
- Standard MII interface for access to IEEE 802.3u compliant physical layer devices

### 1.10.3 10/100Mbps Physical Layer Interface

The physical layer interface is implemented in two devices from National Semiconductor, the DP83840 and the DP83223 (a.k.a. the "Twister"). The DP83840 provides:

- Complete functionality necessary for the 10Base-T interface; directly drives the cable when in 10Mbps mode.
- All functionality required for the 100Base-TX interface except for the NRZ to MLT3 encoding/decoding function, which is provided by the DP83223 "Twister" device.
- Complete set of MII management registers for control and status reporting.
- 802.3u Auto-Negotiation for automatically establishing the best possible operating mode when connected to other 10Base-T or 100Base-TX devices, whether half or full-duplex capable.

### 1.10.4 EtherExpress PRO/100B PCI LAN Subsystem Software Description

The software provided with the EtherExpress PRO/100B PCI LAN subsystem includes setup/diagnostic software (SETUP.EXE) and a readme file viewer (README.EXE) that lists supported drivers.

## 1.11 Motherboard Connectors

Figure 3 shows the location and functions of the motherboard connectors and headers.

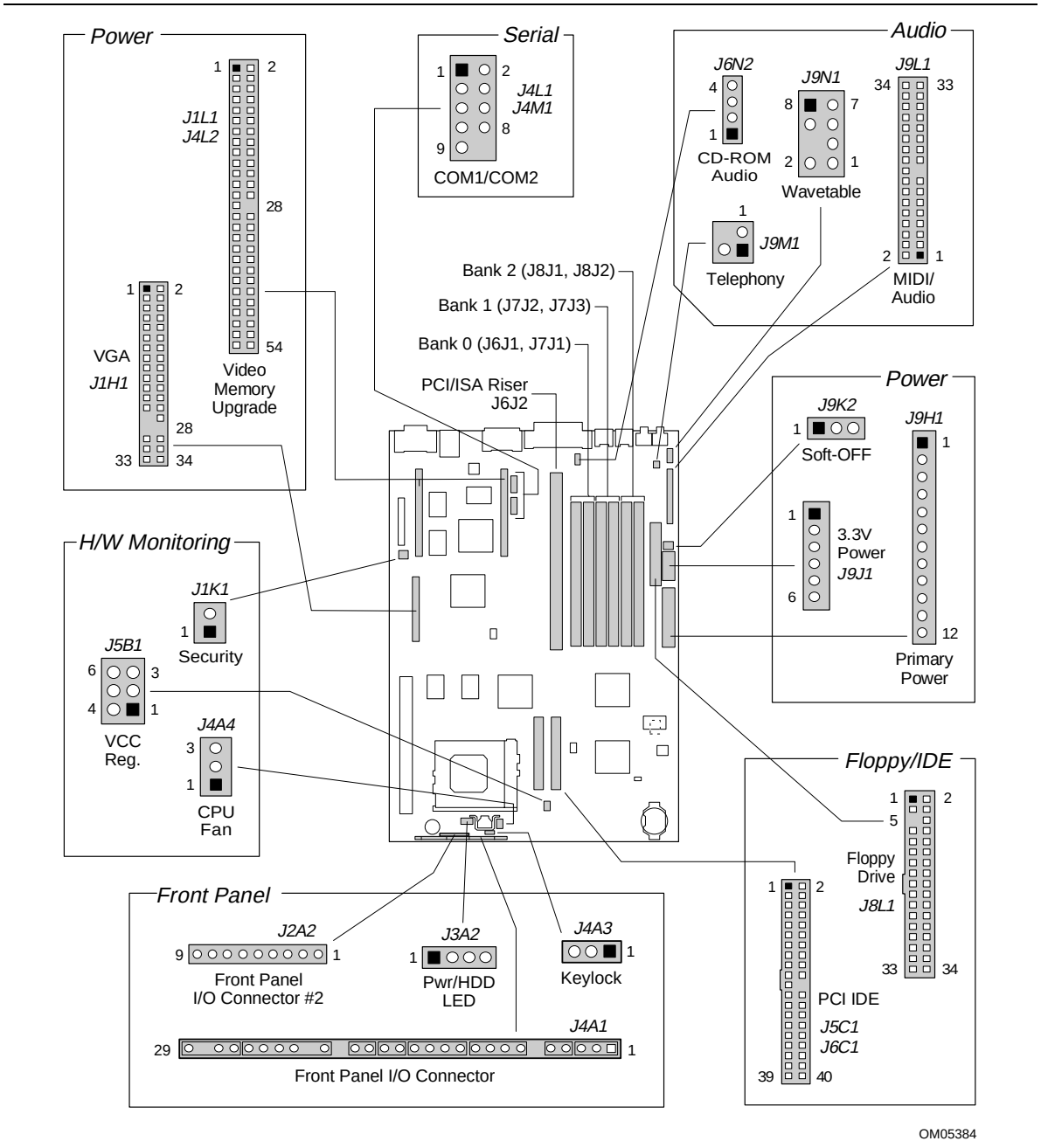


**Figure 3. Motherboard Connector Locations**

### 1.11.1 Front Panel Connectors

The motherboard provides header connectors to support functions typically located on the chassis bezel. Figure 4 shows the front panel connector header. Front panel features supported include:

- CPU fan (FAN)
- System Reset (RST)
- Power LED (PWRLED)
- Hard drive activity LED (HDDLED)
- Power supply ON (PS-ON)
- Sleep/Resume (SLP)
- Infrared (IrDA) port (IR)
- System Speaker (SPKR)

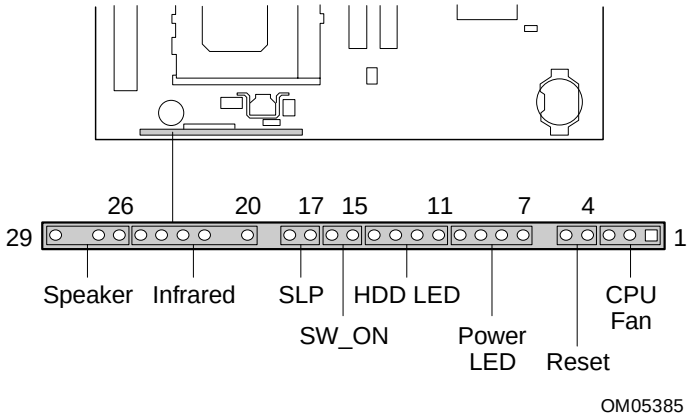


**Figure 4. Front Panel I/O Connectors**

Table 4 lists the pinouts and signals for the front panel I/O connector.

**Table 4. Front Panel I/O Connector (J2A1)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | FANNEG | 16 | Ground |
| 2 | FANPOS | 17 | SLEEP |
| 3 | FANNEG | 18 | SLEEPPU |
| 4 | Ground | 19 | No connection |
| 5 | SW_RST | 20 | VCC |
| 6 | No connection | 21 | No connection |
| 7 | PWR_PU | 22 | IRRIN |
| 8 | PWR_PU | 23 | Ground |
| 9 | PWR_LED_DRV | 24 | IRTX |
| 10 | PWR_LED_DRV | 25 | CONIR |
| 11 | HDD_PU | 26 | SPKR+ |
| 12 | HDA# | 27 | SPKRHDR |
| 13 | PWR_LED_DRV | 28 | No connection |
| 14 | PWR_PU | 29 | Ground |
| 15 | SW_ON | | |

#### 1.11.1.1 CPU Fan (FAN)

The 3-pin fan header of the front panel connector provides a basic 3-wire connection to a CPU fan. The center pin of the header supplies +12 VDC and the outer pins are at ground.

#### 1.11.1.2 System Reset (RST)

This 2-pin header can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the system will hard reset and run POST.

#### 1.11.1.3 Power LED (PWRLED)

This 4-pin header drives an LED to indicate when power is applied to the motherboard.

#### 1.11.1.4 Hard Drive Activity LED (HDDLED)

This 4-pin header drives an LED to indicate when hard drive activity is taking place.

### 1.11.1.5 Power Supply ON (PS-ON)

This 2-pin header connects to a front panel power switch. When the switch is closed, the power supply turns ON. If a mechanical switch is connected to this header, it must apply a momentary ground to the SW_ON header pin in order to signal the supply to turn ON or OFF. Because of the motherboard's internal debounce circuitry, the ground must be applied for at least 50ms. At least 2 seconds must pass before the power supply will recognize another ON/OFF signal (to prevent "double clicking").

### 1.11.1.6 Sleep/Resume (SLP)

When Advanced Power Management (APM) is activated in the system BIOS and the Operating System's APM driver is loaded, Sleep mode (Stand-By) can be entered in one of three ways: an optional front panel "Sleep/Resume" button, a user defined keyboard hot key, or prolonged system inactivity. The Sleep/Resume button is supported by a 2-pin header located on the front panel I/O connector. Closing the "Sleep" switch will generate an SMI (System Management Interrupt) to the processor which immediately goes into System Management Mode (SMM), the so called "Sleep" mode.

The front panel "Sleep mode" switch must be a momentary two pin SPST type that is normally open. The function of the Sleep/Resume button can also be achieved via a keyboard hot-key sequence, or by a time-out of the system inactivity timer. Both the keyboard hot-key and the inactivity timer are programmable in the BIOS setup (timer is set to 10 minutes by default). To re-activate the system, or "Resume", the user must simply press the sleep/resume button again, or use the keyboard or mouse. Mouse activity will only "wake up" the system if a mouse driver is loaded. While the system is in Stand-By or "sleep" mode it is fully capable of responding to and servicing external interrupts (such as in-coming FAX) even though the monitor will only turn on if a user interrupt (keyboard/mouse) occurs as mentioned above

### 1.11.1.7 Infrared (IrDA†) Connector (IR)

Serial port 2 can be configured to support an IrDA module via a 6-pin header connector . Once configured for IrDA, the user can transfer files to or from portable devices such as laptops, PDA's and printers using application software such as LapLink. The IrDA specification provides for data transfers at 115 Kbps from a distance of 1 meter.

### 1.11.1.8 Speaker (SPKR)

The CU430HX motherboard has an onboard speaker to provide basic level beep code information. The front panel speaker connection allows an external (chassis mounted) speaker to be connected. The external or the onboard speaker provides error beep code information during the Power-On Self Test, if the system cannot use the video interface. When an external (chassis mounted) speaker is connected to the 2-pin header on the front panel connector, the onboard speaker is disabled.

### 1.11.1.9 Other Front Panel Connectors

In addition to the front panel I/O connector, there are three other headers included in the front panel group. Two headers (front panel header #2 and pwr/HDD LED header) provide duplicate signals to those available on the front panel I/O connector. The following tables list the pinouts and signals on the remaining front panel connectors.

**Table 5. Power/HDD LED Header (J3A2)**

| Pin | Signal Name |
|---|---|
| 1 | HDD_PU |
| 2 | HDA# |
| 3 | PWR_LED_DRV |
| 4 | PWR_PU |

**Table 6. Front Panel Header #2 (J2A2)**

| Pin | Signal Name |
|---|---|
| 1 | HDD_PU |
| 2 | HDA# |
| 3 | Ground |
| 4 | SW_RST |
| 5 | VCC |
| 6 | IRRIN |
| 7 | Ground |
| 8 | IRTX |
| 9 | No connection |

**Table 7. Keylock Header (J4A3)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | KBLOCK# |
| 3 | Ground |

## 1.11.2 Memory/Expansion Connectors

The CU430HX motherboard provides six 72-pin SIMM sockets for main memory. These sockets accept standard SIMM 72-pin modules, as long as they satisfy the requirements described in the "Main System Memory" section of this specification, starting on page 11.

The CU430HX motherboard uses a PCI/ISA riser connector (J6J2) to provide for expansion PCI or ISA boards. The associated riser board can support either two or three PCI slots. A pair of jumpers on the CU430HX motherboard must be set to define the number of PCI slots on the riser board. Refer to Figure 6 on page 37 for jumper block details. Table 8 contains the pinout listing for the PCI/ISA riser connector.

**Table 8. PCI/ISA Riser Connector (J6J2)**

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| A1 | IOCHK# | B1 | GND | E1 | GND | F1 | GND |
| A2 | SD7 | B2 | RSTDRV | E2 | GND | F2 | GND |
| A3 | SD6 | B3 | Vcc | E3 | PCIINT1# | F3 | PCIINT3# |
| A4 | SD5 | B4 | IRQ9 | E4 | PCIIINT2# | F4 | PCIINT4# |
| A5 | SD4 | B5 | -5 V | E5 | Vcc | F5 | Vcc |
| A6 | SD3 | B6 | DRQ2 | E6 | Key | F6 | Key |
| A7 | SD2 | B7 | -12 V | E7 | Vcc | F7 | Vcc |
| A8 | SD1 | B8 | 0WS# | E8 | PCIRST# | F8 | PCKLF |
| A9 | SD0 | B9 | +12 V | E9 | GNT0# | F9 | GND |
| A10 | IOCHRDY | B10 | GND | E10 | REQ0# | F10 | GNT1# |
| A11 | AEN | B11 | SMEMW# | E11 | GND | F11 | GND |
| A12 | SA19 | B12 | SMEMR# | E12 | PCKLE | F12 | REQ1# |
| A13 | SA18 | B13 | IOW# | E13 | GND | F13 | AD31 |
| A14 | SA17 | B14 | IOR# | E14 | AD30 | F14 | AD29 |
| A15 | SA16 | B15 | DACK3# | E15 | 3.3 V | F15 | 3.3 V |
| A16 | SA15 | B16 | DRQ3 | E16 | Key | F16 | Key |
| A17 | SA14 | B17 | DACK1# | E17 | 3.3 V | F17 | 3.3 V |
| A18 | SA13 | B18 | DRQ1 | E18 | AD28 | F18 | AD27 |
| A19 | SA12 | B19 | REFRESH# | E19 | AD26 | F19 | AD25 |
| A20 | SA11 | B20 | SYSCLK | E20 | AD24 | F20 | CBE3# |
| A21 | SA10 | B21 | IRQ7 | E21 | AD22 | F21 | AD23 |
| A22 | SA9 | B22 | IRQ6 | E22 | AD20 | F22 | AD21 |
| A23 | SA8 | B23 | IRQ5 | E23 | AD18 | F23 | AD19 |
| A24 | SA7 | B24 | IRQ4 | E24 | 3.3 V | F24 | 3.3 V |
| A25 | SA6 | B25 | IRQ3 | E25 | Key | F25 | Key |
| A26 | SA5 | B26 | DACK2# | E26 | 3.3 V | F26 | 3.3 V |
| A27 | SA4 | B27 | TC | E27 | AD16 | F27 | AD17 |
| A28 | SA3 | B28 | BALE | E28 | FRAME# | F28 | IRDY# |
| A29 | SA2 | B29 | Vcc | E29 | CBE2# | F29 | DEVSEL# |
| A30 | SA1 | B30 | OSC | E30 | TRDY# | F30 | PLOCK# |
| A31 | SA0 | B31 | GND | E31 | STOP# | F31 | PERR# |
| C1 | SBHE# | D1 | MEMCS16# | G1 | SDONE | H1 | SERR# |
| C2 | LA23 | D2 | IOCS16# | G2 | SBO# | H2 | AD15 |
| C3 | LA22 | D3 | IRQ10 | G3 | CBE1# | H3 | AD14 |
| C4 | LA21 | D4 | IRQ11 | G4 | PAR | H4 | AD12 |
| C5 | LA20 | D5 | IRQ12 | G5 | GND | H5 | GND |
| C6 | LA19 | D6 | IRQ15 | G6 | Key | H6 | Key |

continued ☛

**Table 8. PCI/ISA Riser Connector (J6J2) (continued)**

| Pin | Signal Name | Pin | Signal Name | Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|---|---|---|---|
| C7 | LA18 | D7 | IRQ14 | G7 | GND | H7 | GND |
| C8 | LA17 | D8 | DACK0# | G8 | AD13 | H8 | AD10 |
| C9 | MEMR# | D9 | DRQ0 | G9 | AD11 | H9 | AD8 |
| C10 | MEMW# | D10 | DACK5# | G10 | AD9 | H10 | AD7 |
| C11 | SD8 | D11 | DRQ5 | G11 | CBE0# | H11 | AD5 |
| C12 | SD9 | D12 | DACK6# | G12 | AD6 | H12 | AD3 |
| C13 | SD10 | D13 | DRQ6 | G13 | AD4 | H13 | AD1 |
| C14 | SD11 | D14 | DACK7# | G14 | AD2 | H14 | AD0 |
| C15 | SD12 | D15 | DRQ7 | G15 | Key | H15 | Key |
| C16 | SD13 | D16 | Vcc | G16 | Vcc | H16 | Vcc |
| C17 | SD14 | D17 | MASTER# | G17 | GNT2 | H17 | Vcc |
| C18 | SD15 | D18 | GND | G18 | (GND \| REQ2) * | H18 | (GND \| PCCLK2) * |
| | | | | G19 | GND | H19 | GND |

* These signals are (2 slot | 3 slot) jumpered signal names.

## 1.11.3 Audio Connectors

The pinouts and signal listings for the audio headers/connectors are provided in the following tables.

**Table 9. CD-Audio Header (J6N2)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | CD-Left |
| 3 | Ground |
| 4 | CD-Right |

**Table 10. Wavetable Header (J9N1)**

| Pin | Signal Name |
|---|---|
| 1 | Wave Right |
| 2 | Ground |
| 3 | Wave Left |
| 4 | Ground |
| 5 | Key |
| 6 | Ground |
| 7 | NC |
| 8 | MIDI_Out |

**Table 11. Telephony Header (J9M1)**

| Pin | Signal Name |
|---|---|
| 1 | Ground |
| 2 | Mono Out |
| 3 | Mic In |
| 4 | Key |

**Table 12. MIDI/Audio Upgrade Header (J9L1)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | +5 V | 2 | +5 V |
| 3 | Joystick Button0 | 4 | Joystick Button2 |
| 5 | Joystick X1 | 6 | Joystick X2 |
| 7 | Ground | 8 | MIDI Out |
| 9 | Ground | 10 | Joystick Y2 |
| 11 | Joystick Y1 | 12 | Joystick Button3 |
| 13 | Joystick Button1 | 14 | MIDI In |
| 15 | +5 V | 16 | Key |
| 17 | Key | 18 | Key |
| 19 | Line Out Right | 20 | Ground |
| 21 | Right Speaker | 22 | Ground |
| 23 | Left Speaker | 24 | Key |
| 25 | Line Out Left | 26 | Ground |
| 27 | Line In Right | 28 | -12 V |
| 29 | Line In Left | 30 | Ground |
| 31 | Mic In | 32 | +12 V |
| 33 | Ground | 34 | Ground |

### 1.11.4 Power Connectors

The CU430HX motherboard must be used with a power supply that supports remote power on/off, so the motherboard can turn off the system power under software control. The Powerman utility supplied for Windows 3.1x allows for soft-off as does the shutdown icon in Windows 95 Start menu. The system BIOS turns the system power off when it receives the proper APM command from the OS. For example, Windows 95 issues this APM command after the user selects "Shutdown the computer" option. APM must be enabled in the system BIOS and OS in order for the soft-off feature to work correctly. The user has the ability to determine the state of the power supply, so if the system was turned on when power was disconnected, the system turns back on when power is reapplied or it remains off, depending on the user setup configuration in CMOS.

Table 13 provides the pinout listing for the primary power supply connector of the CU430HX motherboard.

**Table 13. Primary Power Supply Connector (J9H1)**

| Pin | Signal Name/Function |
|---|---|
| 1 | PWRGD (Power good) |
| 2 | +5 V (VCC) |
| 3 | +12 V |
| 4, key | -12 V |
| 5 | Ground |
| 6 | Ground |
| 7, key | Ground |
| 8 | Ground |
| 9 | -5 V |
| 10 | +5 V (VCC) |
| 11 | +5 V (VCC) |
| 12 | +5 V (VCC) |

Table 14 provides the pinout listing for the external 3.3 volt power supply connector of the CU430HX motherboard.

**Table 14. External 3.3 V Power Supply Connector (J9J1)**

| Pin | Name |
|---|---|
| 1 | Ground |
| 2, key | Ground |
| 3 | Ground |
| 4 | +3.3 V |
| 5 | +3.3 V |
| 6 | +3.3 V |

The pinout listing for the soft-OFF power supply connector of the CU430HX motherboard is shown in Table 15. This 3-pin keyed position supports a software-controlled power supply shutoff (Soft-OFF). When connected to this position, the power supply follows remote ON/OFF commands.

**Table 15. Soft-Off Power Supply Connector (J9K2)**

| Pin | Signal Name/Function |
|---|---|
| 1 | +5 VSB (+5 Volts Standby) |
| 2 | PS_ON (Remote On/Off) |
| 3 | PS_COM (Supply presence) |

### 1.11.5 Floppy/IDE Connectors

Table 16 lists the pinout and signal names for the floppy drive connector.

**Table 16. Floppy Drive Connector (J9K1)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Ground | 2 | DENSEL |
| 3 | Ground | 4 | Reserved |
| 5 | Key | 6 | FDEDIN |
| 7 | Ground | 8 | Index# |
| 9 | Ground | 10 | Motor Enable A# |
| 11 | Ground | 12 | Drive Select B# |
| 13 | Ground | 14 | Drive Select A# |
| 15 | Ground | 16 | Motor Enable B# |
| 17 | MSEN1 | 18 | DIR# |
| 19 | Ground | 20 | STEP# |
| 21 | Ground | 22 | Write Data# |
| 23 | Ground | 24 | Write Gate# |
| 25 | Ground | 26 | Track 00# |
| 27 | MSEN0 | 28 | Write Protect# |
| 29 | Ground | 30 | Read Data# |
| 31 | Ground | 32 | Side 1 Select# |
| 33 | Ground | 34 | Diskette Change# |

Table 17 lists the pinout and signal names for the IDE connectors.

**Table 17. IDE Connectors (J5C1, J6C1)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 1 | Reset IDE | 2 | Ground |
| 3 | Host Data 7 | 4 | Host Data 8 |
| 5 | Host Data 6 | 6 | Host Data 9 |
| 7 | Host Data 5 | 8 | Host Data 10 |
| 9 | Host Data 4 | 10 | Host Data 11 |
| 11 | Host Data 3 | 12 | Host Data 12 |
| 13 | Host Data 2 | 14 | Host Data 13 |
| 15 | Host Data 1 | 16 | Host Data 14 |
| 17 | Host Data 0 | 18 | Host Data 15 |
| 19 | Ground | 20 | Key |
| 21 | DDRQ0 (DDRQ1) | 22 | Ground |
| 23 | I/O Write# | 24 | Ground |
| 25 | I/O Read# | 26 | Ground |

continued ☛

**Table 17. IDE Connectors (J5C1, J6C1) (continued)**

| Pin | Signal Name | Pin | Signal Name |
|---|---|---|---|
| 27 | IOCHRDY | 28 | Vcc pull-down |
| 29 | DDACK0 (DDACK1)# | 30 | Ground |
| 31 | IRQ14 (IRQ15) | 32 | Reserved |
| 33 | DAG1 | 34 | Reserved |
| 35 | DAG0 | 36 | DAG2 |
| 37 | Chip Select 1P (1S)# | 38 | Chip Select 3P (3S)# |
| 39 | Activity# | 40 | Ground |

## 1.11.6 Hardware Monitoring Connectors

The hardware monitoring connectors identified in Figure 3 are all associated with the functions performed by the hardware monitoring ASIC component on the CU430HX motherboard. The following tables list the pinouts and signals of the hardware monitoring connectors.

The security connector can be connected to a chassis-mounted micro-switch that closes if the chassis cover is removed. This switch can be used in addition to the onboard photo-transistor to keep track of each time the system chassis is opened.

**Table 18. Security Connector (J1K1)**

| Pin | Signal Name/Function |
|---|---|
| 1 | Ground |
| 2 | BATPWRSLP (Battery voltage) |

**Table 19. Vcc Regulator Header (J5B1)**

| Pin | Signal Name/Function |
|---|---|
| 1 | VCC3 (Output of U3A1 regulator) |
| 2 | VCC3 (Output of U3A1 regulator) |
| 3 | VCC3 (Output of U3A1 regulator) |
| 4 | VCC2 |
| 5 | VCC2 |
| 6 | VCC2 |

The separate fan connector (not part of the front panel I/O connector) listed in Table 20 has a fan sense (tachometer) line so the hardware monitoring ASIC can monitor the fan speed. This connector is keyed to prevent potential fan damage.

**Table 20. CPU Fan Connector (J4A4)**

| Pin | Signal Name/Function |
|---|---|
| 1 | Ground |
| 2 | FANPOS (+12VDC) |
| 3 | FAN1_SENSE (Tachometer signal) |

## 1.11.7 Video Connectors

The video features identified in Figure 3 are the LBP VESA connector and the video memory upgrade headers. A video memory daughtercard can be added using the video memory upgrade headers. The total installed onboard video memory can be 1MB or 2MB. With an installed video memory daughtercard, the total video memory can be either 2MB or 4MB.

Table 21 provides the pinout and signal listing for the LBP VESA feature connector.

**Table 21. LBP VESA Feature Connector (J1H1)**

| Pin | Signal Name / Function | Pin | Signal Name / Function |
|---|---|---|---|
| 1 | Ground | 2 | Pixel Data 0 |
| 3 | Ground | 4 | Pixel Data 1 |
| 5 | Ground | 6 | Pixel Data 2 |
| 7 | Enable External Pixel Data | 8 | Pixel Data 3 |
| 9 | Enable External Sync | 10 | Pixel Data 4 |
| 11 | Enable External Pixel Clock | 12 | Pixel Data 5 |
| 13 | N/C, not used | 14 | Pixel Data 6 |
| 15 | Ground | 16 | Pixel Data 7 |
| 17 | Ground | 18 | PCLK, Pixel Clock |
| 19 | Ground | 20 | BLANKING |
| 21 | Ground | 22 | HSYNC, Horizontal Sync |
| 23 | N/C, not used | 24 | VSYNC, Vertical Sync |
| 25 | Key (no pin) | 26 | Ground |
| 27 | Key (no pin) | 28 | Key (no pin) |
| 29 | IICCLK | 30 | Ground |
| 31 | IICDAT | 32 | N/C |
| 33 | EN1 | 34 | EN2 |

Table 22 and Table 23 provide the pinout and signal listings for the video memory upgrade headers.

**Table 22. Video Memory Upgrade Header #1 (J4L2)**

| Pin | Signal Name / Function | Pin | Signal Name / Function | Pin | Signal Name / Function |
|---|---|---|---|---|---|
| 1 | MCLK | 19 | VMD2 | 37 | VMD41 |
| 2 | Ground | 20 | VMD1 | 38 | VMD42 |
| 3 | VCC3 | 21 | VMD0 | 39 | VMD43 |
| 4 | VWEVTR# | 22 | Ground | 40 | VMD44 |
| 5 | VMD8 | 23 | VCC3 | 41 | VMD45 |
| 6 | VMD9 | 24 | VCAS0R# | 42 | Ground |
| 7 | VMD10 | 25 | VCAS1R# | 43 | VMD46 |
| 8 | VMD11 | 26 | VCAS2R# | 44 | VMD47 |
| 9 | VMD12 | 27 | VCAS3R# | 45 | VMD39 |
| 10 | VMD13 | 28 | Vacant, Key | 46 | VMD38 |
| 11 | VMD14 | 29 | VCAS4R# | 47 | VMD37 |
| 12 | Ground | 30 | VCAS5R# | 48 | VMD36 |
| 13 | VMD15 | 31 | VCAS6R# | 49 | VMD35 |
| 14 | VMD7 | 32 | Ground | 50 | VMD34 |
| 15 | VMD6 | 33 | VCAS7R# | 51 | VMD33 |
| 16 | VMD5 | 34 | VWE_CAS0R# | 52 | Ground |
| 17 | VMD4 | 35 | VWE_CAS1R# | 53 | VCC3 |
| 18 | VMD3 | 36 | VMD40 | 54 | VMD32 |

**Table 23. Video Memory Upgrade Header #2 (J1L1)**

| Pin | Signal Name / Function | Pin | Signal Name / Function | Pin | Signal Name / Function |
|---|---|---|---|---|---|
| 1 | Ground | 19 | VMD31 | 37 | VMD49 |
| 2 | VMD16 | 20 | VRAS0R# | 38 | VMD50 |
| 3 | VMD17 | 21 | Ground | 39 | VMD51 |
| 4 | VCC3 | 22 | VRAS1R# | 40 | VMD52 |
| 5 | VMD18 | 23 | VMAR0 | 41 | Ground |
| 6 | VMD19 | 24 | VMAR1 | 42 | VMD53 |
| 7 | VMD20 | 25 | VMAR2 | 43 | VMD54 |
| 8 | VMD21 | 26 | VMAR3 | 44 | VMD55 |
| 9 | VMD22 | 27 | VMAR4 | 45 | VMD56 |
| 10 | VMD23 | 28 | Vacant, Key | 46 | VMD57 |
| 11 | Ground | 29 | VMAR5 | 47 | VMD58 |
| 12 | VMD24 | 30 | VCC3 | 48 | VMD59 |
| 13 | VMD25 | 31 | Ground | 49 | VMD60 |
| 14 | VMD26 | 32 | VMAR6 | 50 | VMD61 |
| 15 | VMD27 | 33 | VMAR7 | 51 | DSF |
| 16 | VMD28 | 34 | VMAR8 | 52 | VMD62 |
| 17 | VMD29 | 35 | VMAR9 | 53 | VMD63 |
| 18 | VMD30 | 36 | VMD48 | 54 | VCC3 |

## 1.11.8 USB/Serial Connectors

One of the manufacturing options for the CU430HX motherboard allows substitution of a side-by-side USB connector in place of the serial connector on the back panel. When the USB option is implemented, connection to the serial ports must be made using the COM1/COM2 headers (J4L1, J4M1) on the motherboard. Table 24 lists the signals and pinout for the COM1/COM2 headers, and Table 25 lists the signals and pinout for the side-by-side USB connector.

**Table 24. Serial Port Headers (J4L1, J4M1)**

| Pin | Signal Name | Description |
|---|---|---|
| 1 | DCD | Carrier Detect |
| 2 | DSR | Data Set Ready |
| 3 | SIN# | Serial Data In |
| 4 | RTS | Request To Send |
| 5 | SOUT# | Serial Data Out |
| 6 | CTS | Clear To Send |
| 7 | DTR | Data Terminal Ready |
| 8 | RI | Ring Indicator |
| 9 | GND | Chassis Ground |
| 10 | Key | Vacant |

**Table 25. USB Port Connector (J4N1) Pinout**

| Pin | Signal Name |
|---|---|
| 1 | Power |
| 2 | USBP0# |
| 3 | USBP0 |
| 4 | Ground |
| 5 | Power |
| 6 | USBP1# |
| 7 | USBP1 |
| 8 | Ground |

## 1.11.9 Back Panel Connectors

The back panel provides external access to two PS/2 style keyboard and mouse connectors, one parallel port, the microphone input and audio output connectors, an RS45 LAN connector, and a VGA video connector which are integrated on the motherboard. In addition, an RS232 serial connector or a side-by-side pair of USB connectors are also integrated on the motherboard. Figure 5 shows the general location of the I/O connectors.

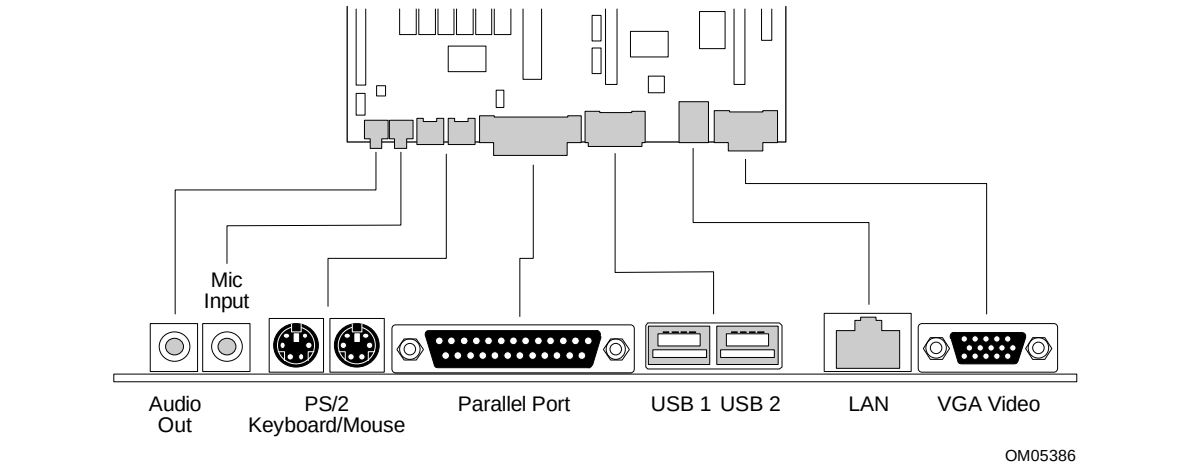


**Figure 5. I/O Connections**

### 1.11.9.1 VGA Video Connector

Table 26 lists the pinout and signal names for the VGA video connector.

**Table 26. VGA Video Connector (J1N1)**

| Pin | Signal Name / Function | Pin | Signal Name / Function |
|---|---|---|---|
| 1 | Red Video | 9 | Key (no pin) |
| 2 | Green Video | 10 | Sync Return (Ground) |
| 3 | Blue Video | 11 | Monitor ID Bit 0 (not used) |
| 4 | Monitor ID Bit 2 (not used) | 12 | Monitor ID Bit 1 (not used) |
| 5 | Chassis Ground | 13 | Horizontal Sync |
| 6 | Red Return (Ground) | 14 | Vertical Sync |
| 7 | Green Return (Ground) | 15 | Not used |
| 8 | Blue Return (Ground) | Shield | Chassis Ground |

### 1.11.9.2 LAN Connector

Table 27 lists the pinout and signal names for the RJ45 LAN connector.

**Table 27. LAN Connector (J2N1)**

| Pin | Signal Name |
|---|---|
| 1 | RJ45_TOP |
| 2 | RJ45_TXM |
| 3 | RJ45_RXP |
| 4 | BS_TERM |
| 5 | BS_TERM |
| 6 | RJ45_RXM |
| 7 | BS_TERM |
| 8 | BS_TERM |

### 1.11.9.3 Serial Port Back Panel Connector

Table 28 lists the pinout and signal names for the optional serial connector.

**Table 28. Serial Port Connector Pinout**

| Pin | Signal Name | Description |
|---|---|---|
| 1 | DCD | Carrier Detect |
| 2 | SIN# | Serial Data In |
| 3 | SOUT# | Serial Data Out |
| 4 | DTR | Data Terminal Ready |
| 5 | GND | Chassis Ground |
| 6 | DSR | Data Set Ready |
| 7 | RTS | Request To Send |
| 8 | CTS | Clear To Send |
| 9 | RI | Ring Indicator |

### 1.11.9.4 USB Back Panel Connectors

Table 29 lists the pinout and signal names for the USB back panel connectors.

**Table 29. USB Connector Pinout**

| Pin | Signal Name |
|---|---|
| 1 | Power |
| 2 | USBP0# [USBP1#] |
| 3 | USBP0 [USBP1] |
| 4 | Ground |

### 1.11.9.5 Keyboard and Mouse Ports

Table 30 lists the pinout and signal names for the PS/2 keyboard and mouse connectors. Although they are labeled as "Keyboard" and "Mouse" on the motherboard and the back panel, the connectors can be used interchangeably for either keyboard or mouse.

**Table 30. PS/2 Keyboard/Mouse Connector Pinout**

| Pin | Signal Name / Function |
|---|---|
| 1 | KBD/Mouse Data |
| 2 | Reserved, No connection |
| 3 | GND, Chassis Ground |
| 4 | +5 VDC (fused) |
| 5 | KBD Clock |
| 6 | Reserved, No connection |
| Shield | Chassis Ground |

### 1.11.9.6 Parallel Port

Table 31 lists the pinout and signal names for the parallel port connector.

**Table 31. Parallel Port Connector Pinout**

| Pin | Signal Name | Description | Pin | Signal Name | Description |
|---|---|---|---|---|---|
| 1 | STB# | Strobe | 14 | AFD# | Auto Feed |
| 2 | PPD0 | Data Bit 0 | 15 | ERROR# | Fault |
| 3 | PPD1 | Data Bit 1 | 16 | INIT# | Initializing printer |
| 4 | PPD2 | Data Bit 2 | 17 | SLCTIN# | Select input |
| 5 | PPD3 | Data Bit 3 | 18 | GND | Chassis Ground |
| 6 | PPD4 | Data Bit 4 | 19 | GND | Chassis Ground |
| 7 | PPD5 | Data Bit 5 | 20 | GND | Chassis Ground |
| 8 | PPD6 | Data Bit 6 | 21 | GND | Chassis Ground |
| 9 | PPD7 | Data Bit 7 | 22 | GND | Chassis Ground |
| 10 | ACK# | Acknowledge | 23 | GND | Chassis Ground |
| 11 | BUSY | Port Busy | 24 | GND | Chassis Ground |
| 12 | PE | Paper end | 25 | GND | Chassis Ground |
| 13 | SLCT | Select | | | |

## 1.12 Jumper Settings

There are three jumper blocks on the CU430HX motherboard. The jumper block at J4G1 defines the number of PCI slots (two or three slots) available on the riser board used with the motherboard. The jumper block at J6C2 sets the Flash memory to either normal or recovery mode of operation. The jumper block at J5B1 is only used to provide power for Pentium processors with MMX technology. The jumper block at J1K2 defines a range of microprocessor and motherboard configuration parameters. Figure 8 shows the jumper block locations on the motherboard, and indicates how jumper placement corresponds to the value defined by the motherboard silk-screening.

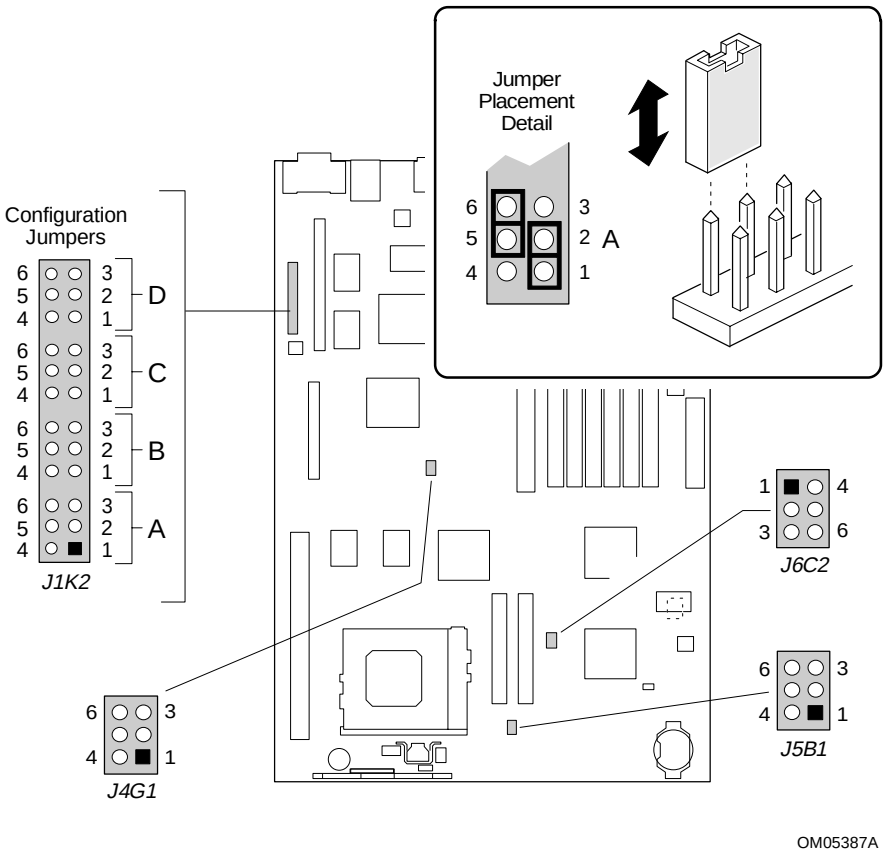


**Figure 6. Jumper Locations**

The jumpers on the CU430HX motherboard perform the following functions:

- Allow the motherboard to be switched between the different frequencies of the Pentium processor. Selecting a processor speed (and multiplier) also changes the Host Bus, PCI Bus, and ISA Bus frequencies.
- Changes output of the onboard voltage regulator and changes power routing to support different processor types.
- Controls clearing or normal operation of the password and CMOS.
- Enables or disables the motherboard setup.

- Determines whether a riser board with two or three PCI slots is being used with the motherboard.
- Determines whether the Flash memory is in a normal or recovery mode of operation.

Table 32 lists the CU430HX motherboard jumper functions and their settings.

**Table 32. Configuration Jumper Settings**

| Function | Jumper | Position | Configuration |
|---|---|---|---|
| Flash Operation | J6C2 | 1-2 | ***NORM*** - Normal mode of operation **(Default)** |
| | | 2-3 | ***RCVR*** - Recovery mode of operation |
| VRE Selection | J6C2 | 4-5 | ***VR*** - Normal mode of operation **(Default)** |
| | | 5-6 | ***VRE*** - VRE operation |
| VCC2 Connection | J5B1 | Vacant | Normal operation (VCC2 not connected) |
| | | 1-4, 2-5, 3-6 | VCC2 connected (support for Pentium® processors using MMX™ technology) |
| 2/3 PCI Slot (***RISER***) | J4G1 | 1-2, 4-5 | ***2 SLOTS*** - Two PCI slots in the riser card. **(Default)** |
| | | 2-3, 5-6 | ***3 SLOTS*** - Three PCI slots in the riser card. |
| Password (***PSWD***) | J1K2(A) | 1-2 | ***KEEP*** - Maintain the current (or Setup-revised) password. **(Default)** |
| | | 2-3 | ***CLR*** - Clear the password. |
| CMOS (***CMOS***) | J1K2(A) | 4-5 | ***KEEP*** - Maintain the current (or Setup-revised) CMOS contents. **(Default)** |
| | | 5-6 | ***CLR*** - Clear the CMOS. |
| Setup (***SETUP***) | J1K2(B) | 1-2 | ***ENBL*** - Enable setup accessibility. **(Default)** |
| | | 2-3 | ***DIS*** - Disable setup accessibility. |
| Reserved function (***RSVD***) | J1K2(B) | 4-5 | ***ENBL*** - Reserved |
| | | 5-6 | ***DIS*** - Reserved **(Default)** |
| Host Bus Frequency (***FREQ***) | J1K2(C) | 2-3, 5-6 | ***50 MHZ*** - Host bus 50 MHz, PCI bus 25 MHz, ISA Bus 6.25 MHz |
| | | 2-3, 4-5 | ***60 MHZ*** - Host bus 60 MHz, PCI bus 30 MHz, ISA Bus 7.5 MHz |
| | | 1-2, 5-6 | ***66 MHZ*** - Host bus 66 MHz, PCI bus 33 MHz, ISA Bus 8.33 MHz **(Default)** |
| | | 1-2, 4-5 | ***RSVD*** - Reserved |
| Microprocessor Clock Multiplier (***MULT***) | J1K2(D) | 1-2, 4-5 | ***1.5*** - Microprocessor clock is 1.5 times the Host Bus frequency. |
| | | 2-3, 4-5 | ***2.0***- Microprocessor clock is 2 times the Host Bus frequency. |
| | | 2-3, 5-6 | ***2.5*** - Microprocessor clock is 2.5 times the Host Bus frequency. **(Default)** |
| | | 1-2, 5-6 | ***3.0*** - Microprocessor clock is 3 times the Host Bus frequency. |

**Notes:** The text appearing in a ***BOLD-ITALIC*** font duplicates the text of the motherboard silk-screening.

## 1.13 Reliability

The Mean-Time-Between-Failures (MTBF) data is calculated from predicted data at 55°C.

| | |
|---|---|
| Motherboard | 63932 Hours |

## 1.14 Environmental

**Table 33. Motherboard Environmental Specifications**

| Parameter | Specification |
|---|---|
| **Temperature** | |
| Non-Operating | -40°C to +70°C |
| Operating | +0°C to +55°C |
| **DC Voltage** | |
| +3.3 V | ±5 % |
| +5 V | ±5 % |
| -5 V | ±5 % |
| +12 V | ±5 % |
| -12 V | ±5 % |
| **Vibration** | |
| Unpackaged | 5 Hz to 20 Hz : 0.01g² Hz sloping up to 0.02 g² Hz |
| | 20 Hz to 500 Hz : 0.02g² Hz (flat) |
| Packaged | 10 Hz to 40 Hz : 0.015g² Hz (flat) |
| | 40 Hz to 500 Hz : 0.015g² Hz sloping down to 0.00015 g² Hz |

## 1.15 Power Consumption

Table 34 lists the voltage and current specifications for a motherboard being used in a hypothetical system. The motherboard has all manufacturing options, and uses a 166 MHz Pentium processor and 16 MB of EDO DRAM. The system power supply is a 200 watt LPX power supply with at least 65% efficiency. This information is preliminary and is provided only as a guide for calculating **approximate** system power usage with additional resources added.

**Table 34. Power Usage**

| | | DC (amps) | | | | | |
|---|---|---|---|---|---|---|---|
| **System Operating Conditions** | **AC (watts)** | **+3.3 V** | **+5 V** | **-5 V** | **+12 V** | **-12 V** | **+5VSB** |
| APM enabled, idle and running Windows 95 desktop | 24.4 | 420 mA | 2.2 A | < 10 mA | 114 mA | 40 mA | N/A |
| APM disabled, running Windows 95 desktop | 28 | 426 mA | 4.0 A | < 10 mA | 114 mA | 41 mA | N/A |
| System powered down | N/A | N/A | N/A | N/A | N/A | N/A | < 10 mA |

### 1.15.1 Power Supply Considerations

The CU430HX is designed to operate with a 200 watt LPX power supply. In addition to supporting the required soft-OFF function, the power supply must meet the following specifications:

- Rise time for power supply - 2ms to 20ms
- Minimum delay from RESET to Powergood - 100ms
- Minimum Powerdown warning - 1ms

## 1.16 Regulatory Compliance

This printed circuit assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system.

### 1.16.1 Safety

#### 1.16.1.1 UL 1950 - CSA 950-95, 3rd edition, Dated 3-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada).

#### 1.16.1.2 CSA C22.2 No. 950-93, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

#### 1.16.1.3 EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

#### 1.16.1.4 IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

#### 1.16.1.5 EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

### 1.16.2 EMI

#### 1.16.2.1 FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)

#### 1.16.2.2 CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

#### 1.16.2.3 EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

#### 1.16.2.4 EN 50 082-1 (1992)

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3 and -- 4. (Europe)

#### 1.16.2.5 VCCI Class 2 (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

#### 1.16.2.6 ICES-003, Issue 2

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

### 1.16.3 Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of a marking on the board or shipping container.
- UL Recognition Mark: Consists of the UL File No. E139761 on the component side of the board and the PBA No. on the solder side of the board. Board material flammability is 94V-1 or -0.
- Canadian Compliance: Consists of small c followed by a stylized backward UR on component side of board.

# 2 Motherboard Resources

## 2.1 Memory Map

**Table 35. Memory Map**

| Address Range (Decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| 1024K-196608K | 100000-C000000 | 191M | Extended Memory |
| 960K-1023K | F0000-FFFFF | 64K | Main BIOS |
| 944K-959K | EC000-EFFFF | 16K | Boot Block (Available as UMB) |
| 936K-943K | EA000-EBFFF | 8K | VPD ESCD- DMI Configuration Info |
| 932K-935K | E9000-E9FFF | 4K | 4KB Reserved for BIOS |
| 928k-931K | E8000-E8FFF | 4K | OEM Logo Area or Scan User Flash |
| 896K-927K | E0000-E7FFF | 32K | Post BIOS (Available as UMB) |
| 800K-895K | C8000-DFFFF | 96K | Available HI DOS Memory(open to ISA & PCI bus |
| 640K-799K | A0000-C7FFF | 160K | On-board video memory and BIOS |
| 639K | 9FC00-9FFFF | 1K | Extended BIOS Data(Moveable by QEMM, 386MAX) |
| 512K-638K | 80000-9FBFF | 127K | Extended Conventional |
| 0K-511K | 00000-7FFFF | 512K | Conventional Memory |

## 2.2 I/O Map

**Table 36. I/O Map**

| Address (hex) | Size | Description |
|---|---|---|
| 0000 - 000F | 16 bytes | PIIX3 - DMA 1 |
| 0020 - 0021 | 2 bytes | PIIX3 - Interrupt Controller 1 |
| 002E - 002F | 2 bytes | Super I/O configuration registers |
| 0040 - 0043 | 4 bytes | PIIX3 - counter 1 |
| 0048 - 004B | 4 bytes | PIIX3 - counter 2 |
| 0060 | 1 byte | Keyboard Controller Byte - Reset IRQ |
| 0061 | 1 byte | PIIX3 - NMI, speaker control |
| 0064 | 1 byte | Keyboard Controller, CMD/STAT Byte |
| 0070, bit 7 | 1 bit | PIIX3 - Enable NMI |
| 0070, bits 6:0 | 7 bits | PIIX3 - Real Time Clock, Address |
| 0071 | 1 byte | PIIX3 - Real Time Clock, Data |
| 0078 | 1 byte | Reserved - board configuration |

continued ☛

**Table 36. I/O Map (continued)**

| Address (hex) | Size | Description |
|---|---|---|
| 0079 | 1 byte | Reserved - board configuration |
| 80h | 1 byte | Monitors and stores POST codes (used during POST) |
| 85h | 1 byte | Address and control functions (used during POST) |
| 86h | 1 byte | Register read/write operations (used during POST) |
| 0080 - 008F | 16 bytes | PIIX3 - DMA Page Register |
| 00A0 - 00A1 | 2 bytes | PIIX3 - Interrupt Controller 2 |
| 00B2 - 00B3 | 2 bytes | APM control |
| 00C0 - 00DE | 31 bytes | PIIX3 - DMA 2 |
| 00F0 | 1 byte | Reset Numeric Error |
| 0170 - 0177 | 8 bytes | Secondary IDE Channel |
| 01F0 - 01F7 | 8 bytes | Primary IDE Channel |
| 0200 - 0207 | 8 bytes | Audio (reserved) |
| 0220 - 022F | 16 bytes | Audio (SB compatible) |
| 0240 - 024F | 16 bytes | Audio (SB compatible) |
| 0260 - 026F | 16 bytes | Audio (SB compatible) |
| 0278 - 027B | 4 bytes | Parallel port 2 |
| 0280 - 028F | 16 bytes | Audio (SB compatible) |
| 0290 - 0297 | 8 bytes | H/W Monitoring ASIC |
| 02E8 | 1 byte | Video (8514A) |
| 02F8 - 02FF | 8 bytes | COM2 |
| 0300 - 0301 | 2 bytes | MPU - 401 (MIDI) |
| 0330 - 0331 | 2 bytes | MPU - 401 (MIDI) |
| 0376 | 1 byte | Sec IDE Chan Cmd Port |
| 0377 | 1 byte | Floppy channel 2 command |
| 0377, bit 7 | 1 bit | Floppy disk chng channel 2 |
| 0377, bits 6:0 | 7 bits | Sec IDE Chan Status Port |
| 0378 - 037F | 8 bytes | LPT1 |
| 0388 - 038D | 6 bytes | AA LIB (FM synth) |
| 03B4 - 03B5 | 2 bytes | Video (VGA) |
| 03BA | 1 byte | Video (VGA) |
| 03BC - 03BF | 4 bytes | LPT3 |
| 03C0 - 03CA | 11 bytes | Video (VGA) |
| 03CC | 1 byte | Video (VGA) |
| 03CE - 03CF | 2 bytes | Video (VGA) |
| 03D4 - 03D5 | 2 bytes | Video (VGA) |
| 03DA | 1 byte | Video (VGA) |
| 03E8 - 03EF | 8 bytes | COM3 |
| 03F0 - 03F5 | 6 bytes | Floppy Channel 1 |

continued ☛

**Table 36. I/O Map (continued)**

| Address (hex) | Size | Description |
|---|---|---|
| 03F6 | 1 byte | Pri IDE Chan Cmd Port |
| 03F7 (Write) | 1 byte | Floppy Chan 1 Cmd |
| 03F7, bit 7 | 1 bit | Floppy Disk Chg Chan 1 |
| 03F7, bits 6:0 | 7 bits | Pri IDE Chan Status Port |
| 03F8 - 03FF | 8 bytes | COM1 |
| 04D0 - 04D1 | 2 bytes | Edge/level triggered |
| LPT + 400h | 8 bytes | ECP port |
| 0530 - 0537 | 8 bytes | Windows sound system |
| 0604 - 060B | 8 bytes | Windows sound system |
| 0CF8* | 4 bytes | PCI Config Address Reg. |
| 0CF9** | 1 byte | Turbo & Reset Control Reg. |
| 0CFC-0CFF | 4 bytes | PCI Config Data Register |
| 0E80 - 0E87 | 8 bytes | Windows sound system |
| 0F40 - 0F47 | 8 bytes | Windows sound system |
| 0F86 - 0F87 | 2 bytes | Yamaha OPL3 configuration |
| FF00 - FF07 | 8 bytes | IDE Bus Master Reg. |
| FFA0 - FFA7 | 8 bytes | Primary Bus Master IDE Registers |
| FFA8 - FFAF | 8 bytes | Secondary Bus Master IDE Registers |

* DWORD access only

** Byte access only

## 2.3 PCI Configuration Space Map

**Table 37. PCI Configuration Space Map**

| Bus Number (hex) | Dev Number (hex) | Function Number (hex) | Description |
|---|---|---|---|
| 00 | 00 | 00 | Intel 82437HX (TXC) |
| 00 | 07 | 00 | Intel 82371FB (PIIX3 ) PCI/ISA bridge |
| 00 | 07 | 01 | Intel 82371FB (PIIX3 ) IDE Bus Master |
| 00 | 07 | 02 | Intel 82371FB (PIIX3 ) USB |
| 00 | 08 | 00 | ATI VGA Graphics |
| 00 | 0C | 00 | Intel 82557 Ethernet Network |
| 00 | 11 | 00 | PCI Expansion Slot: User Available |
| 00 | 13 | 00 | PCI Expansion Slot: User Available |
| 00 | 0B | 00 | PCI Expansion Slot: User Available for 3-slot riser |

## 2.4 DMA Channels

**Table 38. DMA Channels**

| DMA | Data Width | System Resource |
|---|---|---|
| 0 | 8- or 16-bits | |
| 1 | 8- or 16-bits | Audio |
| 2 | 8- or 16-bits | Floppy |
| 3 | 8- or 16-bits | Parallel Port (for ECP/EPP Config.) |
| 4 | | Reserved - Cascade channel |
| 5 | 16-bits | Audio |
| 6 | 16-bits | Open |
| 7 | 16-bits | Open |

## 2.5 Interrupts

**Table 39. Interrupts**

| IRQ | System Resource |
|---|---|
| NMI | I/O Channel Check |
| 0 | Reserved, Interval Timer |
| 1 | Reserved, Keyboard buffer full |
| 2 | Reserved, Cascade interrupt from slave PIC |
| 3 | COM2 * |
| 4 | COM1 * |
| 5 | Audio * |
| 6 | Floppy |
| 7 | LPT1 * |
| 8 | Real Time Clock |
| 9 | Onboard Ethernet * |
| 10 | USB * |
| 11 | User available |
| 12 | Onboard Mouse Port if present, else user available |
| 13 | Reserved, Math coprocessor |
| 14 | Primary IDE if present, else user available |
| 15 | Secondary IDE if present, else user available |

* Moveable resources that depend on user configuration. Resources shown are for a typical configuration.

# 3 Motherboard BIOS and Setup Utility

## 3.1 Introduction

The motherboard uses an Intel BIOS, which is stored in Flash EEPROM and easily upgraded using a floppy disk-based program. In addition to the Intel BIOS, the Flash EEPROM also contains the Setup utility, Power-on Self Tests (POST), APM 1.2, the PCI auto-configuration utility, and Windows 95 ready Plug and Play. This motherboard also supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a sign-on message during POST identifying the type of BIOS and a five-digit revision code. The initial production BIOS in the motherboard will be identified as 1.00.01.DK0.

Information on BIOS functions can be found in the *IBM PS/2 and Personal Computer BIOS Technical Reference* published by IBM, and the *ISA and EISA Hi-Flex AMIBIOS Technical Reference* published by AMI. Both manuals are available at most technical bookstores.

## 3.2 BIOS Flash Memory Organization

The Intel E28F002BX 2Mb Flash component is organized as 256K x 8 (256 KB). The Flash device is divided into several areas, as described in Table 40.

**Table 40. Flash Memory Organization**

| System Address (Hex) | Size | Description |
|---|---|---|
| FFFF0000 - FFFFFFFF | 64 KB | Main BIOS block |
| FFFEC000 - FFFEFFFF | 16 KB | Boot block (available as UMB) |
| FFFEA000 - FFFEBFFF | 8 KB | VPD ESCD (DMI configuration information) |
| FFFE9000 - FFFE9FFF | 4 KB | Reserved for BIOS |
| FFFE8000 - FFFE8FFF | 4 KB | OEM logo or Scan User Flash |
| FFFE0000 - FFFE7FFF | 32 KB | Main BIOS block |
| FFFD0000 - FFFDFFFF | 64 KB | Main BIOS block |
| FFFC0000 - FFFCFFFF | 64 KB | Main BIOS block |

## 3.3 BIOS Upgrades

Flash memory makes distributing BIOS upgrades easy. A new version of the BIOS can be installed from a diskette. General BIOS upgrade instructions are available at the Intel World Wide Web site at *http://www-cs.intel.com/oem_developer/motherbd/genbios.htm*. BIOS updates can also be downloaded from Intel's FTP site at *ftp://ftp.intel.com/pub/bios*.

The disk-based Flash upgrade utility, FMUP.EXE, has three options for BIOS upgrades:

- The Flash BIOS can be updated from a file on a disk;
- The current BIOS code can be copied from the Flash EEPROM to a disk file as a backup in the event that an upgrade cannot be successfully completed; or
- The BIOS in the Flash device can be compared with a file to ensure the system has the correct version.

The upgrade utility ensures the upgrade BIOS extension matches the target system to prevent accidentally installing a BIOS for a different type of system.

## 3.4 PCI IDE Support

The two local bus IDE connectors with independent I/O channel support are setup up automatically by the BIOS if the user selects "Autoconfiguration" in setup. The IDE interface supports PIO Mode 3, and Mode 4 hard drives and recognition of ATAPI CD-ROMs, tape drives, and any other ATAPI devices. The BIOS will determine the capabilities of each drive and configure them to optimize capacity and performance. For the high capacity hard drives typically available today, the drive will be automatically be configured for Logical Block Addressing (LBA) for maximum capacity and to PIO Mode 3 or 4 depending on the capability of the drive. The user is able to override the auto-configuration options by using the manual mode setting. The ATAPI Specification Revision 2.5 recommends that an ATAPI device be configured as shown in Table 41.

**Table 41. Recommendations for Configuring an ATAPI Device**

| Primary Cable | | Secondary Cable | | |
|---|---|---|---|---|
| Drive 0 | Drive 1 | Drive 0 | Drive 1 | |
| ATA | | | | Normal, no ATAPI |
| ATA | | ATAPI | | Disk and CD-ROM for enhanced IDE systems |
| ATA | ATAPI | | | Legacy IDE System with only one cable |
| ATA | | ATAPI | ATAPI | Enhanced IDE with CD-ROM and a tape or two CD-ROMs |

## 3.5 PCI Auto-configuration

The PCI auto-configuration utility operates in conjunction with the system Setup utility to allow the insertion and removal of PCI cards to the system without user intervention (Plug and Play). When the system is turned on after adding a PCI add-in card, the BIOS automatically configures interrupts, I/O space, and other parameters. PCI interrupts are distributed to available ISA interrupts that have been not been assigned to an ISA card, or system resources. Those interrupts left set to "available" in the CMOS setup will be considered free for PCI add-in card use. It is nondeterministic as to which PCI interrupt will be assigned to which ISA IRQ.

The PCI auto-configuration function complies with version 2.10 of the PCI BIOS specification. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position.

PCI specification 2.1 for add-in card auto-configuration is also a part of the Plug and Play BIOS. Peer-to-peer hierarchical PCI Bridge 1.0 is supported, and by using an OEM supplied option ROM or TSR, a PCI-to-PCMCIA bridge capability is possible as well.

## 3.6 ISA Plug and Play

The BIOS incorporates ISA Plug and Play capabilities as delivered by Plug and Play Release 1.0A (Plug and Play BIOS V.. 1.0A, ESCD V.. 1.03). When used in conjunction with the ISA Configuration Utility (ICU) for DOS or Windows 3.x, the system allows auto-configuration of Plug and Play ISA cards, PCI cards, and resource management for legacy ISA cards. Because the BIOS supports configuring devices across PCI bridges, release 1.41 or greater of the ICU must be used with the motherboard to properly view and change system settings. System configuration information is stored in ESCD format. The ESCD data may be cleared by setting the CMOS clear jumper to the ON position .

The BIOS also has a setup option to support the Windows 95 run time plug and play utilities. When this option is selected, only devices critical to booting are assigned resources by the BIOS. Device Node information is available for all devices to ensure compatibility with Windows 95.

Copies of the IAL Plug and Play specification may be accessed through Intel's web site at *http://www.intel.com/ial/plugplay/* or they can be downloaded from the Microsoft FTP site at *ftp://ftp.microsoft.com/developr/drg/Plug-and-Play/Pnpspecs*.

## 3.7 Advanced Power Management

The BIOS has support for Advanced Power Management (APM version 1.1). The energy saving Stand By mode can be initiated by a keyboard hot key sequence set by the user, a time-out period set by the user, or by a suspend/resume button tied to the front panel sleep connector.

When in Stand-by mode, the motherboard reduces power consumption by utilizing the Pentium processor's System Management Mode (SMM) capabilities and also spinning down hard drives and turning off VESA DPMS compliant monitors. The user may select which DPMS mode (Stand By, Suspend, or Off) send to the monitor in setup. The ability to respond to external interrupts is fully maintained while in Stand-by mode allowing the system to service requests such as in-coming Fax's or network messages while unattended. Any keyboard or mouse activity brings the system out of the energy saving Stand By mode. When this occurs the monitor and IDE drives are turned back on immediately.

APM is enabled in BIOS by default, however, the system must be configured with an APM driver in order for the system power saving features to take effect. Windows 95 will enable APM automatically upon detecting the presence of the APM BIOS.

## 3.8 Language Support

The BIOS setup screen and help messages are supported in 32 languages. There are five languages available at this time; American English, German, Italian, French, and Spanish. Translations of other languages could become available at a later date.

With a 2 Mb Flash BIOS, only two languages can be resident at a time. The default language is American English, and is always present unless another language is programmed into the BIOS using the Flash Memory Update Program (FMUP). The FMUP utility is available through the Intel World Wide Web site at *http://www-cs.intel.com/oem_developer/motherbd/genbios.htm*, or from Intel's FTP site at *ftp://ftp.intel.com/pub/bios*, or call your local Intel sales office. American English is the only language present in the standard BIOS.

## 3.9 Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the Boot Options field in setup, CD-ROM is one of four possible boot devices which are defined in priority order. The default setting is for floppy to be the primary boot device and hard drive to be the secondary boot device. If CD-ROM is selected, it must be the first device. The third and fourth devices are set to Disabled in the default configuration. The user can add also select Network as a boot device. The network option allows booting from a network add-in card with a remote boot ROM installed.

**⟹ NOTE**

*A copy of "El Torito" is available from the Phoenix Web page (http://www.ptltd.com/techs/specs.html).*

## 3.10 Flash LOGO Area

The motherboard supports a 4 KB programmable FLASH user area located at FFFE8000 - FFFE8FFF. An OEM may use this area to display a custom logo. The BIOS accesses the user area just after completing POST. A utility is available from Intel to assist with installing a logo into flash for display during POST.

## 3.11 Setup Enable Jumper

A motherboard configuration jumper controls access to the BIOS Setup utility. By setting the jumper to the disable position, the user is prevented from accessing the Setup utility during the Power-on Self Test or at any other time. The message prompting the user to press <F1> to enter setup is also disabled.

## 3.12 BIOS Setup Utility

The ROM-based Setup utility allows the configuration to be modified without opening the system for most basic changes. The Setup utility is accessible only during the Power-on Self Test (POST) by pressing the <F1> key after the POST memory test has begun and before boot begins. A prompt may be enabled that informs users to press the <F1> key to access Setup. A jumper setting on the motherboard can be set to prevent user access to Setup for security purposes.

### 3.12.1 Overview of the Setup Menu Screens

The Setup program initially displays the Main menu screen. In each screen there are options for modifying the system configuration. Select a menu screen by pressing the left <←> or right <→> arrow keys. Use the up <↑> or down <↓> arrow keys to select items in a screen. Use the <Enter> key to select an item for modification. For certain items, pressing <Enter> will bring up a subscreen. After you have selected an item, use the arrow keys to modify the setting.

**Table 42. Overview of the Setup Menu Screens**

| Setup Menu Screen | Description |
|---|---|
| Main | For setting up and modifying some of the basic options of a PC, such as time, date, diskette drives, hard drives. |
| Advanced | For modifying the more advanced features of a PC, such as peripheral configuration and advanced chipset configuration. |
| Security | For specifying passwords that can be used to limit access to the system. |
| Exit | For saving or discarding changes. |
| **Setup Subscreen** | **Description** |
| Floppy Options | For configuring your diskette drives. |
| Hard Disk Configuration | For configuring your hard drives. |
| Boot Options | For modifying options that affect the system boot up, such as the boot sequence. |
| Peripheral Configuration | For modifying options that affect the serial ports, the parallel port, and the disk drive interfaces. |
| Advanced Chipset Configuration | For modifying options that affect memory and system busses. |
| Power Management Configuration | For accessing and modifying Advanced Power Management (APM) options. |
| Plug and Play Configuration | For modifying options that affect the system's Plug and Play capabilities. |
| Event Logging Configuration | For modifying and viewing the hardware management devices and logs. |

### 3.12.2 Main BIOS Setup Screen

This section describes the Setup options found on the main menu screen. If you select certain options from the main screen (e.g., Hard Disk), the Setup program switches to a subscreen for the selected option.

#### 3.12.2.1 System Date

Specifies the current date. Select the month from a pop-up menu.

#### 3.12.2.2 System Time

Specifies the current time. Type over the current time to set a new time.

#### 3.12.2.3 Floppy Options

When selected, this pops up the Floppy Options menu.

#### 3.12.2.4 Hard Disk C:, D:, E:, F:

Reports if a hard disk is connected to the system. When selected, this brings up the Hard Disk Configuration subscreen.

#### 3.12.2.5 Language

Specifies the language of the text strings used in the Setup program and the BIOS. The options are any installed languages.

#### 3.12.2.6 Boot Options

When selected, this brings up the Boot Options subscreen.

#### 3.12.2.7 Video Mode

Reports the video mode. There are no options.

#### 3.12.2.8 Mouse

Reports if a mouse is installed or not. There are no options.

#### 3.12.2.9 Base Memory

Reports the amount of base memory. There are no options.

#### 3.12.2.10 Extended Memory

Reports the amount of extended memory. There are no options.

#### 3.12.2.11 BIOS Version

Reports the version of the BIOS installed. There are no options.

## 3.12.3 Floppy Options Subscreen

### 3.12.3.1 Floppy A:

Reports if a diskette drive is connected to the system. There are no options.

### 3.12.3.2 Floppy B:

Reports if a second diskette drive is connected to the system. There are no options.

### 3.12.3.3 Floppy A: Type

Specifies the physical size and capacity of the diskette drive. The options are Disabled, 360 KB, 5¼-inch; 1.2 MB, 5¼-inch; 720 KB, 3½-inch; 1.44/1.25 MB, 3½-inch; 2.88 MB, 3½-inch. The default is 1.44/1.25 MB, 3½-inch.

### 3.12.3.4 Floppy B: Type

Specifies the physical size and capacity of the diskette drive. The options are Disabled, 360 KB, 5¼-inch; 1.2 MB, 5¼-inch; 720 KB, 3½-inch; 1.44/1.25 MB, 3½-inch; 2.88 MB, 3½-inch. The default is Disabled.

### 3.12.3.5 Floppy Access

Sets whether the floppy drive is writeable or not. The options are READ/WRITE or READ ONLY.

## 3.12.4 Hard Disk Configuration Subscreen

### 3.12.4.1 IDE Device Configuration

Used to manually configure the hard drive or have the system auto configure it. The options are Auto Configured and User Definable. The default is Auto Configured. If you select User Definable then the Number of Cylinders, Number of Heads, and Number of Sectors items can be modified.

### 3.12.4.2 Number of Cylinders

If Hard Disk Type is set to User Definable, you must type the correct number of cylinders for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of cylinders for your hard disk and cannot be modified.

### 3.12.4.3 Number of Heads

If Hard Disk Type is set to User Definable, you must type the correct number of heads for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of heads for your hard disk and cannot be modified.

### 3.12.4.4 Number of Sectors

If Hard Disk Type is set to User Definable, you must type the correct number of sectors for your hard disk. If Hard Disk Type is set to Auto Configured, this reports the number of sectors for your hard disk and cannot be modified.

### 3.12.4.5 Maximum Capacity

Reports the maximum capacity of your hard disk. It is calculated from the number of cylinders, heads, and sectors. There are no options here.

### 3.12.4.6 IDE Translation Mode

Specifies the IDE translation mode. The options are Standard CHS (standard cylinder head sector –less than 1024 cylinders), Logical Block, Extended CHS (extended cylinder head sector–greater than 1024 cylinders), and Auto Detected (BIOS detects IDE drive support for LBA). The default is Auto Detected.

**⚠ CAUTION**

*Do not change this from the option selected when the hard drive was formatted. Changing the option can result in corrupted data.*

### 3.12.4.7 Multiple Sector Setting

Sets the number of sectors transferred by an IDE drive per interrupt generated. The options are Disabled, 4 Sectors/Block, 8 Sectors/Block, or Auto Detected. The default is Auto Detected. Check the specifications for your hard disk drive to determine which setting provides optimum performance for your drive.

### 3.12.4.8 Fast Programmed I/O Modes

Sets how fast transfers on the IDE interface occur. The options are Disabled or Auto Detected. The default is Auto Detected. If set to Disabled, transfers occur at a less than optimized speed. If set to Auto Detected, transfers occur at the drive's maximum speed.

## 3.12.5 Boot Options Subscreen

This section describes the options available on the Boot Options subscreen.

### 3.12.5.1 First, Second, Third, Fourth Boot Device

Sets which drives the system checks to find an operating system to boot from. The following options are available:

| | |
|---|---|
| First Boot Device: | Select Disabled, Floppy, Hard Disk, CD-ROM, Network. |
| Second, Third, Fourth Device: | Select Disabled, Floppy, Hard Disk, Network. |

### 3.12.5.2 System Cache

Enables or disables both the primary and the secondary cache memory. The options are Enabled or Disabled. The default is Enabled.

### 3.12.5.3 Boot Speed

Sets the system's boot speed. The options are Deturbo and Turbo. The default is Turbo. If Turbo is selected, boot-up occurs at full speed. If Deturbo is selected, the board operates at a slower speed.

### 3.12.5.4 Num Lock

Sets the beginning state of the Num Lock feature on your keyboard. The options are On and Off. The default is Off.

### 3.12.5.5 Setup Prompt

Turns on (or off) the "Press <F1> Key if you want to run Setup" prompt during the power-up sequence. The options are Enabled and Disabled. The default is Enabled.

**NOTE**

*This option has no effect on your ability to access the Setup program. It only toggles the prompt.*

### 3.12.5.6 Hard Disk Pre-delay

Sets the hard disk drive pre-delay. The options are Disabled, 3, 6, 9, 12, 15, 21 or 30 seconds. The default is 3 seconds. When enabled, this option causes the BIOS to wait the specified time before it accesses the first hard drive. If your system contains a hard drive, and you don't see the drive type displayed during boot-up, the hard drive may need more time before it is able to communicate with the controller. Setting a pre-delay provides additional time for the hard drive to initialize.

### 3.12.5.7 Typematic Rate Programming

Sets the typematic rates. The options are Default and Override. The default is Default. Choosing Override enables Typematic Rate Delay and Typematic Rate.

### 3.12.5.8 Typematic Rate Delay

Sets how long it takes for the key-repeat function to start when you hold down a key on the keyboard. The options are 250, 500, 750, and 1000 millisecond delays. The default is 250. If Typematic Rate Programming is set to Default, this option will not be visible.

#### 3.12.5.9 Typematic Rate

Sets the speed at which characters repeat when you hold down a key on the keyboard. The higher the number, the faster the characters repeat. The options are 6, 8, 10, 12, 15, 20, 24, and 30 characters per second. The default is 6. If Typematic Rate Programming is set to Default, this option will not be visible.

#### 3.12.5.10 Scan User Flash Area

Allows a user's program to scan the user Flash area for user data The default is set to Disabled.

### 3.12.6 Advanced Screen

This section describes the Setup options found on the Advanced menu screen. If you select certain options from the Advanced screen (e.g., Peripheral Configuration), the Setup program switches to a subscreen for the selected option. Subscreens are described in the sections following the description of the Advanced screen options.

#### 3.12.6.1 Processor Type

Reports the CPU type. There are no options.

#### 3.12.6.2 Processor Speed

Reports the CPU clock speed. There are no options.

#### 3.12.6.3 Cache Size

Reports the size of the secondary cache. There are no options. If your system contains no L2 cache, this item will not appear.

#### 3.12.6.4 Peripheral Configuration

When selected, this brings up the Peripheral Configuration subscreen.

#### 3.12.6.5 Advanced Chipset Configuration

When selected, this brings up the Advanced Chipset Configuration subscreen.

#### 3.12.6.6 Power Management Configuration

When selected and enabled, this brings up the Advanced Power Management subscreen.

#### 3.12.6.7 Plug and Play Configuration

When selected, this brings up the Plug and Play Configuration subscreen.

#### 3.12.6.8 Event Logging Configuration

When selected, this brings up the Event Logging Configuration subscreen.

## 3.12.7 Peripheral Configuration Subscreen

This section describes the screens for the peripheral configuration subscreen.

### 3.12.7.1 Primary PCI IDE Interface

Enables or disables the primary PCI IDE hard disk interface. The options are Auto Configured and Disabled. The default is Auto Configured. (If Configuration Mode is set to Auto Configured, this option cannot be modified.)

### 3.12.7.2 Secondary PCI IDE Interface

Enables or disables the secondary PCI IDE hard disk interface. The options are Auto Configured and Disabled. The default is Auto Configured. (If Configuration Mode is set to Auto Configured, this option cannot be modified.)

### 3.12.7.3 Floppy Interface

Enables or disables the diskette drive interface. The options are Auto Configured, Enabled, and Disabled. The default is Auto Configured.

### 3.12.7.4 Serial Port 1 Address

Selects the address of the serial port. The options are described and listed in Table 43.

**Table 43. Serial Port Configuration Options**

| Option | Description |
|---|---|
| Disable | Port not enabled |
| COM1, 3F8, IRQ4 | Enabled as COM1 at indicated I/O address and IRQ |
| COM2, 2F8, IRQ3 | Enabled as COM2 at indicated I/O address and IRQ |
| COM3, 338, IRQ4 | Enabled as COM3 at indicated I/O address and IRQ |
| COM4, 238, IRQ3 | Enabled as COM4 at indicated I/O address and IRQ |
| COM1, 3F8, IRQ3 | Enabled as COM1 at indicated I/O address and IRQ |
| COM2, 2F8, IRQ4 | Enabled as COM2 at indicated I/O address and IRQ |
| COM3, 338, IRQ3 | Enabled as COM3 at indicated I/O address and IRQ |
| COM4, 238, IRQ4 | Enabled as COM4 at indicated I/O address and IRQ |
| Auto Configured | Port will be auto configured (Default option) |

### 3.12.7.5 Serial Port 2 Address

Selects the address of the serial port. The options are described and listed in Table 43.

**NOTE**

*If either serial port address is set, the address it is set to will not appear in the options dialog box of the other serial port. If an ATI mach32† or an ATI mach64† video controller is active, the COM4, 2E8h address will not appear in the options dialog box of either serial port.*

### 3.12.7.6 Serial Port 2 IR Mode

Makes Serial Port 2 available to infrared applications. The options are Enabled and Disabled. The default is Disabled. (If Configuration Mode is set to Auto, this option cannot be modified.)

### 3.12.7.7 Parallel Port Address

Selects the address and IRQ of the parallel port. The options are described and listed in Table 44.

**Table 44. Parallel Port Configuration Options**

| Option | Description |
|---|---|
| Disable | Port not enabled |
| LPT3, 3BC, IRQ7 | Enabled as LPT3 at indicated I/O address and IRQ |
| LPT1, 378, IRQ7 | Enabled as LPT1 at indicated I/O address and IRQ (Default option) |
| LPT2, 278, IRQ7 | Enabled as LPT2 at indicated I/O address and IRQ |
| LPT3, 3BC, IRQ5 | Enabled as LPT3 at indicated I/O address and IRQ |
| LPT1, 378, IRQ5 | Enabled as LPT1 at indicated I/O address and IRQ |
| LPT2, 278, IRQ5 | Enabled as LPT2 at indicated I/O address and IRQ |
| Auto Configured | Port will be auto configured |

### 3.12.7.8 Parallel Port Mode

Selects the mode for the parallel port. The options are Compatible, Bi-directional, EPP, and ECP. The default is Compatible. Compatible means the parallel port operates in AT-compatible mode. Bi-directional means the parallel port operates in bi-directional PS/2-compatible mode. EPP and ECP mean the parallel port operates high-speed, bidirectionally. This option is not affected by the Configuration Mode field above.

### 3.12.7.9 USB Interface

This option enables the Universal Serial Bus (USB) interface. If this option is Disabled, the USB ports will not be recognized. The default is Enabled.

### 3.12.7.10 Audio Interface

This option Enables the Vibra 16C audio subsystem. If this option is Disabled, it frees the I/O resources and addresses used to support this audio interface. The default is Enabled.

### 3.12.7.11 Hardware Monitor Interface

This option Enables or Disables the hardware monitor subsystem. The default is Enabled.

### 3.12.7.12 PCI LAN Interface

This option Enables or Disables the onboard LAN interface. The default is Enabled.

### 3.12.8 Advanced Chipset Configuration Subscreen

This section describes the options available on the Advanced Chipset Configuration Subscreen.

#### 3.12.8.1 Base Memory Size

Sets the size of the base memory. The options are 512 KB and 640 KB. The default is 640 KB.

#### 3.12.8.2 ISA LFB Size

Sets the size of the linear frame buffer. The options are Disabled and 1MB. The default is Disabled. If this is set to 1 MB, then the ISA LFB Base Address field will appear.

#### 3.12.8.3 ISA LFB Base Address

Reports the base address of the LFB. There are no options. This field will not appear if the ISA LFB Size is set to Disabled. If the ISA LFB size is 1MB, the base address is 15MB.

#### 3.12.8.4 Video Palette Snoop

Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card. The options are Enabled and Disabled. The default is Disabled.

#### 3.12.8.5 Latency Timer (PCI Clocks)

Sets the length of time an agent on the PCI bus can hold the bus when another agent has requested the bus. Valid numbers are between 0 and 256. The default is 66.

#### 3.12.8.6 Bank 0 SIMM Detected

Reports the type of memory found in the bank 0 SIMM slots. There are no options.

#### 3.12.8.7 Bank 1 SIMM Detected

Reports the type of memory found in the bank 1 SIMM slots. There are no options.

#### 3.12.8.8 Bank 2 SIMM Detected

Reports the type of memory found in the bank 2 SIMM slots. There are no options.

### 3.12.9 Power Management Configuration Subscreen

This section describes the options available on the Power Management Subscreen.

#### 3.12.9.1 Advanced Power Management

Enables or disables the Advanced Power Management (APM) support in your system's BIOS. The options are Enabled and Disabled. The default is Disabled. Power Management will only work with APM-capable operating systems to manage power consumption in your system. If Advanced Power Management is set to Disabled, none of the fields in the Advanced Power Management subscreen will be visible.

### 3.12.9.2 IDE Drive Power Down

Sets any IDE drives to spin down when the system goes into power managed mode. The options are Enabled and Disabled. The default is Enabled.

### 3.12.9.3 Inactivity Timer

Sets how long the system must be inactive before it enters power managed mode. Enter the number of minutes. The range is 0 to 255 minutes. The default is 10 minutes.

### 3.12.9.4 Hot Key

Sets the hot key that, when pressed while holding down the <Ctrl> and <Alt> keys, causes the system to enter power managed mode. All alphabetic keys are valid.

## 3.12.10 Plug and Play Configuration Subscreen

This section describes the options found on the Plug and Play configuration subscreen.

### 3.12.10.1 Configuration Mode

Sets how the BIOS gets information about ISA cards that do not have Plug and Play capabilities. The options are Use BIOS Setup and Use PnP OS. The default is Use PnP OS.

If Use PnP OS is selected, the BIOS will depend on run-time software to ensure that there are no conflicts between ISA boards with Plug and Play capabilities and those without. Only Boot With PnP OS will be visible.

### 3.12.10.2 Boot with PnP OS

Enables the PC to boot with an operating system capable of managing Plug and Play add-in cards. The options are None, Other, and Windows 95. The default is Windows 95.

### 3.12.10.3 ISA Shared Memory Size

Enables you to specify a range of memory addresses that will be directed to the ISA bus rather than on-board memory. The options are Disabled, 16 KB, 32 KB, 48 KB, 64 KB, 80 KB, and 96 KB. The default is Disabled. If this is set to Disabled, the ISA Shared Memory Base Address (described below) will not be visible.

This field should be set to Enabled only when a non Plug and Play ISA card (legacy card) that requires non-ROM memory space is used. LAN cards that have on-board memory buffers are one example of this; video capture cards that have video buffer memory are another.

By default, allocation of upper memory is as follows: memory from C0000-C7FFF is automatically shadowed. (This memory range is typically reserved for video BIOS.) Memory from C8000-DFFFFh is initially unshadowed. The BIOS scans this range for any ISA expansion card BIOSes that may be present and notes their location and size. The BIOS will then autoconfigure the PCI and Plug and Play devices, shadowing the ROM requirements (other than video) into the area above E0000h until that area is full. It will then assign additional PCI and

Plug and Play expansion cards to the area between C8000h and DFFFFh. If an ISA legacy card has non-ROM memory requirements, the autoconfigure routine may write into an area that is needed by the ISA expansion card. The ISA Shared Memory Size parameter signifies the autoconfigure routine that this block of memory is reserved and should not be shadowed.

Shadowing is a technique that copies a block of memory from an add-in card's ROM to the same address in system memory. This provides faster access and achieves higher performance. By default, all upper memory is shadowed.

#### 3.12.10.4 ISA Shared Memory Base Address

Sets the base address for the ISA Shared Memory. The options are C8000h, CC000h, D0000h, D4000h, D8000h, and DC000h. The default is C8000h. This setting could affect the ISA Shared Memory Size item. The value entered in the ISA Shared Memory Size item cannot extend to the E0000h address. For example, if a size of 64K was selected, options D4000h, D8000h, and DC000h will not be available.

#### 3.12.10.5 IRQ 3, 4, 5, 7, 9, 10, 11, 12

Sets the status of the IRQ. The options are Available and Used By ISA Card. The default is Available. The PCI auto-configuration code looks here to see if these interrupts are available for use by a PCI or Plug and Play device. If an interrupt is available, the PCI auto-configuration code or the PnP configuration agent can assign the interrupt to be used by the PCI or PnP device. If your system contains an ISA Legacy card that uses one of these interrupts, select Used By ISA Card for that interrupt.

**NOTE**

*IRQ 3, 4, 5, and 7 may not be available in this option, depending on the setting chosen for the COM1, COM2 and parallel ports in the Peripheral Configuration Subscreen.*

### 3.12.11 Event Logging Configuration

This section describes the options available in the Event Logging Configuration subscreen.

#### 3.12.11.1 Event Log Capacity

This information field tells whether or not the log is full.

#### 3.12.11.2 Event Log Count Granularity

Defines the number of log events that must occur before the event log is updated. The default is 10 events.

#### 3.12.11.3 Event Time Granularity (Minutes)

Defines the amount of time that must pass before the event log is updated. The default is 30 minutes.

### 3.12.11.4 Event Log Control

Allows users to enable or disable event logging. The options are All Events Enabled, ECC Events Disabled, or All Events Disabled. The default is All Events Enabled.

### 3.12.11.5 Clear Event Log

Sets a flag that clears the event log on the next pass through POST. The options are Keep and On Next Boot. The default is Keep.

### 3.12.11.6 Mark Existing Events as Read

Marks all events already in the log as having been not read (Do Not Mark) or read (Mark). The options are Do Not Mark and Mark. The default is Do Not Mark.

### 3.12.11.7 Event Log Subscreens

The bottom of the Event Log screen includes several information fields that display information about the date and time of the last event of a specific type, as well as a count of how many events of that type are logged. Selecting a field and pressing Enter brings up a subscreen that shows information specific to that event type. Event types for which subscreens are availalbe include:

- Single Bit ECC Events
- Multiple Bit ECC Events
- Pre-Boot Events
- Logging Disabled Certain Events
- System Limit Exceeded Events

The subscreens presented for each of these event types are described in Table 45. Note that the initial three lines of information for all screens cover the same information.

**Table 45. Event Log Subscreens**

| Event Type | Subscreen Detail | Initial Value |
|---|---|---|
| Single Bit ECC Events | Date of Last Occurrence<br>Time of Last Occurrence<br>Total Count of Events/Errors<br>Memory Bank with Errors | None<br>None<br>None<br>None |
| Multiple Bit ECC Events * | Memory Bank with Errors | None |
| Pre-Boot Events * | POST ERRORS FOUND: | None |
| Logging Disabled Certain Events * | Event Type Disabled | None |
| System Limit Exceeded Events * | Type of System Limit Error | None |

* The first three lines of the subscreen detail are the same as is shown for the Single Bit ECC Events type.

## 3.12.12 Security Screen

This section describes the two access modes that can be set using the options found on the Security screen, and then describes the Security screen options themselves.

### 3.12.12.1 Administrative and User Access Modes

The options on the Security screen menu make it possible to restrict access to the Setup program by enabling you to set passwords for two different access modes: Administrative mode and User mode.

In general, Administrative mode has full access to the Setup options, whereas User mode has restricted access to the options. Thus, by setting separate Administrative and User passwords, a system administrator can limit who can change critical Setup values. The actual limitations depend on whether either the Administrative or User passwords or both are set. (See the table below for a description of how the passwords actually work together.)

To limit access to who can boot the system, set the User password. This is the password that the system asks for before booting. If only the Administrative password is set, the system boots up without asking for a password. If both passwords are set, you can enter either password to boot the system.

Table 46 shows the effects of setting the Administrative and User passwords. (The table is for reference only, and is not shown on the Security screen.) In the table, the statement "Can change a limited number of options" means you can change the system date and time, the power management hot key, the User password, the security hot key, and unattended start.

**Table 46. Administrative and User Password Functions**

| Password Set | Administrative mode can . . . | User mode can . . . | Password Required During Boot Process |
|---|---|---|---|
| Neither | Can change all options* | Can change all options* | None |
| Administrative only | Can change all options | Can change a limited number of options | None |
| User only | N/A | Can change all options | User |
| Both | Can change all options | Can change a limited number of options | Administrative or User |

* If no password is set, any user can change all Setup options.

## 3.12.13 Security Screen Options

### 3.12.13.1 User Password is

Reports if there is a User password set. There are no options.

### 3.12.13.2 Administrative Password is

Reports if there is an Administrative password set. There are no options.

### 3.12.13.3 Set User Password

Sets the User password. The password can be up to seven alphanumeric characters.

### 3.12.13.4 Set Administrative Password

Sets the Administrative password. The password can be up to seven alphanumeric characters.

## 3.12.14 Exit Screen

This section describes the different ways to exit and save or not save changes made in the Setup program.

### 3.12.14.1 Exit Saving Changes

Saves the changes to CMOS RAM and exits the Setup program. You can also press the <F10> key anywhere in the Setup program to do this.

### 3.12.14.2 Exit Discarding Changes

Exits the Setup program without saving any changes. This means that any changes made while in the Setup program are discarded and NOT SAVED. Pressing the <Esc> key in any of the four main screens will do this.

### 3.12.14.3 Load Setup Defaults

Resets all of the setup options to their defaults. You can also press the <F5> key anywhere in the Setup program to do this.

This selection loads the default Setup values from the ROM table.

### 3.12.14.4 Discard Changes

Discards any changes you made during the current Setup session without exiting the program. You can also press the <F6> key anywhere in the Setup program to do this.

This selection loads the CMOS RAM values that were present when the system was turned on.

# 4 Error Messages and Beep Codes

## 4.1 BIOS Beep Codes

**Table 47. BIOS Beep Codes**

| Beeps | Error Message | Description |
|---|---|---|
| 1 | Refresh Failure | The memory refresh circuitry on the motherboard is faulty. |
| 2 | Parity Error | Parity is not supported on this product, will not occur. |
| 3 | Base 64 KB Memory Failure | Memory failure in the first 64 KB. |
| 4 | Timer Not Operational | Memory failure in the first 64 KB of memory, or Timer 1 on the motherboard is not functioning. |
| 5 | Processor Error | The CPU on the motherboard generated an error. |
| 6 | 8042 - Gate A20 Failure | The keyboard controller (8042) may be bad. The BIOS cannot switch to protected mode. |
| 7 | Processor Exception Interrupt Error | The CPU generated an exception interrupt. |
| 8 | Display Memory Read/Write Error | The system video adapter is either missing or its memory is faulty. This is not a fatal error. |
| 9 | ROM Checksum Error | ROM checksum value does not match the value encoded in BIOS. |
| 10 | CMOS Shutdown Register Rd/Wrt Error | The shutdown register for CMOS RAM failed. |

## 4.2 PCI Configuration Error Messages

The following PCI messages are displayed as a group with bus, device and function information.

**Table 48. PCI Configuration Error Messages**

| Error Message | Explanation |
|---|---|
| NVRAM Checksum Error, NVRAM Cleared | The ESCD data was reinitialized because of an NVRAM checksum error. Try rerunning the ICU. |
| System Board Device Resource Conflict | A non Plug and Play ISA card has requested a resource that is already in use. |
| Primary Output Device Not Found | The designated primary output device (printer, modem, or other, if output is redirected) could not be found. |
| Primary Input Device Not Found | The designated primary input device (keyboard, mouse, or other, if input is redirected) could not be found. |
| Primary Boot Device Not Found | The designated primary boot device (hard disk drive, diskette drive, or CD-ROM drive) could not be found. |
| NVRAM Cleared By Jumper | The “Clear CMOS” jumper has been moved to the “CLR” position and CMOS RAM has been cleared. |

continued ☛

**Table 48. PCI Configuration Error Messages (continued)**

| Error Message | Explanation |
|---|---|
| NVRAM Data Invalid, NVRAM Cleared | Invalid entry in the ESCD. |
| Static Device Resource Conflict | A non Plug and Play ISA card has requested a resource that is already in use. |
| PCI Error Log is Full. | If and when more than 15 PCI conflict errors are detected the log full message is displayed. If this message displays, no additional PCI errors can be logged. |
| Floppy Disk Controller Resource Conflict | The floppy disk controller has requested a resource that is already in use. |
| Primary IDE Controller Resource Conflict | The primary IDE controller has requested a resource that is already in use. |
| Secondary IDE Controller Resource Conflict | The secondary IDE controller has requested a resource that is already in use. |
| Parallel Port Resource Conflict | The parallel port has requested a resource that is already in use. |
| Serial Port 1 Resource Conflict | Serial port 1 has requested a resource that is already in use. |
| Serial Port 2 Resource Conflict | Serial port 2 has requested a resource that is already in use. |

The following PCI messages are chained together to give an error message.

**Table 49. Chained PCI Error Messages**

| Error Message | Explanation |
|---|---|
| PCI *resource name* Conflict: Bus: *aa*, Device *bb*, Function: *cc*<br><br>where | A PCI resource conflict has been detected. The full message Is formed by chaining the fixed text with the variable text indicated by italics. Each message variation provides details on the type of resource conflict, and detailed information on the bus, device, and function associated with the resource conflict. |
| PCI *I/O Port* Conflict: | Two devices requested the same I/O port, resulting in a conflict. |
| PCI *Memory* Conflict: | Two devices requested the same memory address, resulting in a conflict. |
| PCI *IRQ* Conflict: | Two devices requested the same IRQ address, resulting in a conflict. |
| Bus: *aa* | Is a hexadecimal number corresponding to the PCI bus number. For desktop motherboards, the bus number is 00. |
| Device: *bb* | Is a hexadecimal number corresponding to the PCI device. |
| Function: *cc* | Is a hexadecimal number corresponding to the active PCI function within a device. |

## 4.3 BIOS Error Messages

**Table 50. BIOS Error Messages**

| Error Message | Explanation |
|---|---|
| Gate A20 Error | Gate A20 on the keyboard controller is not working. |
| Address Line Short! | Error in the address decoding circuitry on the motherboard. |
| Cache Memory Bad, Do Not Enable Cache! | Cache memory is defective. Replace it. |
| CH-2 Timer Error | Most AT systems include two timers. There is an error in timer 2. |
| CMOS Battery State Low | CMOS RAM is powered by a battery. The battery power is low. Replace the battery. |
| CMOS Checksum Failure | After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run Setup. |
| CMOS System Options Not Set | The values stored in CMOS RAM are either corrupt or nonexistent. Run Setup. |
| CMOS Display Type Mismatch | The video type in CMOS RAM does not match the type detected by the BIOS. Run Setup. |
| CMOS Memory Size Mismatch | The amount of memory on the motherboard is different than the amount in CMOS RAM. Run AMIBIOS Setup. |
| CMOS Time and Date Not Set | Run Setup to set the date and time in CMOS RAM. |
| Diskette Boot Failure | The boot disk in floppy drive A: is corrupt. It cannot be used to boot the system. Use another boot disk and follow the screen instructions. |
| Display Switch Not Proper | The display jumper is not implemented on this product. This error should not occur. |
| DMA Error | Error in the DMA controller. |
| DMA #1 Error | Error in the first DMA channel. |
| DMA #2 Error | Error in the second DMA channel. |
| FDD Controller Failure | The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down. |
| HDD Controller Failure | The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down. |
| INTR #1 Error | Interrupt channel 1 failed POST. |
| INTR #2 Error | Interrupt channel 2 failed POST. |
| Invalid Boot Diskette | The BIOS can read the disk in floppy drive A:, but cannot boot the system. Use another boot disk. |
| Keyboard Is Locked...Unlock It | The keyboard lock on the system is engaged. The system must be unlocked to continue. |
| KB/Interface Error | There is an error in the keyboard connector. |
| On Board Parity Error | Parity error detected in system memory. |

## 4.4 ISA NMI Messages

**Table 51. ISA NMI Messages**

| ISA NMI Message | Explanation |
|---|---|
| Memory Parity Error at xxxxx | Memory failed. If the memory location can be determined, it is displayed as xxxxx. If not, the message is Memory Parity Error ????. |
| I/O Card Parity Error at xxxxx | An expansion card failed. If the address can be determined, it is displayed as xxxxx. If not, the message is I/O Card Parity Error ????. |
| DMA Bus Time-out | A device has driven the bus signal for more than 7.8 microseconds. |